Design of Emerging Mixed-Signal Controlled SMPS

Prof. Aleksandar Prodić

E-mail: prodic@ece.utoronto.ca

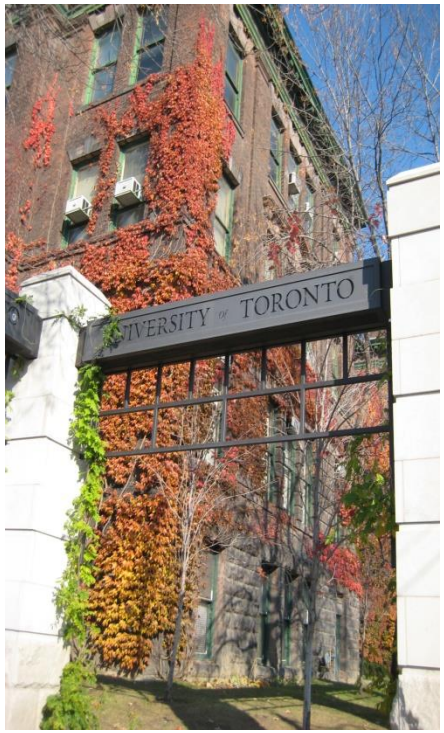
Laboratory for Power Management and Integrated SMPS

University of Toronto, E. Rogers ECE Department

http://www.ele.utoronto.ca/power_management/publications.html

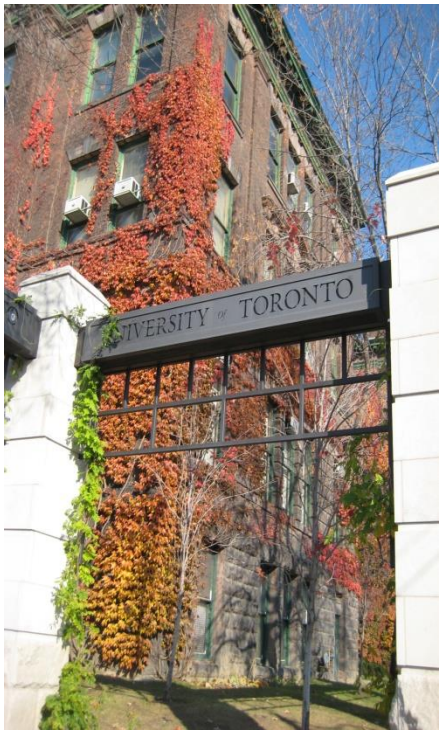
University of Toronto

- *Formed in 1827*
- *84,000 students*
- *Around 12,500 faculty members*
- *Yearly budget exceeds $2 billion*
- *Research grants and contracts $1.2 billion/year*



University of Toronto

- *The largest and most known University in Canada*
- *Constantly ranks among top 10 - 20 in the world*
- *10 Nobel Laureates (5 in the last 20 years)*
- *Sir Frederick Banting and J.J.R. Macleod won the Nobel Prize in 1923 for their work with Charles Best in the discovery of the role of insulin in controlling diabetes*



The Edward S. Rogers Department of Electrical and Computer Engineering

- *Formed in 1909*
- *2,500 students*
- *85 faculty members*
- *The ECE department constantly ranks among top in the world*
- *Notable faculty members: Ted Davison, W.M. Wonham, Bruce Francis, Kenneth Smith, Adel Sedra, Andre Salama*

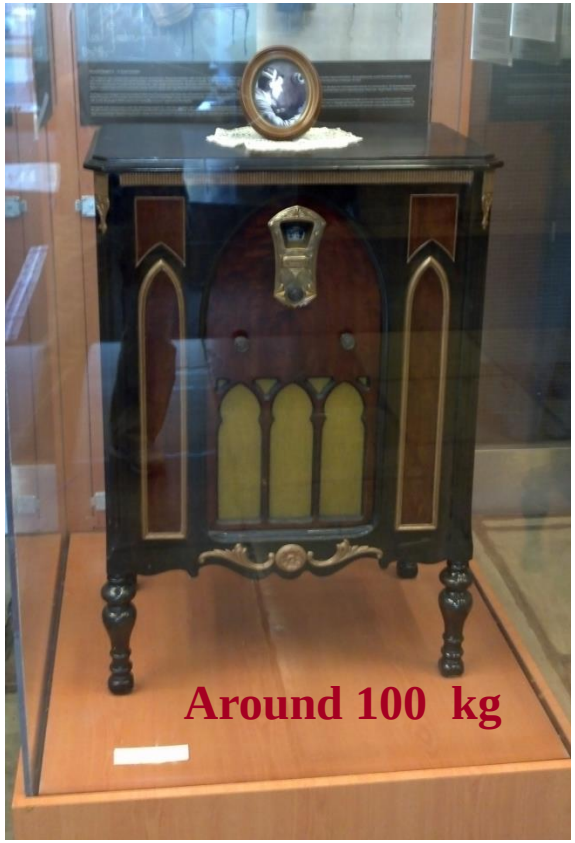
Research Groups

- *Biomedical*
- *Computer Engineering*
- *Communications*
- *Electromagnetics*
- *Photonics*
- *Electronics*
- *Energy Systems*
- *Control Systems*

Laboratory for Power Management and integrated SMPS

About High Power Density Power Supplies from

42” or 105 cm

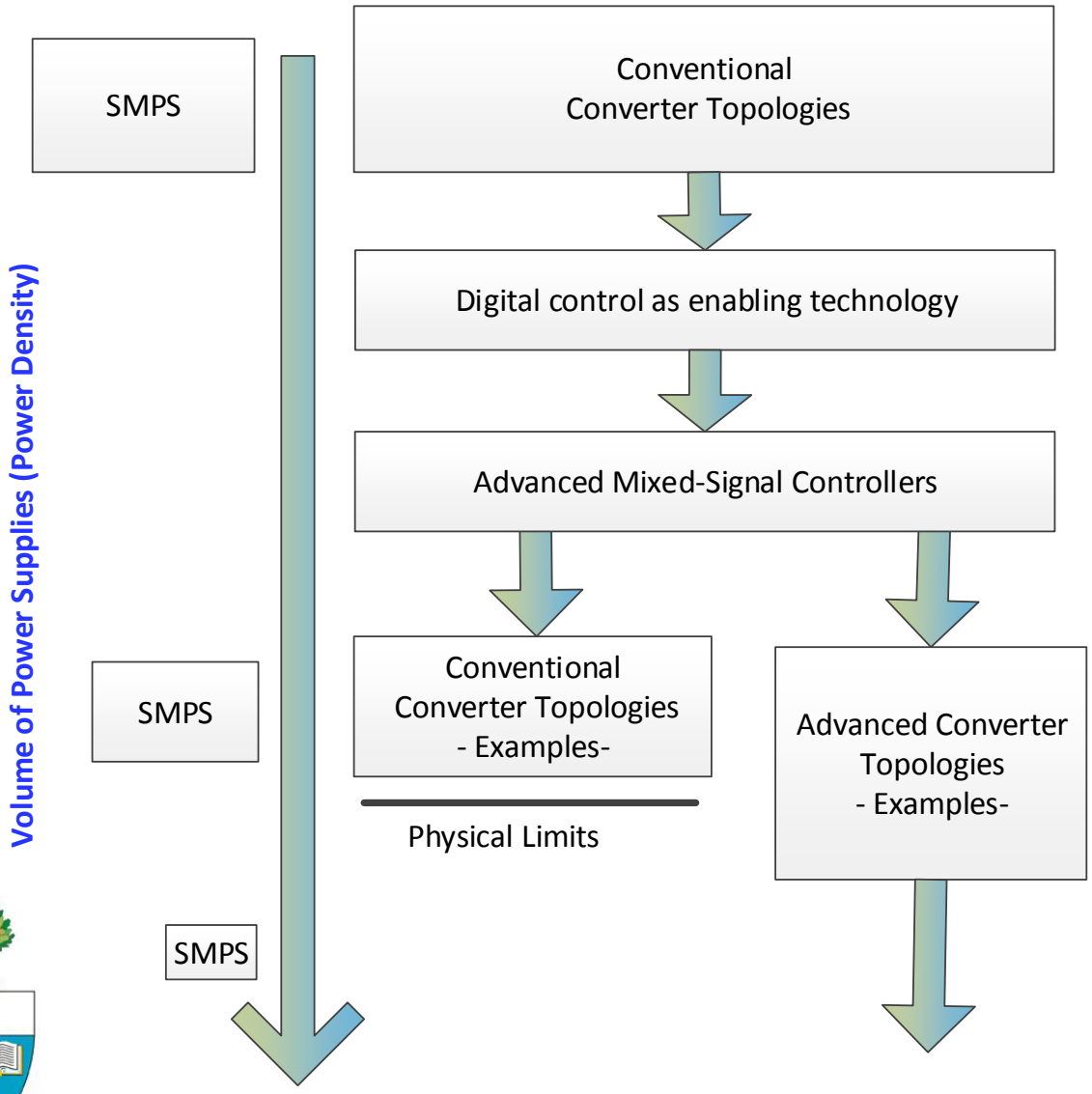


- *Allowed a large number of households to have daily access to information*
- *Reduced the volume and weight by using more efficient electronics (increased power density)*

Portable Radio !

Main motivation: to reduce the volume and weight of power supplies, by far the largest part of previous radios

Our Seminar Covers The Same Ideas: Outline



Main motivation: to reduce the volume and weight of switch mode power supplies (SMPS) while improving power processing efficiency.

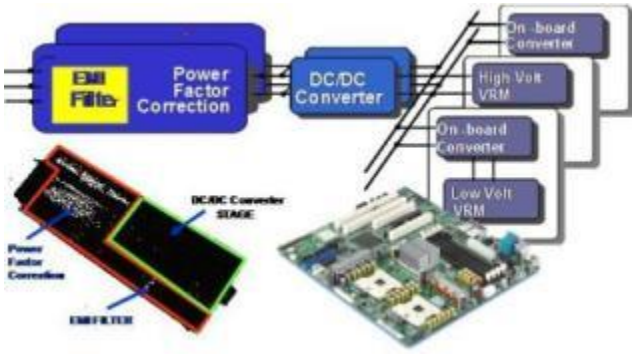
Outline

Part I: Introduction to High Power Density SMPS

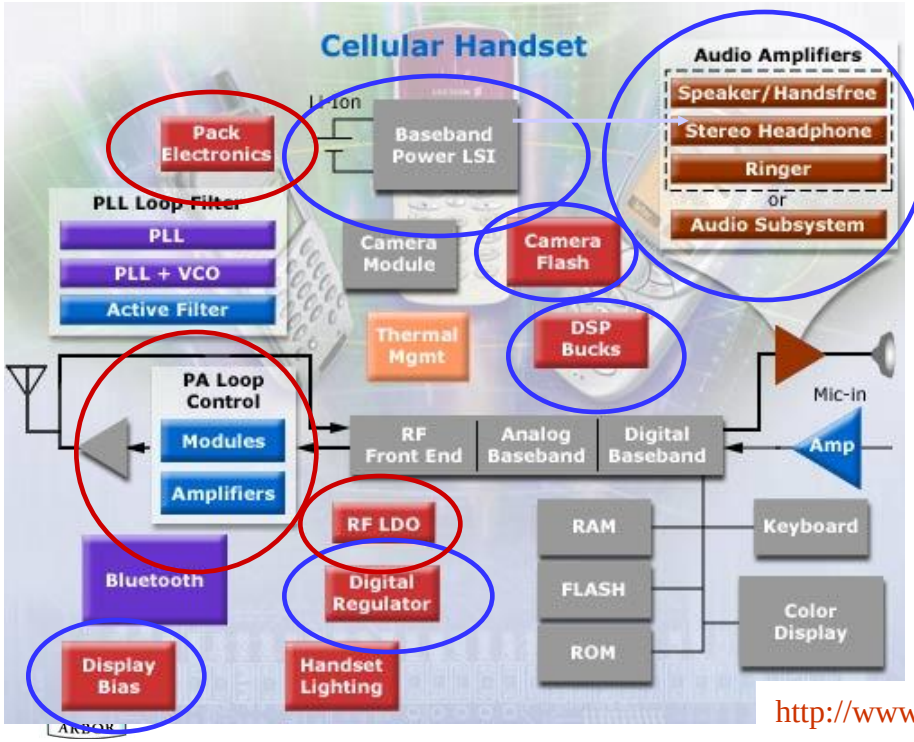
Switch Mode Power Supplies (SMPS) and their applications

- Power management system architectures and applications
  - Typical SMPS functions and structures
  - Power stage topologies and controllers

Computer Server Application



http://www.cpes.vt.edu/



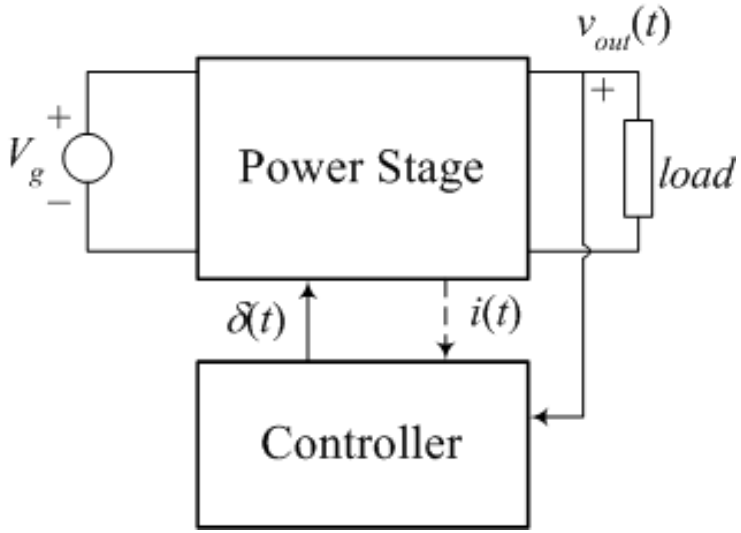
http://www.ti.com

Outline

Part I: Introduction to High Power Density SMPS

Switch Mode Power Supplies (SMPS) and their applications

- Requirements for high power density SMPS (volume and efficiency)
- Controller architectures
  - Voltage mode controllers (VMC)
  - Current programmed control (CPM)
  - Controllers for frequency-regulated topologies



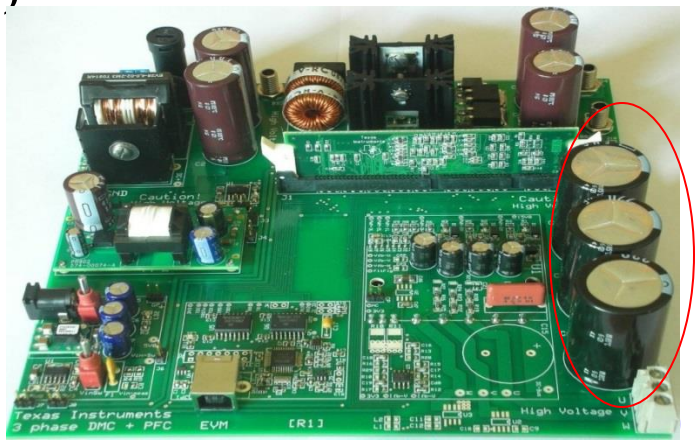
Power Stage + Controller = Switch Mode Power Supply (SMPS)

Outline

Part I: Basic Principles of Volume Reduction (Capacitors)

Volume of Reactive Components – Capacitors

- Size of the output and input filter capacitors
  - Energy storage capacity and the capacitor volume
  - Capacitor volume drivers (nominal voltage & charge fluctuation)
- Switching frequency, charge fluctuation (ripple), and design tradeoffs
- Feedback loop and charge fluctuation (voltage deviation)
  - Relation between the capacitor volume and transient response
  - Design tradeoffs (size of the input filter)
  - Influence of the nominal voltage on the charge fluctuation

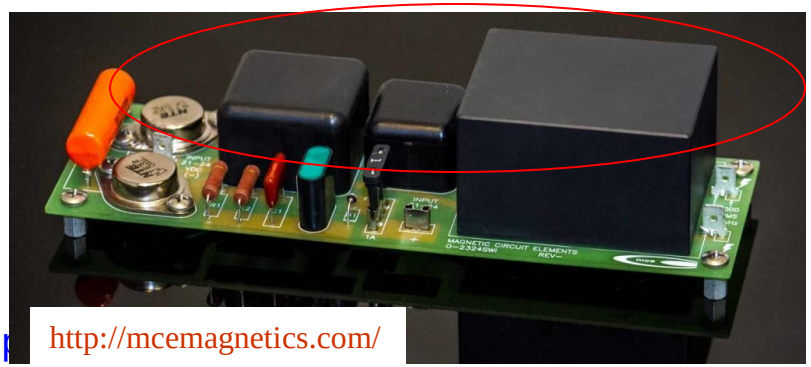


Outline

Part I: Basic Principles of Volume Reduction (Inductors)

Volume of Reactive Components – Inductors

- Size of filter and energy transfer inductors
  - Energy storage capacity and inductor volume
  - Inductor volume drivers (peak current & flux linkage)
  - Principles of flux linkage minimization
  - Influence of the inductor current
- Influence of feedback on the inductor volume (inductor peak current)
- Converter topologies and inductor volume (flux linkage) reduction



http://mcemagnetics.com/

Outline

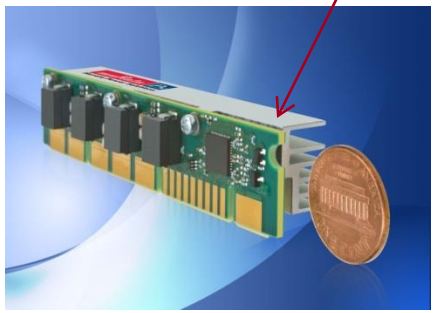
Part I: Power Losses, Efficiency, and Volume Reduction

Power Losses and Volume

- Relation between power losses and cooling requirements
  - Hot spots and heat sinks
  - Distribution of power losses
  - Emerging components
- Influence of feedback on the converter efficiency

Part I: Main Volume Drivers in Conventional Topologies - Examples

- Point of load converters (PoL Converters)
- Ac/dc converters (Boost and Flyback based solutions)
- Resonant topologies



http://murata.com/

Outline

Part II: Analog, Digital and Mixed-Signal Control of Power Converters

Review of Control Methods and Practical Challenges

- Voltage mode control methods (PWM, voltage hysteresis, V^2)
- Current mode controllers (Average & peak CPM control)
- Frequency based control:
  - Light load control methods
  - Control of resonant converters
  - Control of DAB (and back-to-back VSC topologies)

System Modeling and Practical Implementation of Analog Controller

- Modeling of voltage loop controlled system and design of control loop
  - Practical implementation challenges
- Control loop design for current programmed mode controllers
  - Practical implementation challenges

Outline

Part II: Digital and Mixed-Signal Controllers

Digital and Mixed-Signal Control

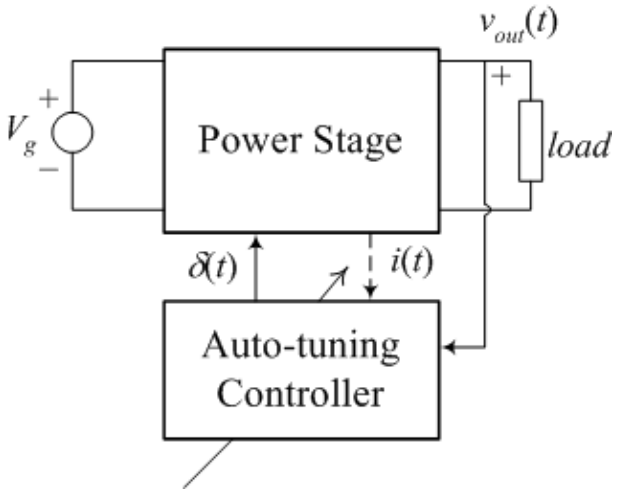
- Comparison of analog, digital and mixed-signal controller implementations
- Current state of the art (penetration of digital in low power applications)
- Power consumption, complexity, and silicon area
- Discretization effects and limit cycling

Digital Controller Implementation and Design Examples

- Modeling of voltage loop controlled system and design of control loop
- Principle of silicon and power efficient controller implementation
    - Determination of minimum hardware requirements
- Hardware-efficient implementation of functional blocks and on-chip implementation

Outline

Part III: Advanced Mixed-Signal Controllers



Auto-tuning (plug and play) controllers

- Network emulator based control
- Limit-cycling based solutions
- Controllers for on-line efficiency optimization

Optimal response controllers

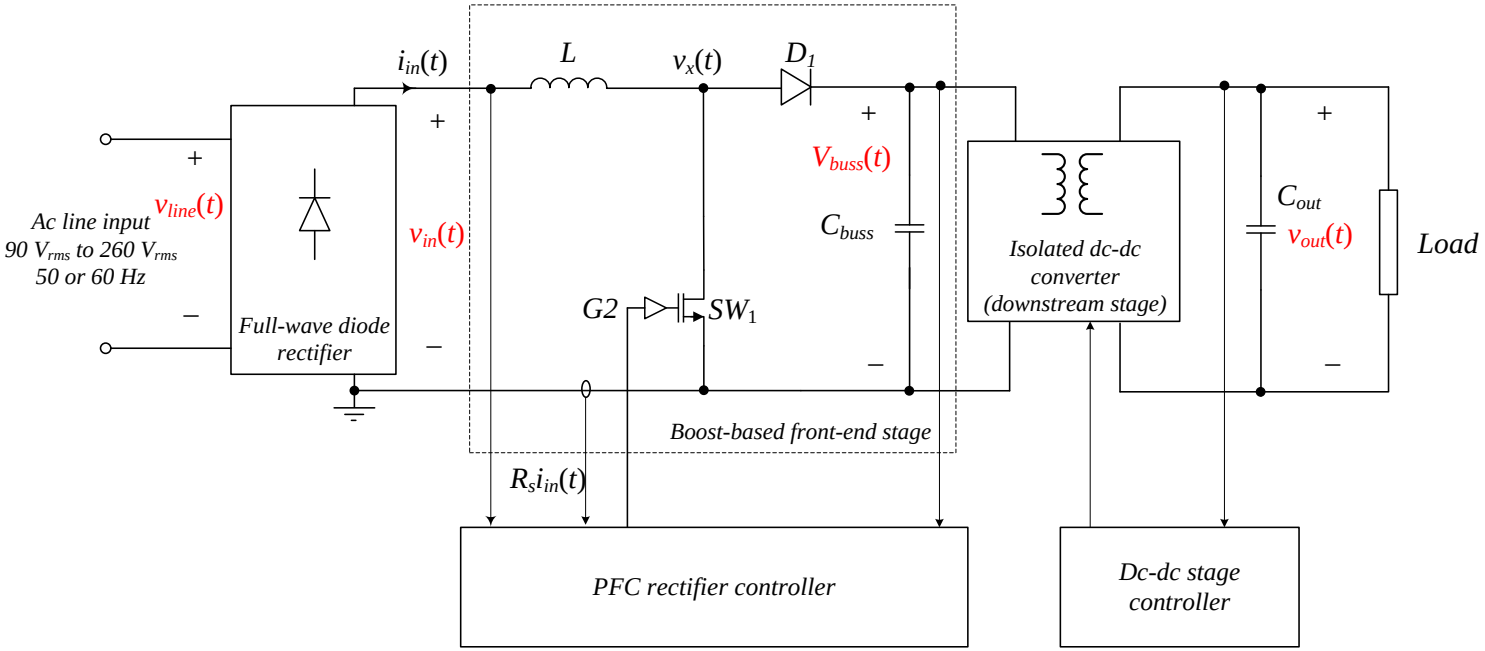
- Optimal (proximity) time controllers
- Minimum deviation controllers (for direct and indirect energy converters)
- Optimal control of resonant (LLC) converters

Outline

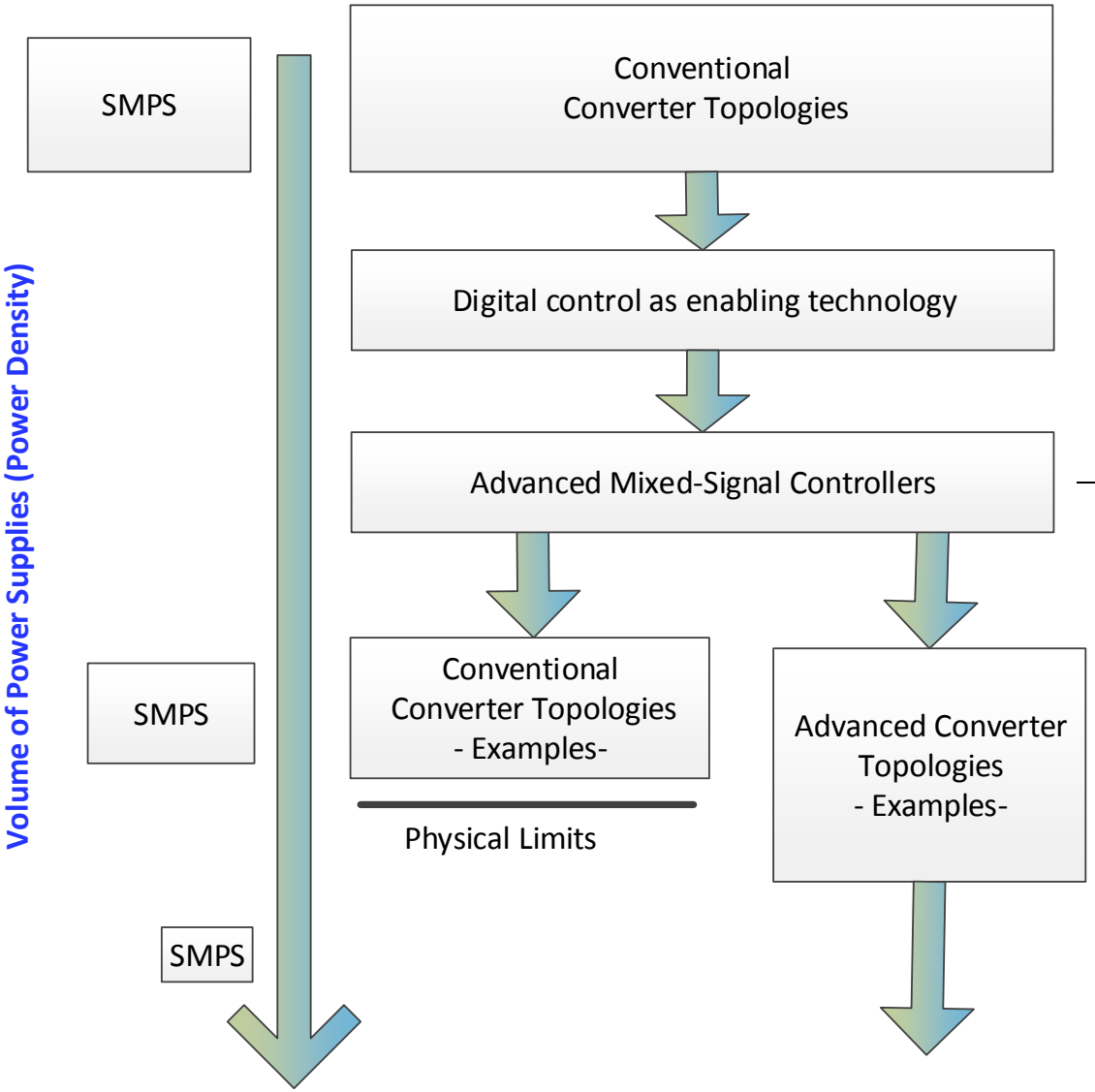
Part III: Advanced Mixed-Signal Controllers

Advanced controllers for rectifiers with power factor correction (PFC)

- PFC rectifier with predictive current control
- PFC with wide-bandwidth voltage loops



Seminar Outline



Seminar day 1

Seminar day 2

Outline

Part IV: High Power Density Mixed-Signal Controlled Dc-Dc Converters

Physical Limits of Conventional Topologies and Principles of Volume Reduction

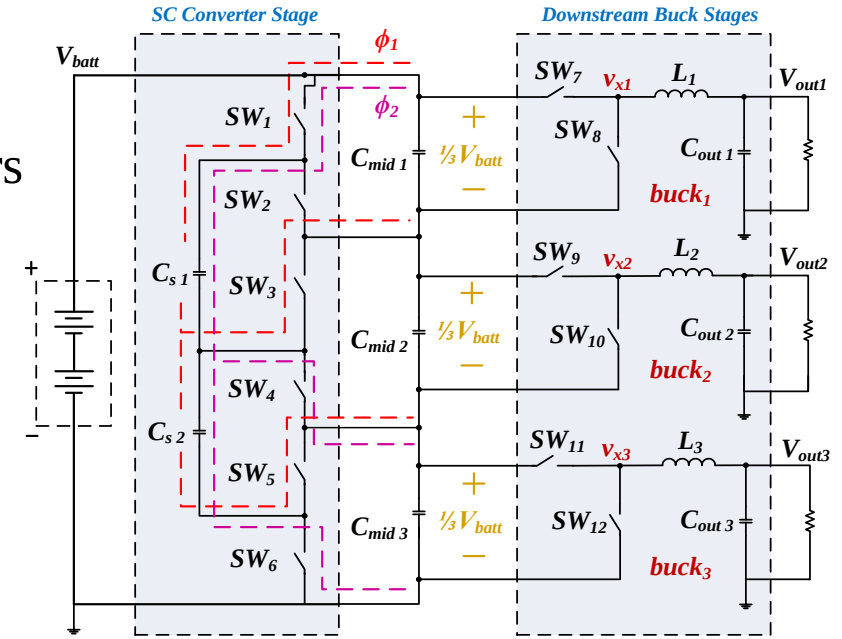
- Transient and efficiency limits
- Basic principles of volume reduction (short review)

Multi- Level and Hybrid Dc-Dc Converters

- Multi-level converters (basic principles)
- Switched capacitor (SC) and hybrid converters
- Design examples

Modular Dc-Dc Converters

- Modular and partial power processing ideas
- Design examples



Outline

Part V: High Power Density Mixed-Signal Controlled Ac-Dc PFC Converters

Review of Conventional Rectifiers with PFC Architectures

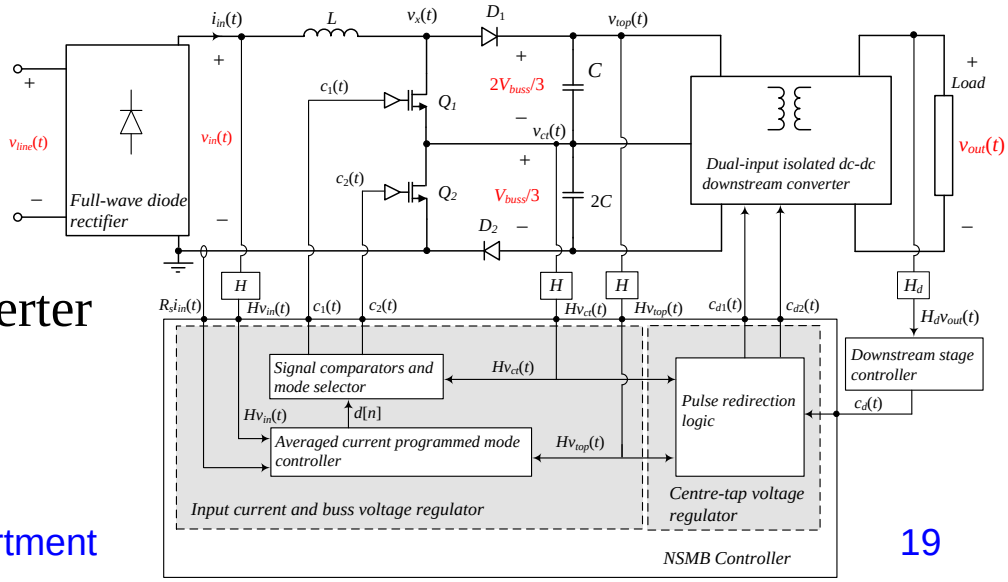
- DCM flyback
- Boost based PFC
- Inductor and capacitor volumes, cooling requirements

PFC with Ripple Cancellation

- Design challenges and principle of operation
- Controller design for ripple-cancellation systems

Modular and Multi-level PFC Structures

- Interleaved structures
- Multi-level PFC topologies
- Non-symmetric multi-level PFC converter



Part I

Introduction: Applications, Power Management Systems and SMPS Architectures

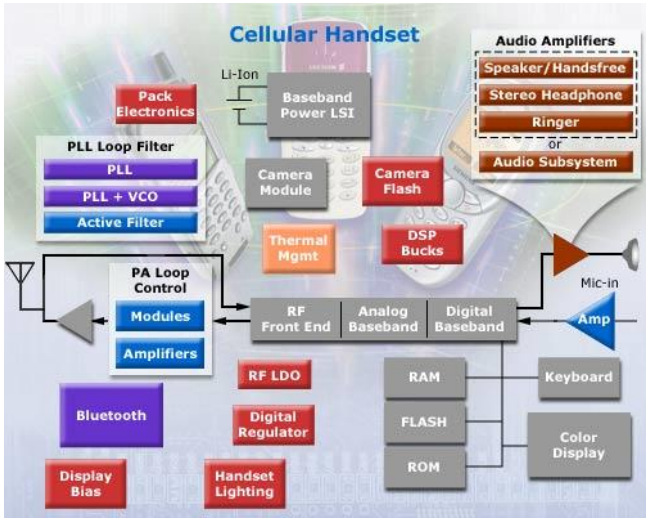
SMPS Applications

Portable Devices (fraction of W to several W-s) billions/year

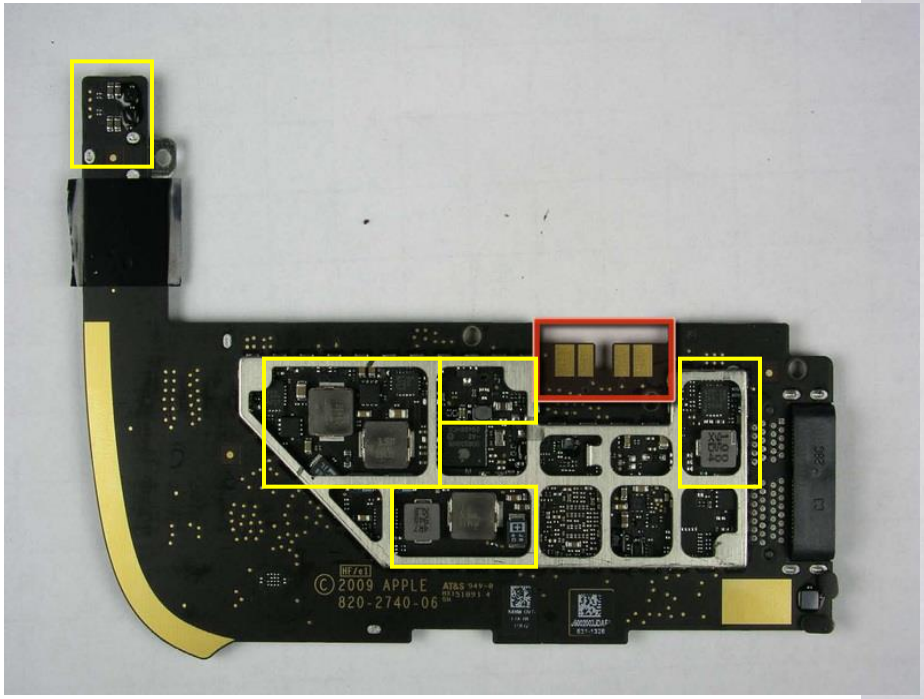
- Power supplies for functional components / hundreds of mW to few Watts
  - Point of Load converters
- Power management modules/ tens of Watts
- Adapters/chargers/ tens of Watts

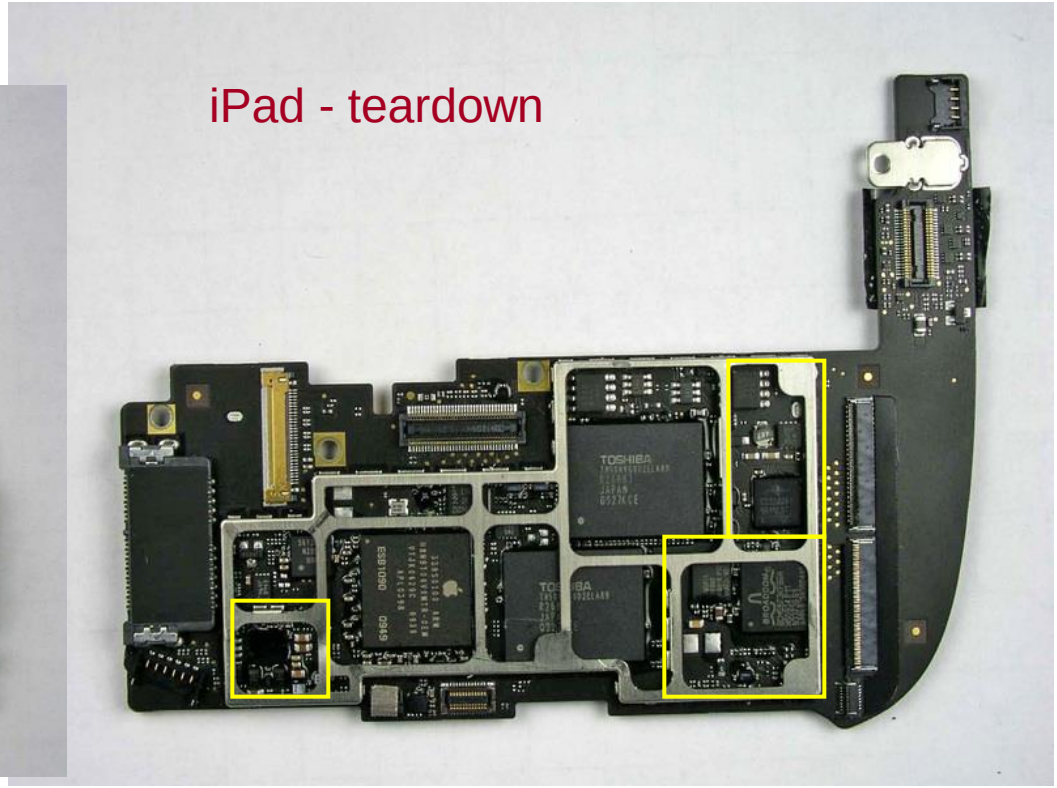
Lighting Applications (several W to tens of W)

- LED and HID Lamp Supplies (drivers)



SMPS in Portable/Consumer Electronics

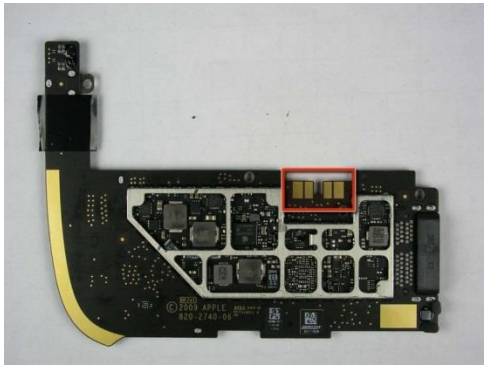




http://www.ifixit.com/Teardown/iPad-FCC-Teardown/2197/1

- *Dc-dc SMPS occupy between 12% and 80% of the total volume in modern electronics devices, communication equipment, computers…*

Portable, Consumer Electronics, Comm. Syst.



- *Power from a fraction of a watt to hundreds of watts*
- *Power management systems often have more than 30 different supplies*

SMPS Applications

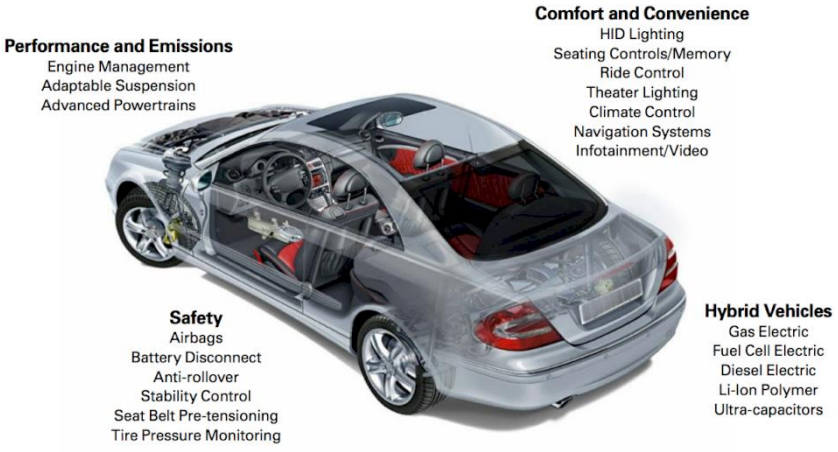
Computers, Comm., and Consumers Electronics (up to few hundred W)

- Power supplies for components/ several watts
- Voltage Regulator Modules (VRM-s), i.e. processor supply/ around 100 Watts
- Off-line power supplies and rectifiers with PFC / up to kW

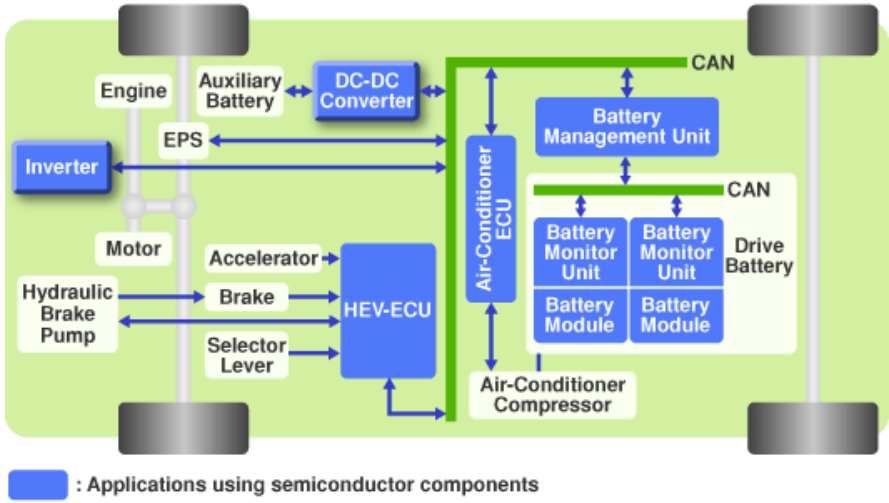
SMPS Applications

Automotive (several hundreds of watts to tens of kW)

- In car electronics and lighting (tens of watts to hundred of watts)
- Engine management unit and injection systems (hundreds of watts)
- Hybrid/electric drivetrains and chargers (up to tens/hundred of kW)



http://www.eeweb.com

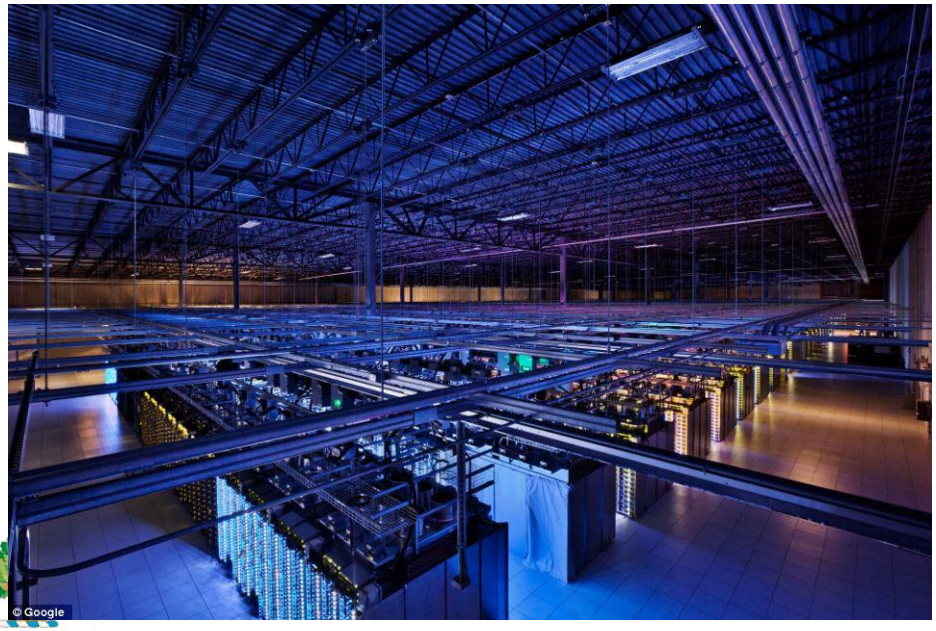


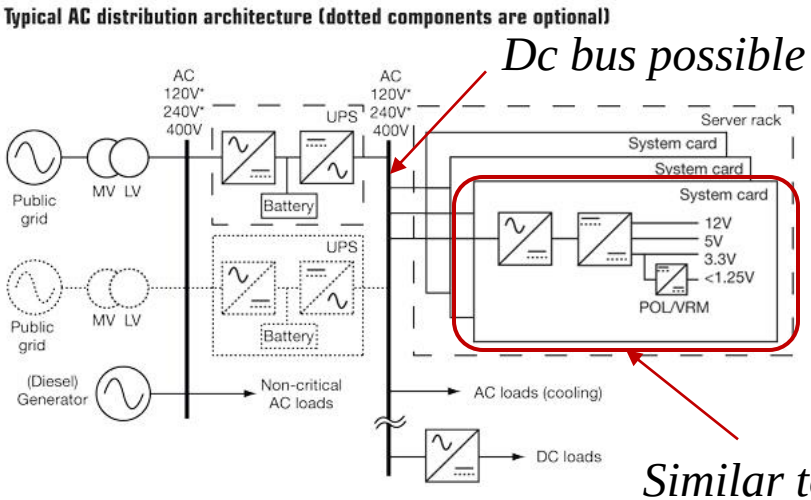
http://www.toshiba-components.com/automotive/evs.html

SMPS Applications

Servers and Server Farms (often MWs of total power)

- High step down ratio dc-dc converters (hundreds of watts)
- Ac/dc and dc/dc storage-connected units (up to tens of kW)





http://powerelectronics.com

Requirements for SMPS

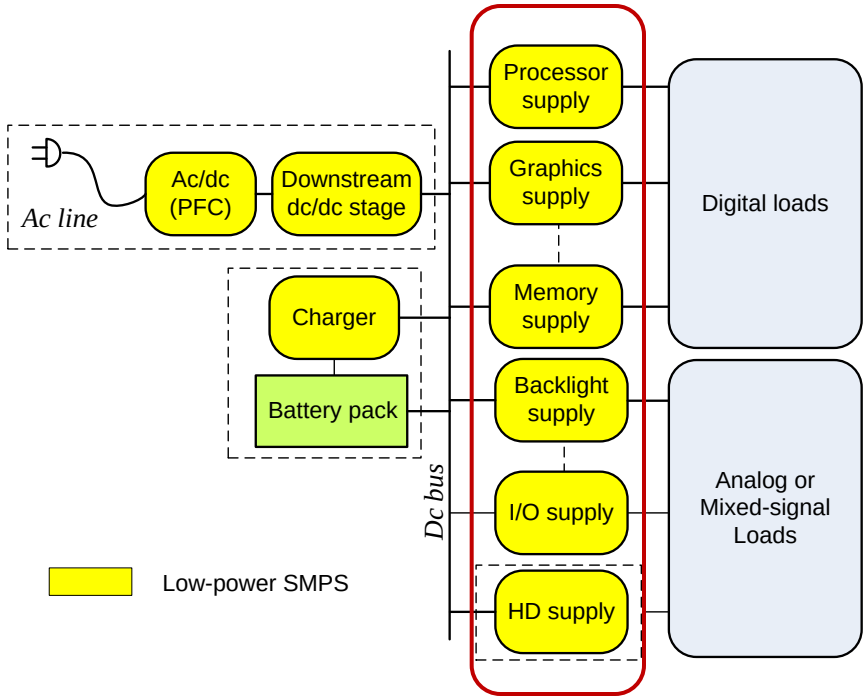
- *Low-volume and weight implementation (mobile, automotive)*
- *Low steady state power consumption (mobile, consum. electronics)*
- *High power efficiency (servers, consumer electronics, mobile)*
- *Cost-driven applications (all, mobile in particular)*

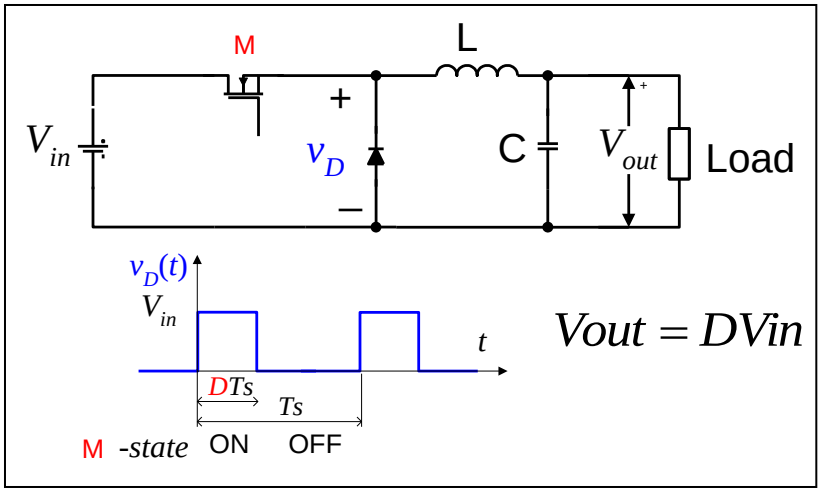
" *1 cent is a lot of money in mobile industry*" F. Carabolante

-Budgets given for total volume and quiescent power consumption are usually very constrained

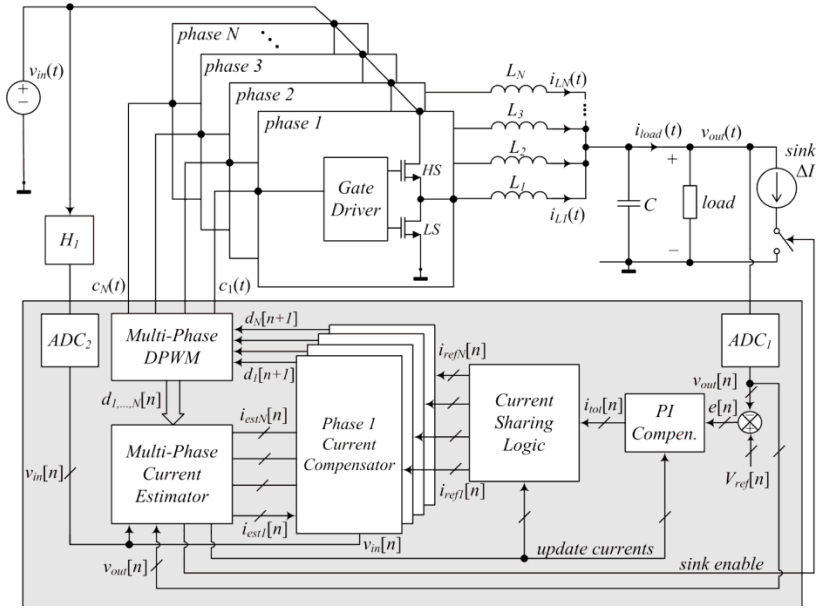
-Many functional blocks of modern devices compete for volume and power

SMPS Topologies and Basic Principles (Buck)

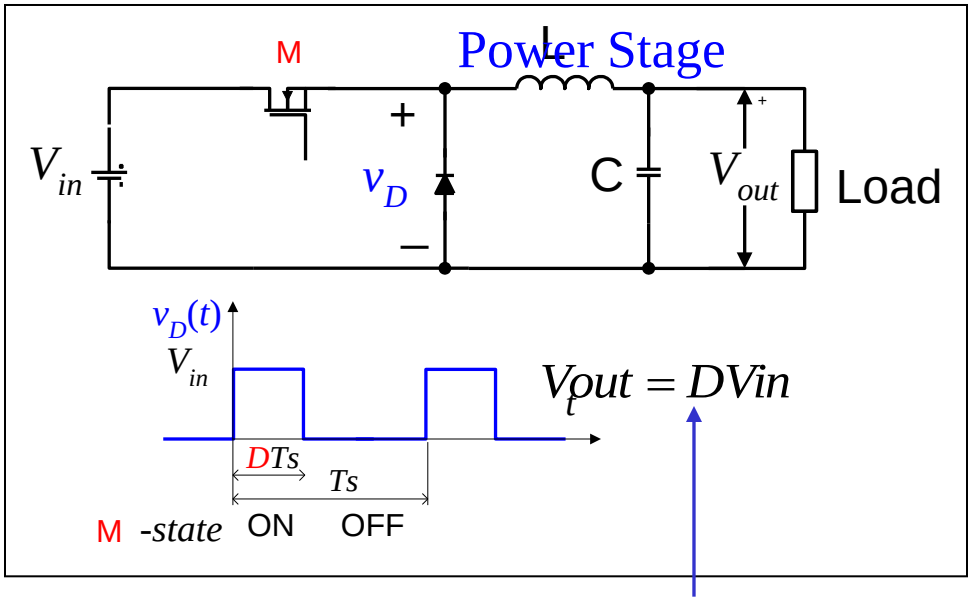




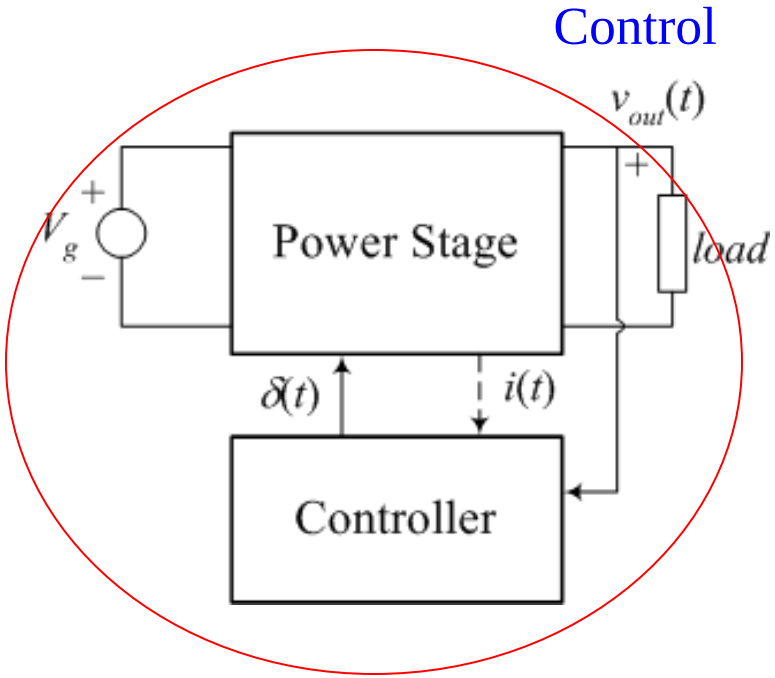
Point of Load (PoL) converters



SMPS Basic Principles: Buck Example



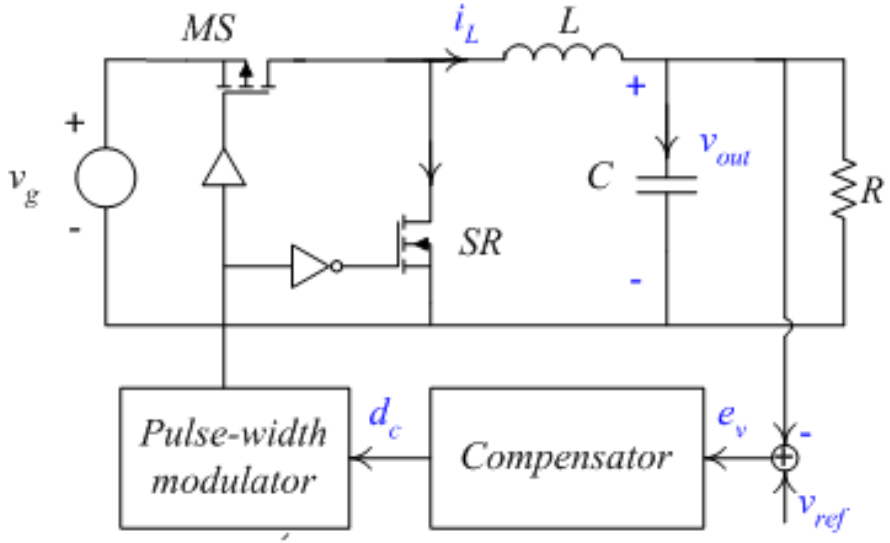
Duty ratio (control variable)



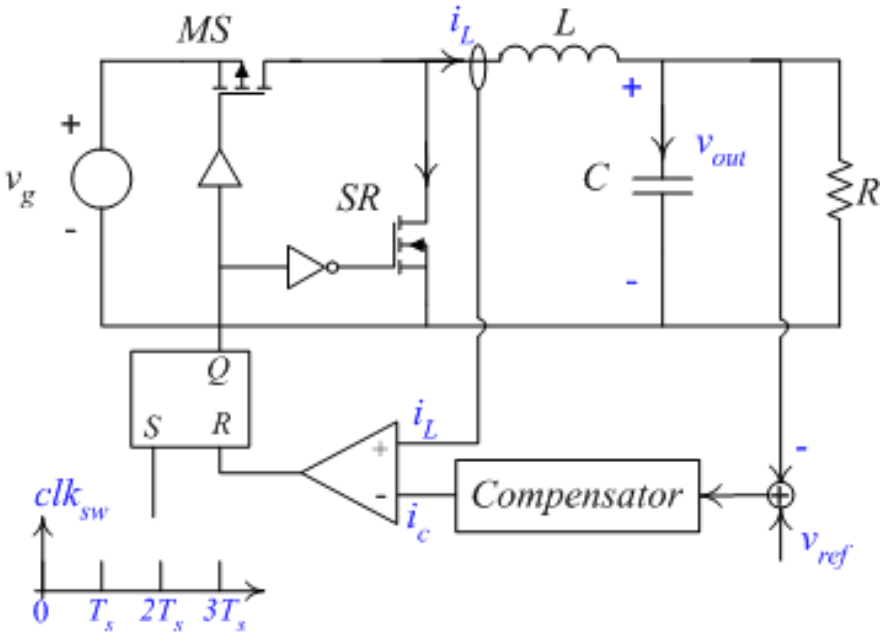
Power Stage + Controller = Switch Mode Power Supply (SMPS)

- Higher switching frequency implies smaller LC components.
- Ideally, no losses (in reality - high efficiency).
- Control requires special attention (nonlinear time-varying system).

Common Controller Structures (Dc-Dc Converters)



PWM voltage mode control

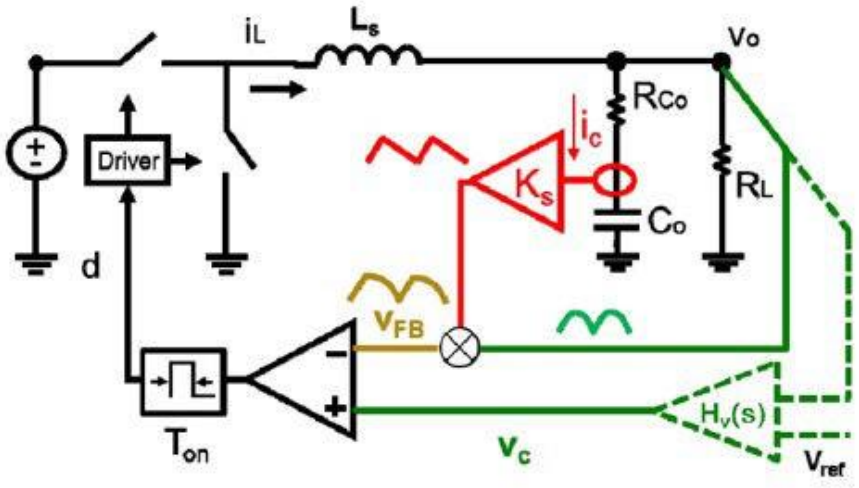


Current-programmed mode

Direct control of the output voltage

Indirect control, by setting the current for the next switching cycle (Note)

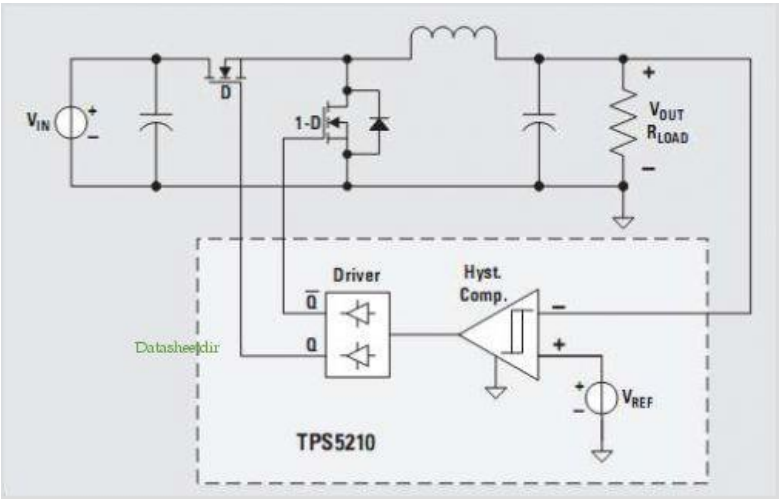
Common Controller Structures (Dc-Dc Converters)



http://www.cpes.vt.edu

V^2 control

In this case information about the capacitor current (rather than inductor current is used) – fast response and stability



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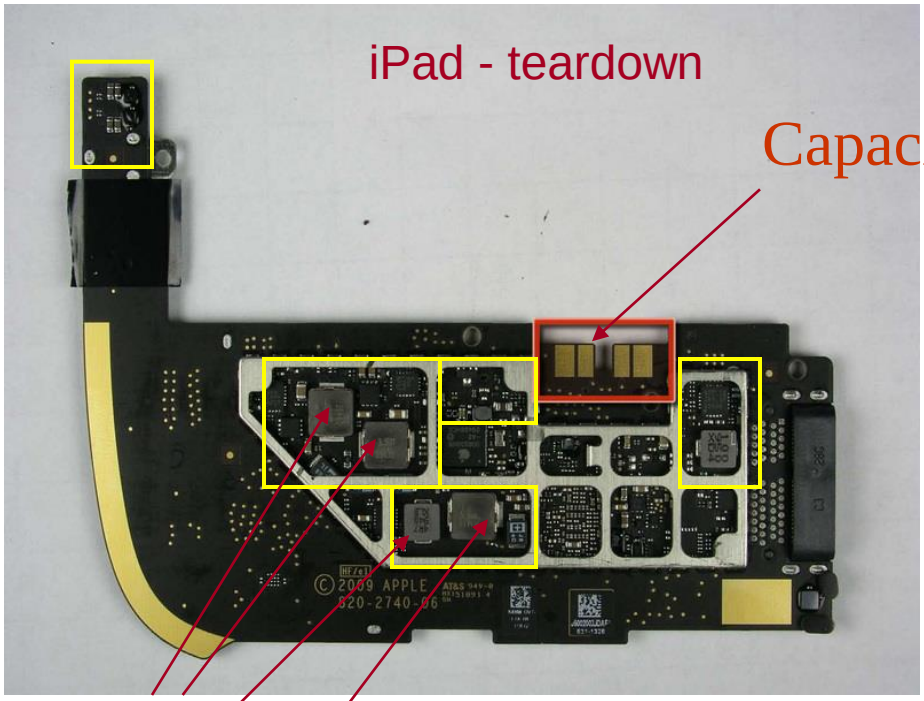
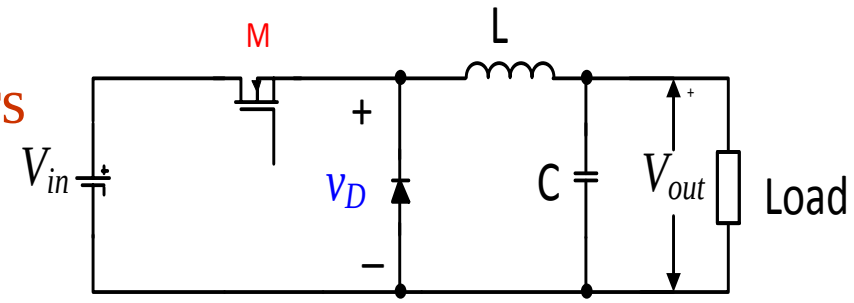
Hysteretic Control

Variable frequency control based on output voltage measurement only

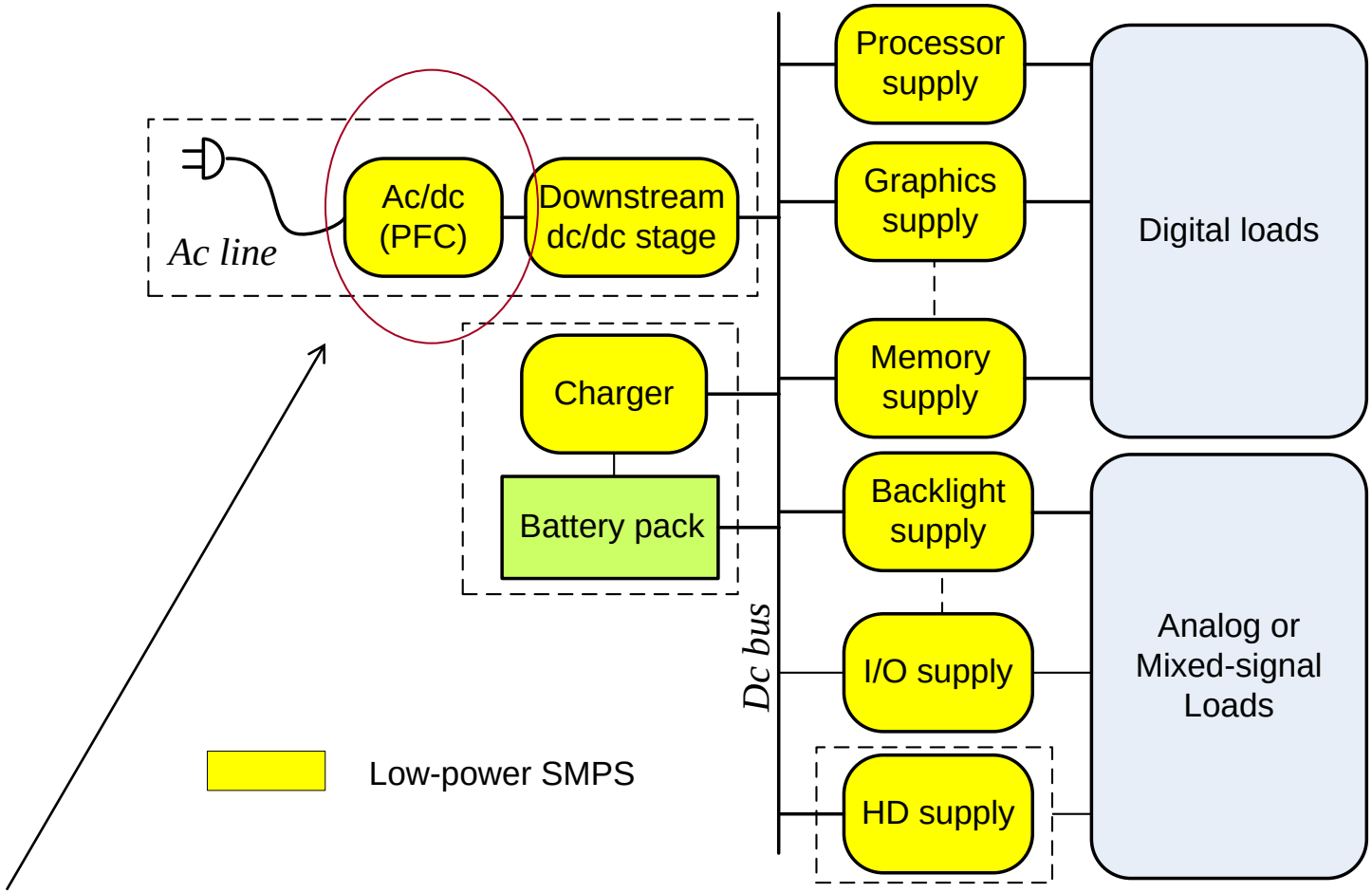
Volume of the SMPS





- *Most of the volume occupied by passive components and cooling components*
- *The passives often dominate the overall cost of the supplies*

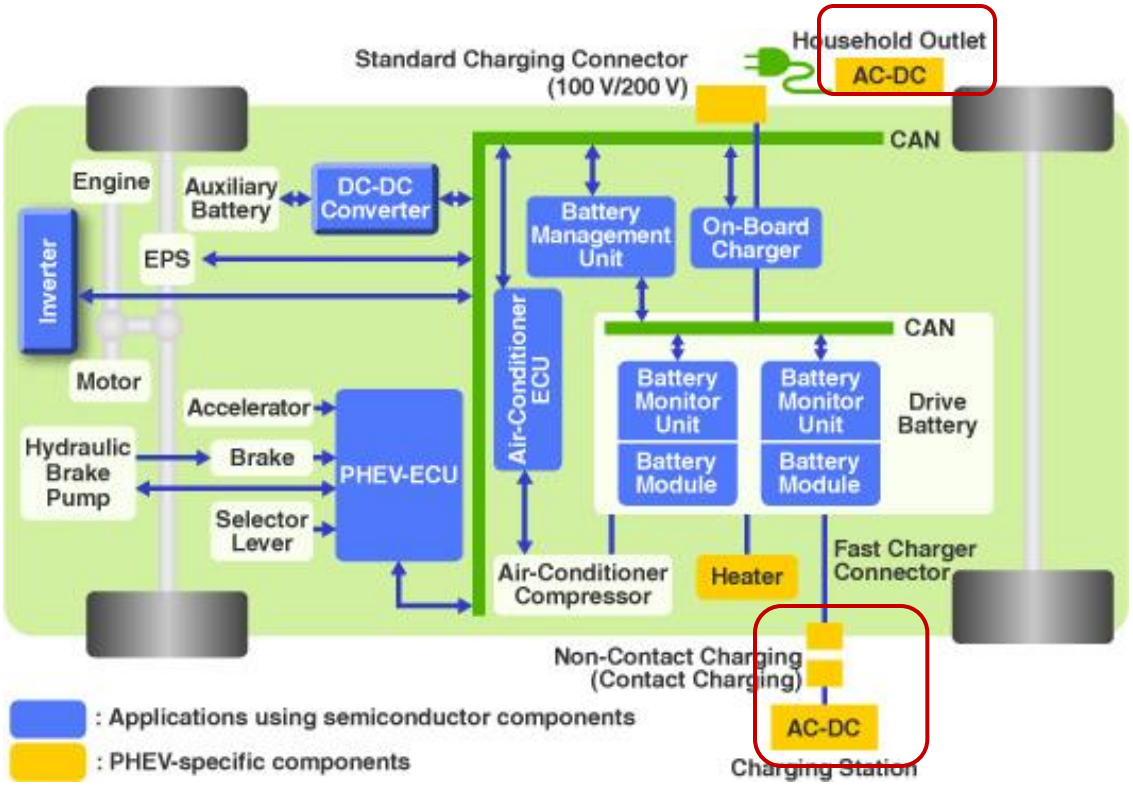
PFC Volume



Rectifier with power factor correction (PFC), also known as PFC rectifier, is also bulky, often, by far the largest element

PFC in Hybrid and Plug-In Hybrid Electric Vehicles (PHEV)

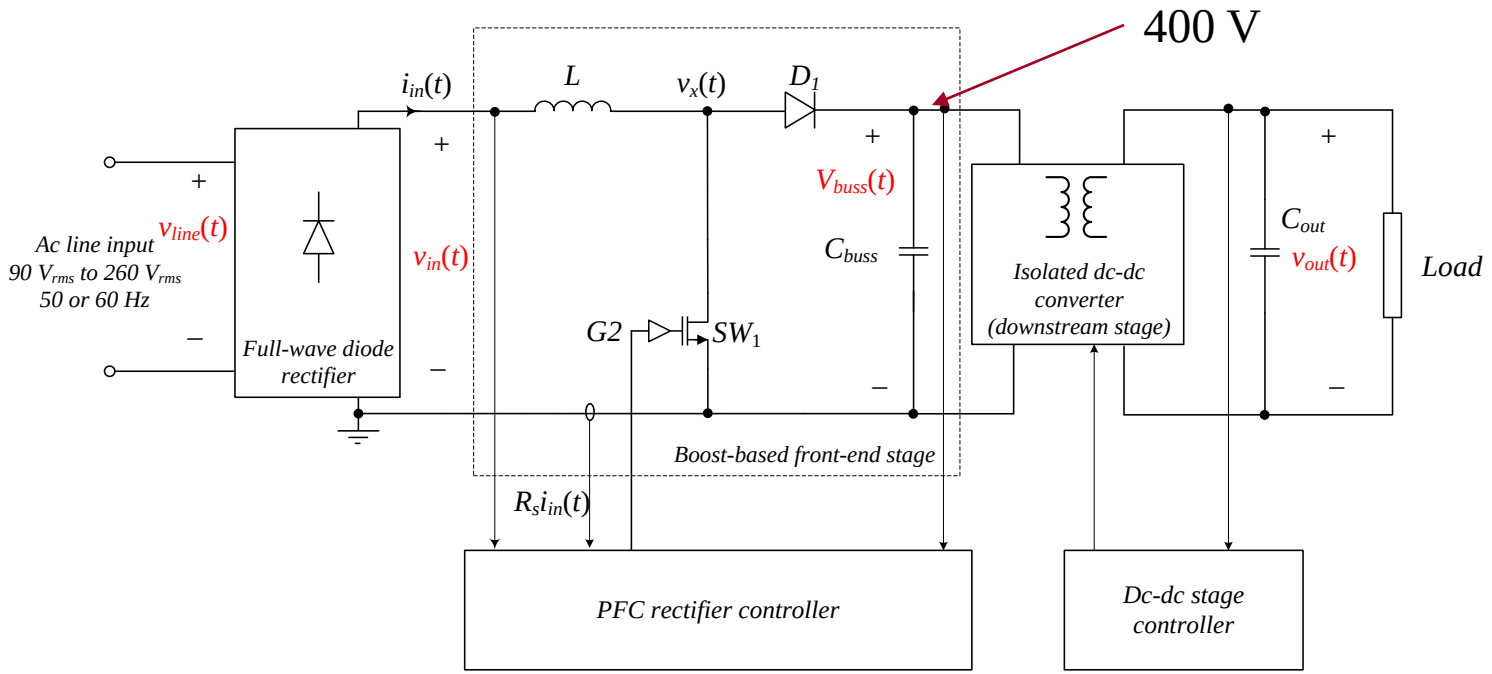
PFC



PFC

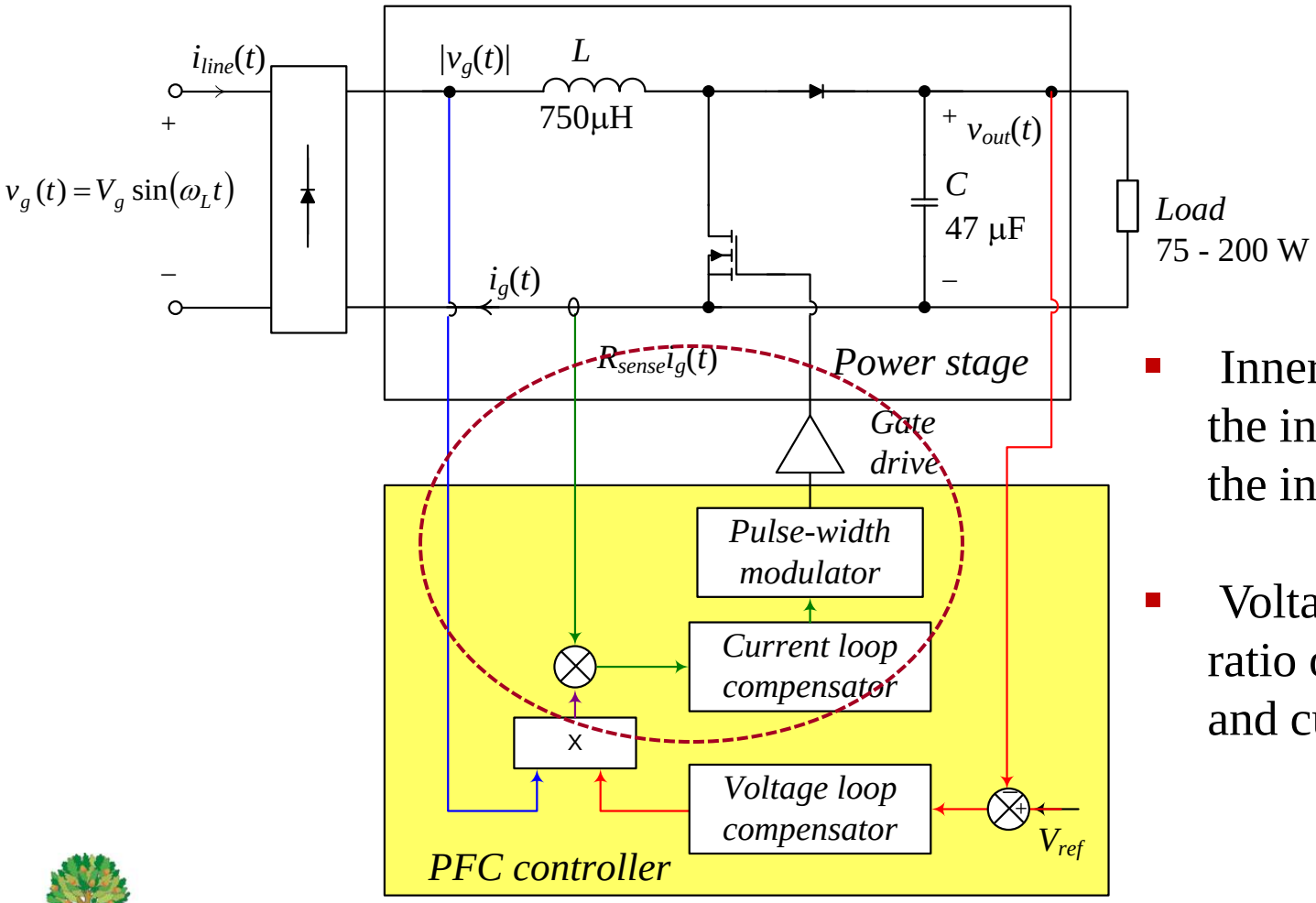
http://www.toshiba-components.com/automotive/evs.html

Conventional Boost Based PFC Rectifier + Downstream



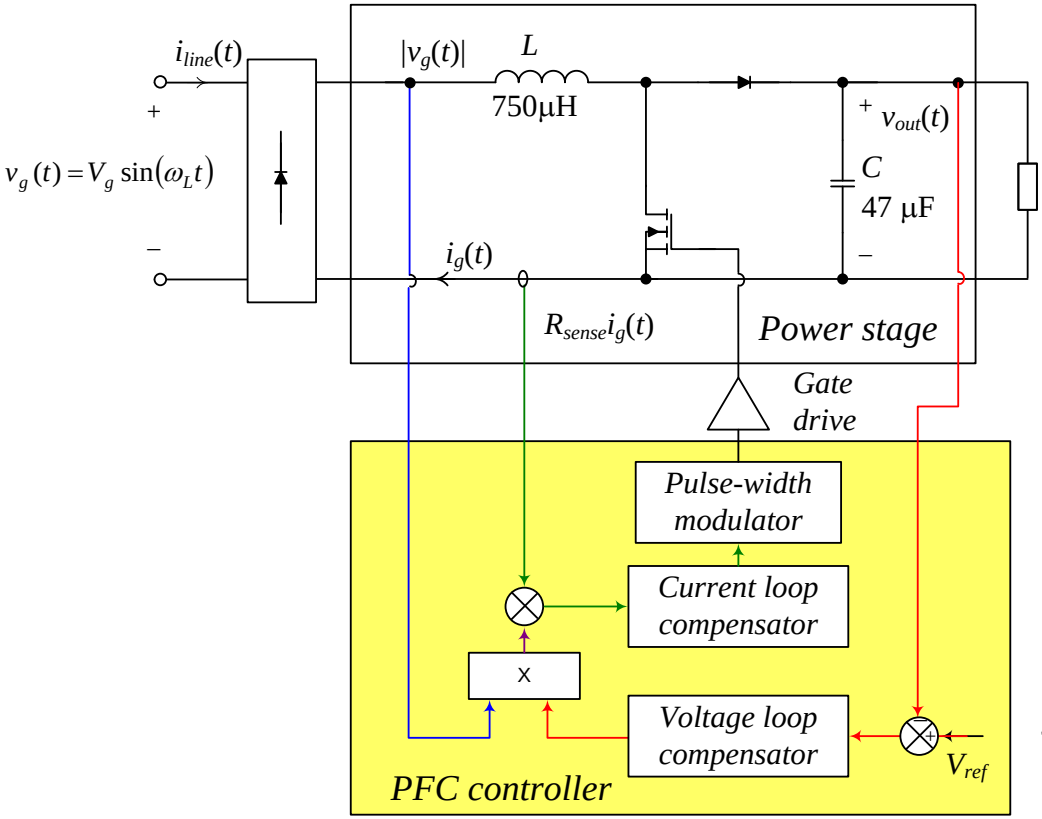
- Boost converter controlled by a current programmed mode
- Downstream stage usually steps down from 400 V to 48 V, 24 V or 12 V

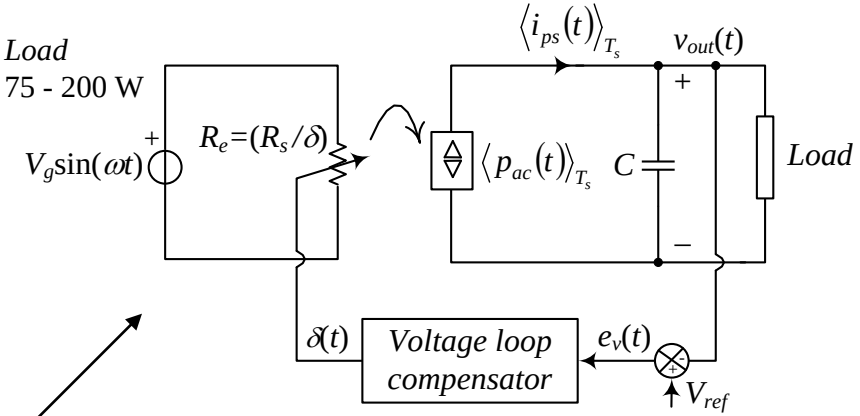
Conventional Boost Based PFC Rectifier



- Inner current loop forces the input current to follow the input voltage waveform
- Voltage loop controls the ratio of the input voltage and current

Conventional Boost Based PFC – Low Bandwidth V. Loop



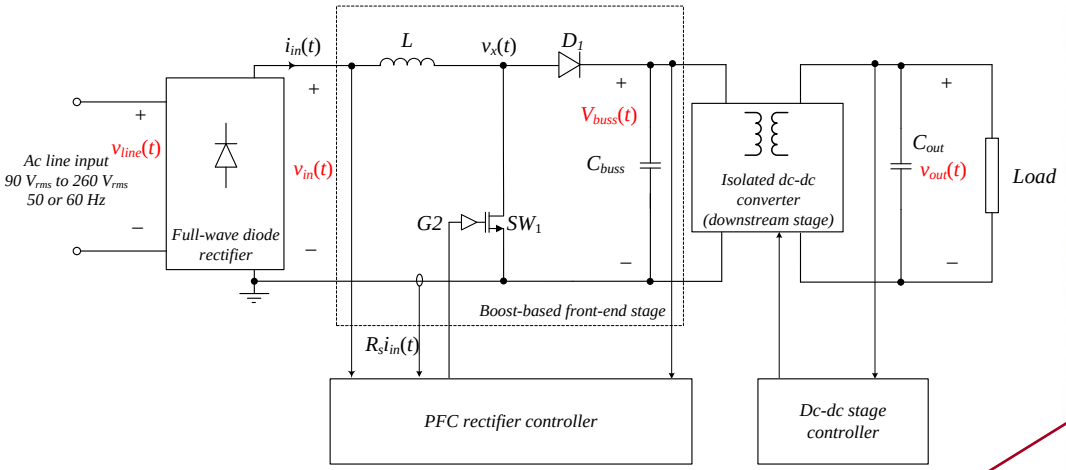


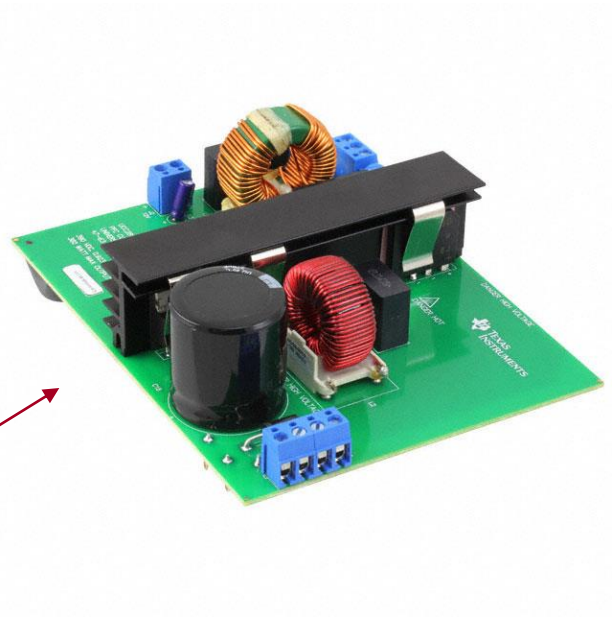
Average model

$$\langle p_{ac}(t) \rangle_{T_s} = \frac{V_g^2 \sin^2(\omega_L t)}{R_e} = \frac{V_g^2}{2R_e}(1 - \cos(2\omega_L t))$$

The voltage loop must not attempt to eliminate the output capacitor ripple through Re variations. Hence, it is usually designed to be very slow. We have a bulky high voltage cap.

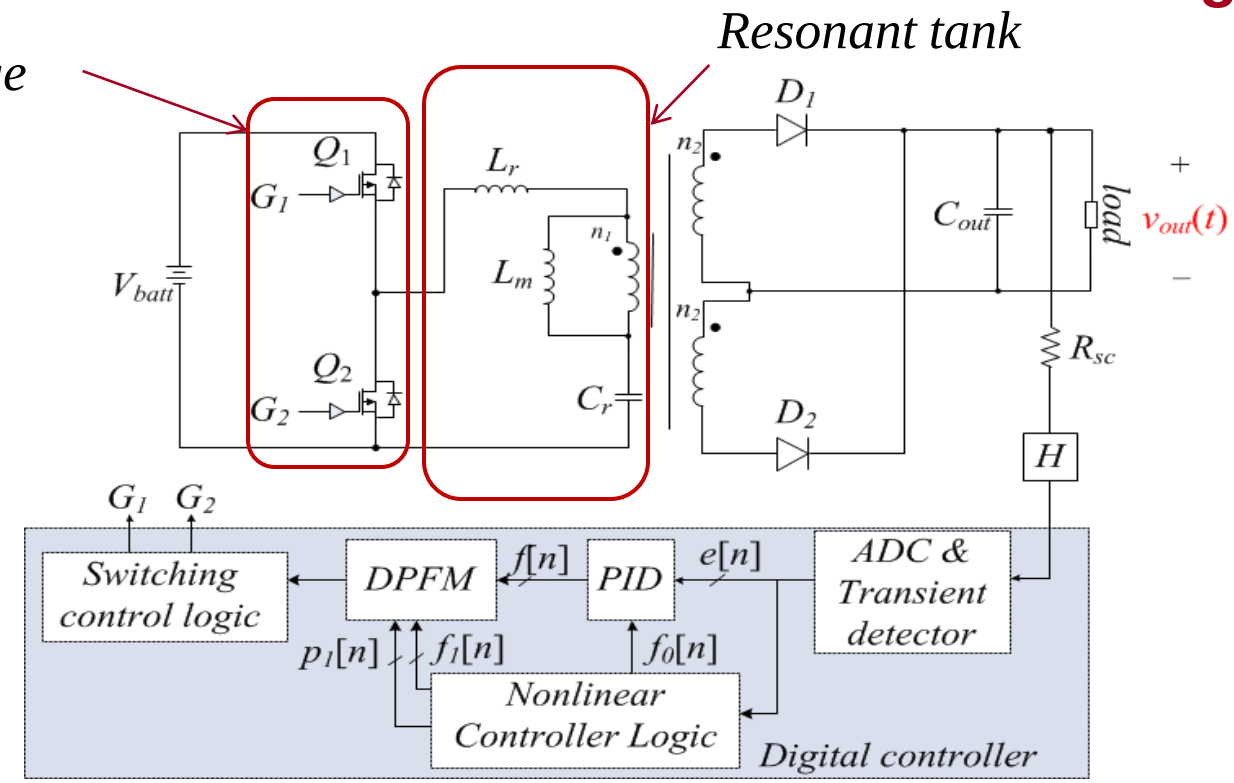
Conventional Boost Based PFC Rectifier





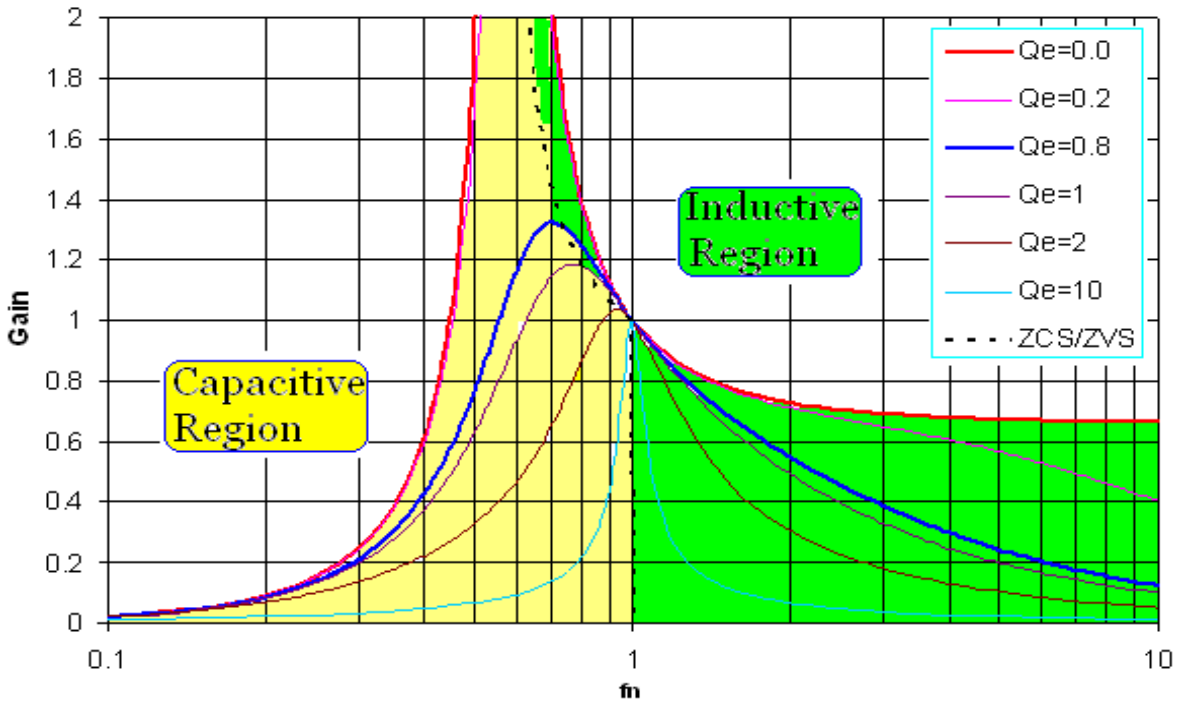
- Very large boost inductor due to a large voltage swing (400 V)
- Bulky heat sink to cool down the switch (and diode)

LLC Resonant Converter as the Downstream Stage



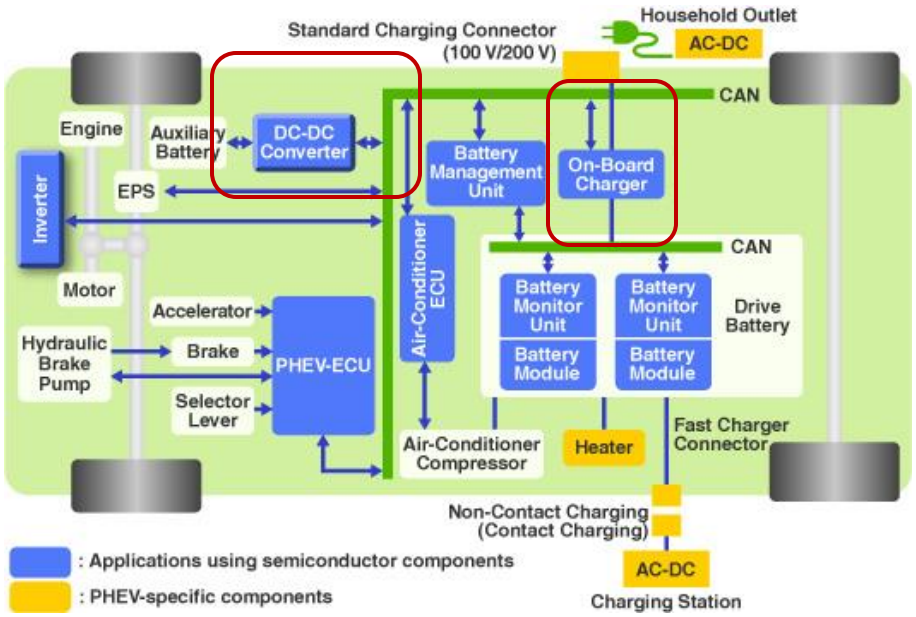
- Lr, Lm and Cr form a resonant circuit
- The control is performed by regulating frequency of the half bridge

LLC Resonant Converter as the Downstream Stage

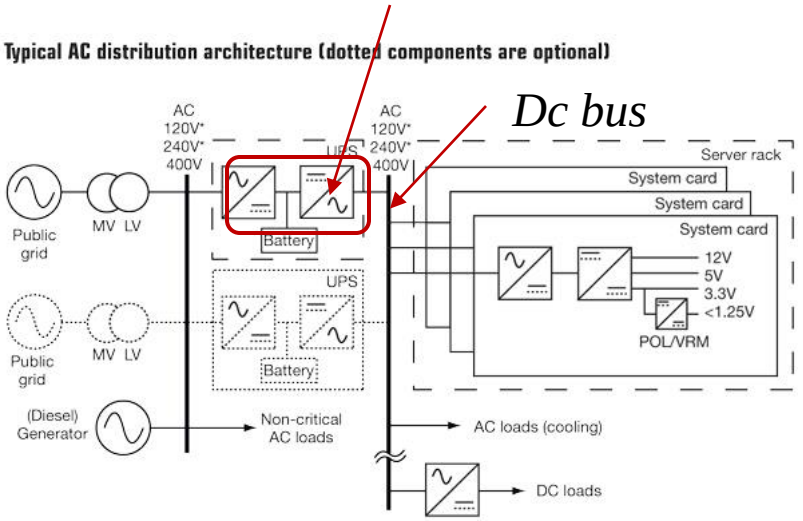


- The gain of resonant circuit defines conversion ratio
- The input of the resonant circuit can behave as an inductor or capacitor
- Due to slow regulation the output capacitor is usually very large

Dual-Active Bridge (DAB) as a Bidirectional Stage



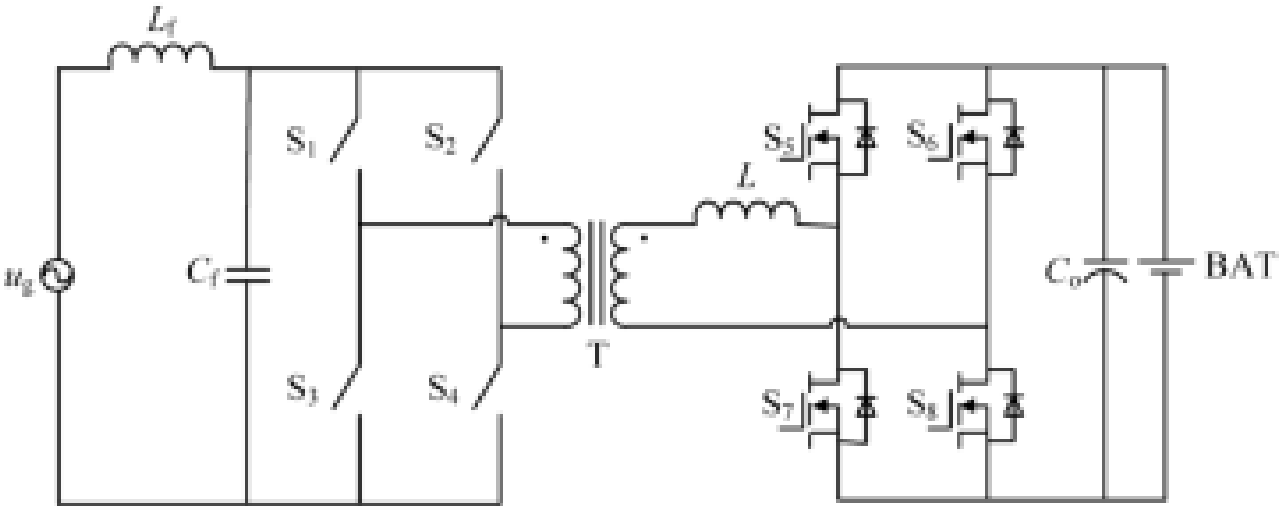
Bidirectional dc-dc converters also frequently used



http://powerelectronics.com

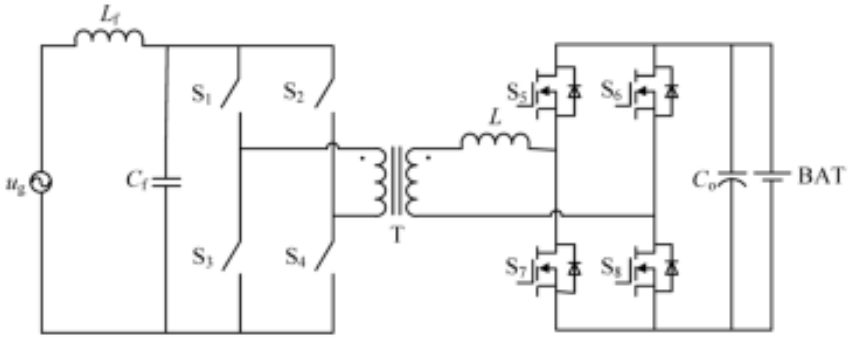
- Dual active bridge as the most common configuration

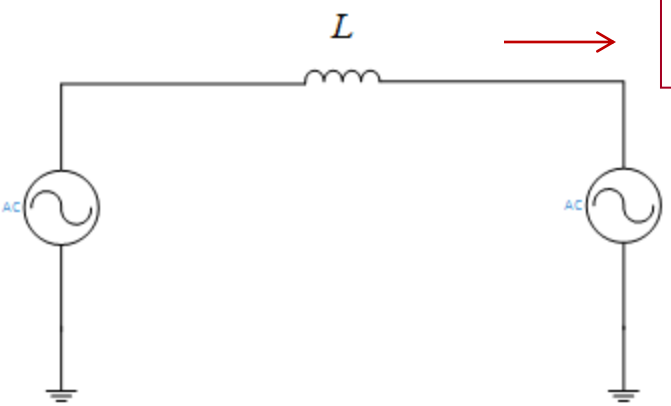
Dual-Active Bridge (DAB) as a Bidirectional Converter



- Can operate as a bidirectional ac-dc or dc-dc converter

Dual-Active Bridge (DAB) as a Bidirectional Converter





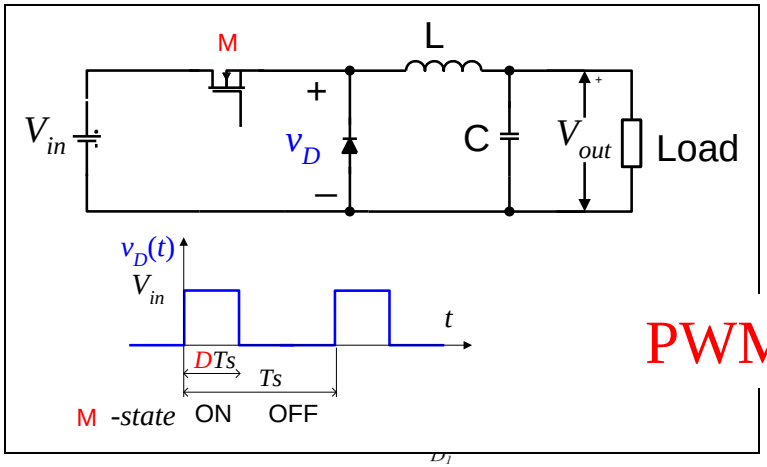
$$P = \frac{V_1 V_2}{2\omega L}\sin(\delta)$$

$$v_1(t) = V_1 \sin(\omega t)$$

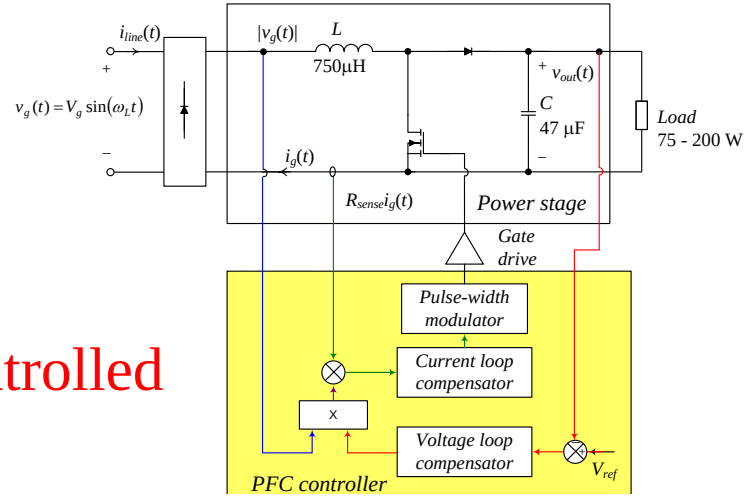
$$v_2(t) = V_2 \sin(\omega t + \delta)$$

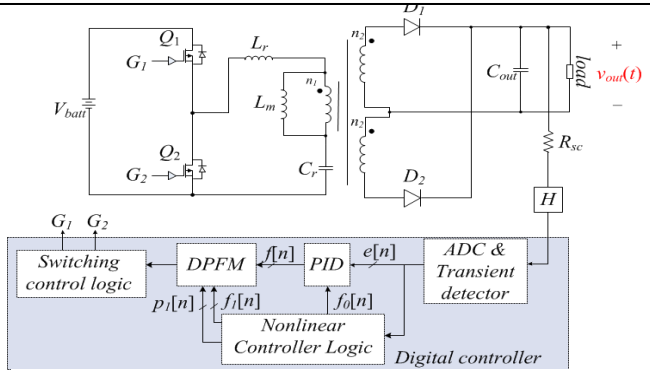
- Power can be regulated through phase modulation (PM) between two bridges and/or through frequency regulation

Applications/Topologies to be Analyzed

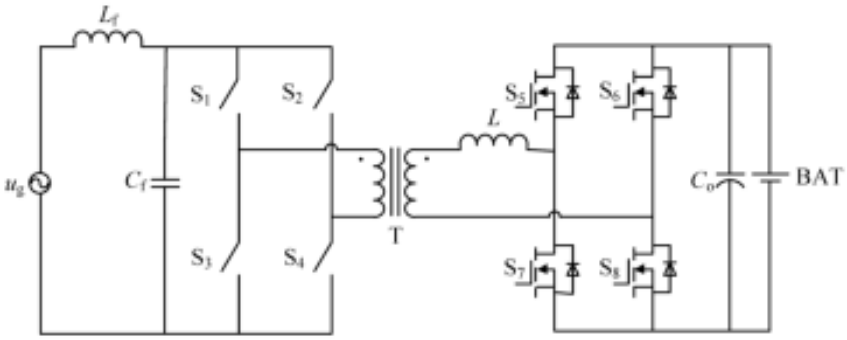


PWM controlled





Frequency controlled

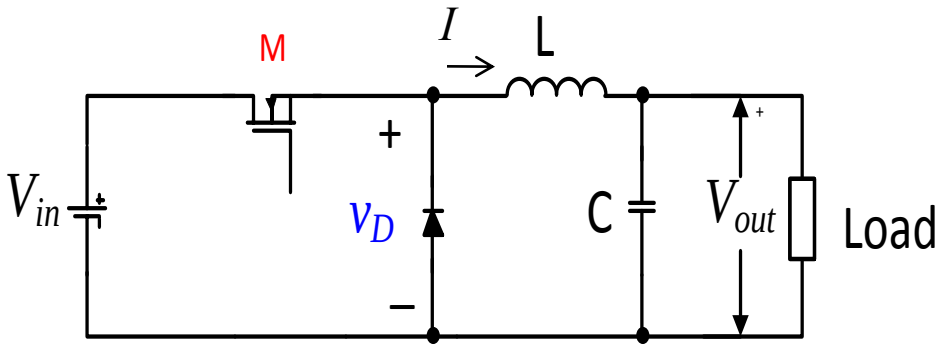


Frequency/ PM controlled

- Throughout the seminar these 4 classes of converters will be primarily analyzed (principles can be extended to other topologies/classes)

Passive Components Volume & Fundamental Volume Reduction Principles

Passive Components Volume & Fundamental Volume Reduction Principles



$$Volume\_C \approx k_1\left(W_{cap}\right) = k_1\left(\frac{1}{2}CV^2\right)$$

$$Volume\_L \approx k_2\left(W_{inductor}\right) = k_2\left(\frac{1}{2}LI^2\right)$$

- Volume of reactive components is proportional to their energy storage capacity

Volume Reduction Principle

All of the following volume reduction methods that will be presented here are centered around reduction of the energy storage requirements

$$Volume\_C \approx k_1\left(W_{cap}\right) = k_1\left(\frac{1}{2}CV^2\right)$$

$$Volume\_L \approx k_2\left(W_{inductor}\right) = k_2\left(\frac{1}{2}LI^2\right)$$

Since in the applications of interest most often: $k_1 << k_2$, i.e. the energy storage capacity per unit volume of the capacitors is larger than that of the inductors, we will be looking at an increased use of the capacitive energy transfer/conversion.

Side benefits (byproducts): Reduction of voltage/current stress of the components allowing for power processing efficiency improvements and cost-effective implementation .

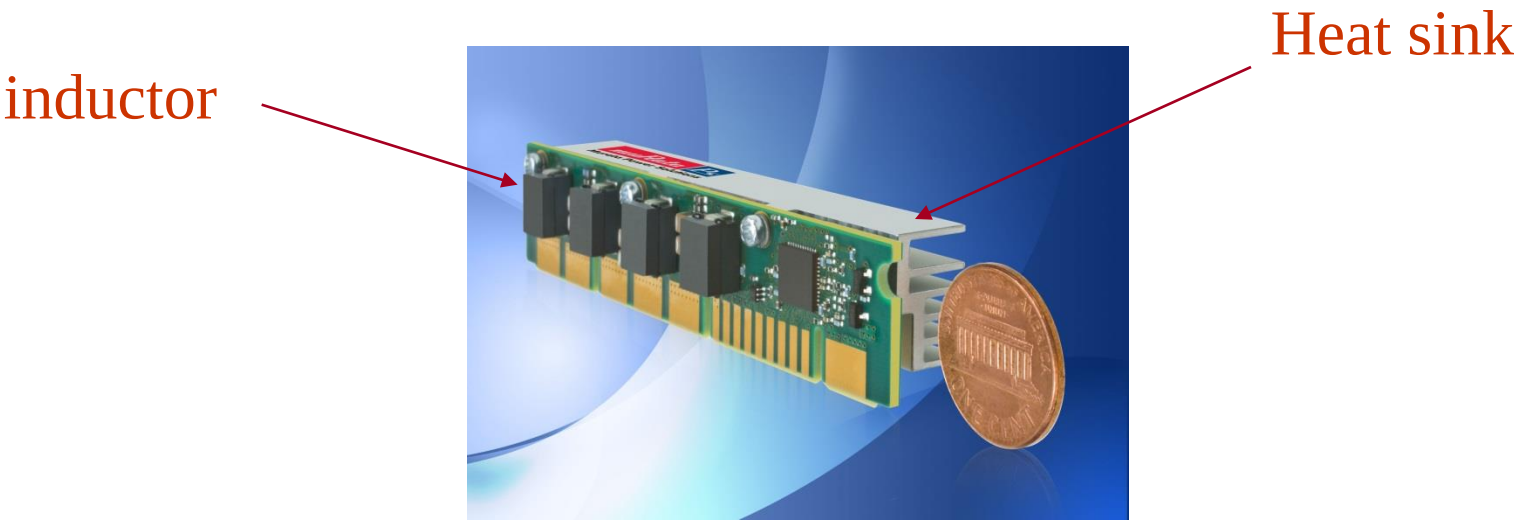
- Potential for operation at higher switching frequencies

Volume Reduction

Side benefits (byproducts): Reduction of voltage/current stress of the components allowing for power processing efficiency improvements and cost-effective implementation .

Drawbacks/Challenges: In some applications the capacitors have lower reliability and the complexity of topologies/control method significantly increases

Volume Reduction vs. Efficiency (Bulky Components)



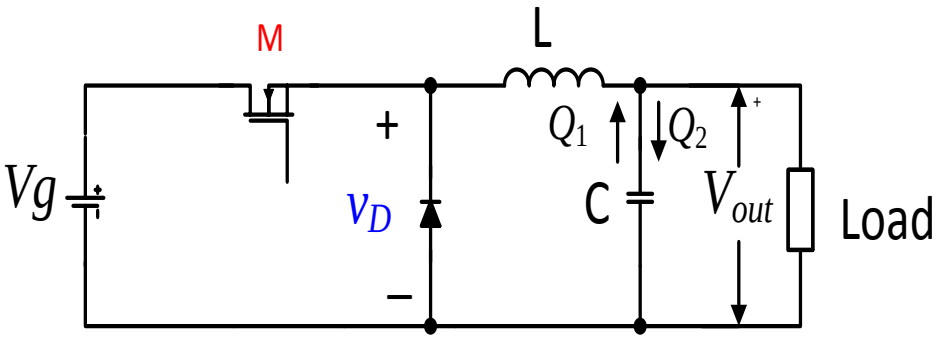
http://www.murata-ps.com/en/news/new-products/214

- Volume reduction without efficiency improvement can increase the size of the heat sink.

=> We also need to improve efficiency and/or reduce temperatures of hot spots (loss distribution)

Capacitor Volume Reduction Through Charge Swing Minimization - Basic Principles

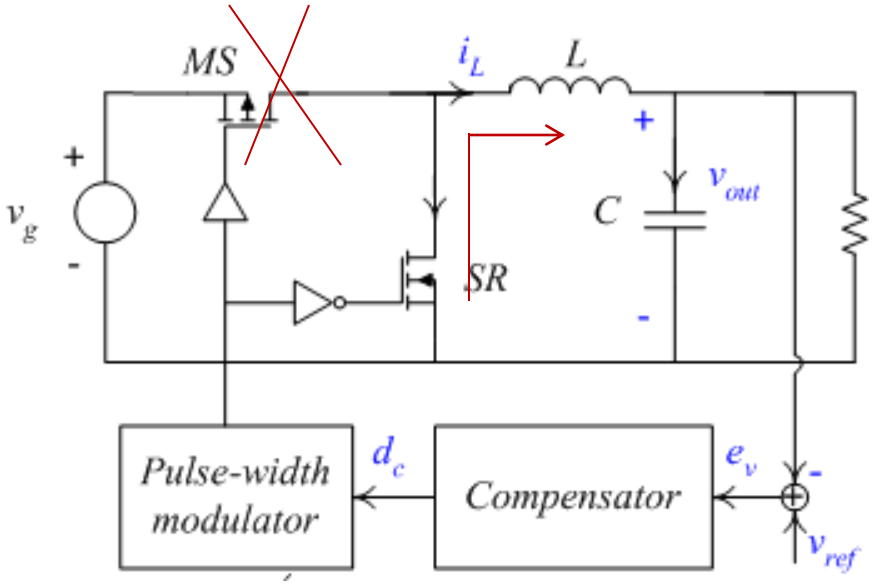
Capacitor Volume Reduction (Reduction of Supply Voltage)

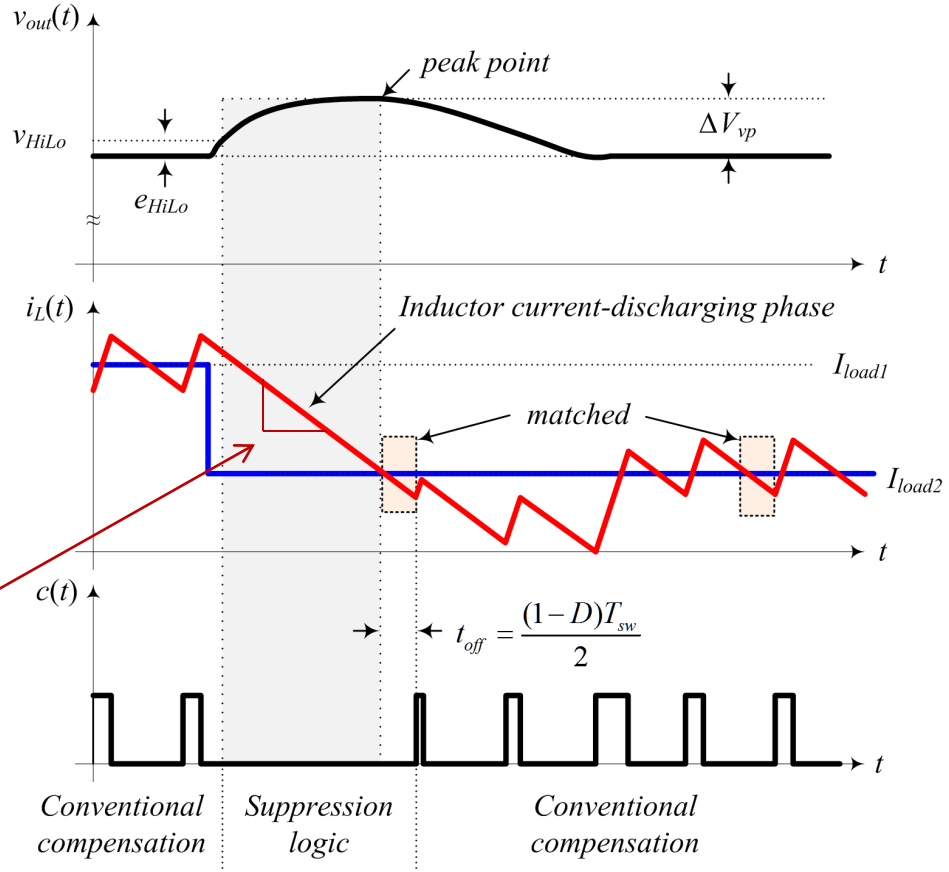


$$Volume\_C \approx k_1\left(\frac{1}{2}CV_{out}^{\ 2}\right)$$

- Trend of reducing supply voltages in PoL (V_{out}) helps us but, at the same time, increasing power requirements create challenges
  - Increased current and conduction losses (i.e. larger inductor)
  - Reduced slew rate and slower transient response for heavy-to-light load transients

Capacitor Volume Reduction (Reduction of Supply Voltage)

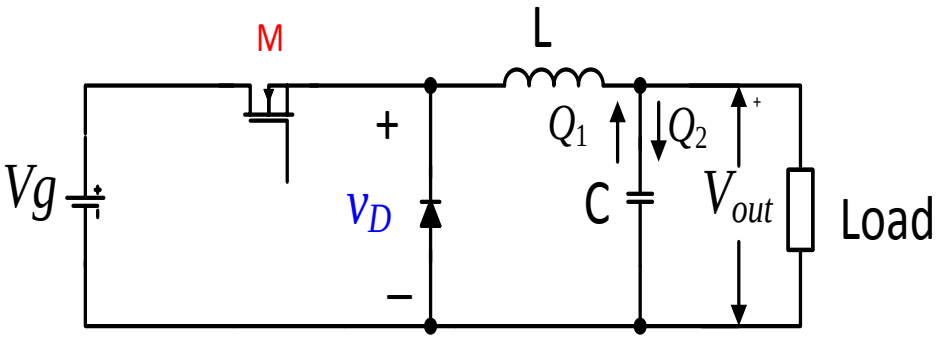




$$Slew\_rate \cong \frac{V_{out}}{L}$$

- Heavy-to-light load transient and the influence of the inductor slew rate (lower output voltage)

Capacitor Volume Reduction – Basic Principles

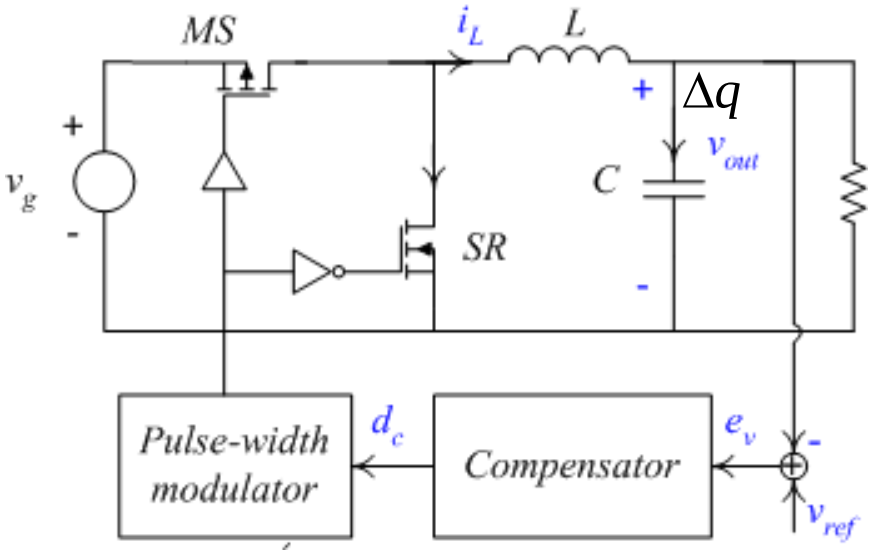


$$Volume\_C \approx k_1\left(\frac{1}{2}CV_{out}^{\ 2}\right)$$

- C reduction through minimization of the capacitor charge swing (variation) => reduction of the capacitance value

We will focus on this principle

Sizing of the Output Capacitor and Charge Swing



Capacitor sizing criteria (based on maximum allowable voltage variations), i.e. charge swing:

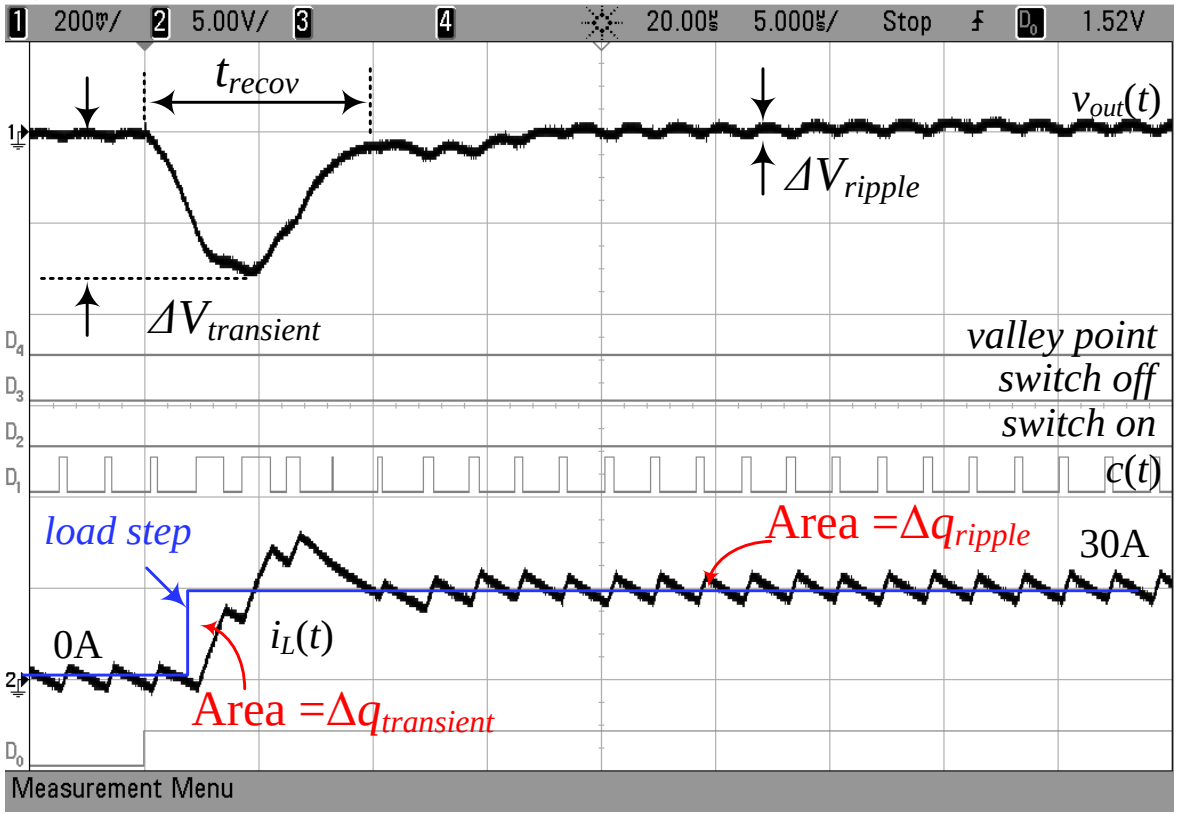
$$\Delta q = C\Delta V$$

$$\Delta v_{out} = \frac{\Delta q_{ripple} + \Delta q_{transient}}{C}$$

In point-of-load converters (and number of other applications) the ripple component of the charge swing Δq_{ripple} is often much smaller than that of the transient component $\Delta q_{transient}$.

=> *The output capacitors size is in most cases determined by the dynamic performance of the controller*

Sizing of the Output Capacitor and Charge Swing



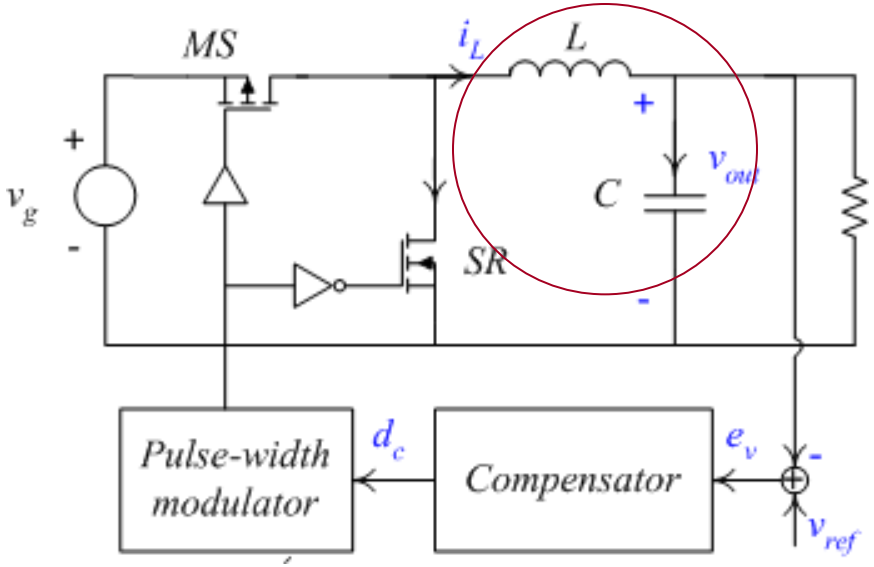
Charge swing:

$$\Delta q = C\Delta V$$

The faster the controller brings inductor current to the new load value the less charge Δq_{trans} capacitor needs to give and, therefore, for the same output voltage deviation $\Delta V_{transient}$ we can use a smaller capacitor.

Conventional Methods for Charge Swing Reduction

- Operation at higher switching frequencies for reducing $\Delta q_{tripple}$ (also reduces the inductor value)
- Fast dynamic response of the controller for reducing $\Delta q_{transient}$

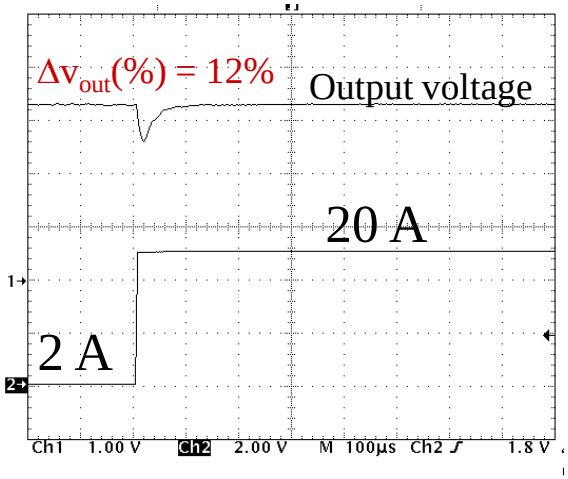


Load current

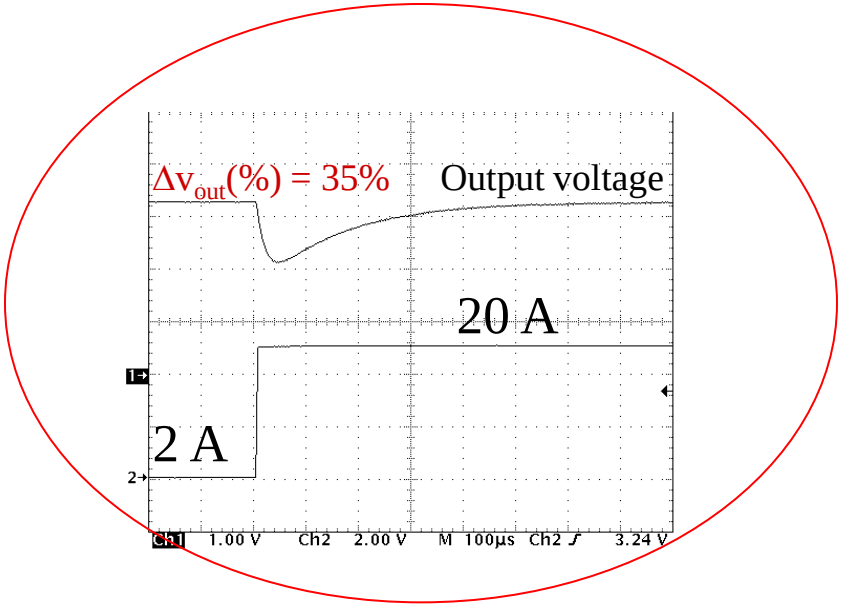
A fast response controller operating at a high switching frequency can drastically reduce the volume of the SMPS.

Influence of the Controller on the Size of the Output Capacitor

Due to slower dynamic response, i.e. larger filter requirement..



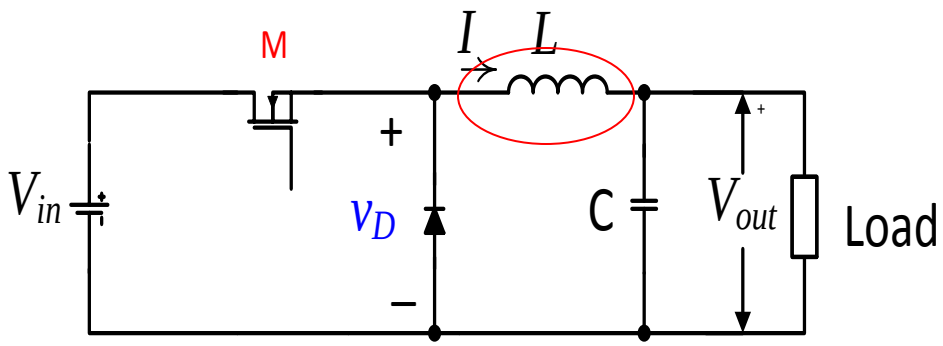
Faster controller



Slower controller requires 3 times larger output capacitor to achieve the same output voltage deviation as the faster one

Inductor Volume Reduction Through Flux Linkage Minimization - Basic Principles

Inductor Volume Reduction – Basic Principles



$$Volume\_L \approx k_2\left(\frac{1}{2}LI^2\right)$$

k_2- *depends on the type of inductor*

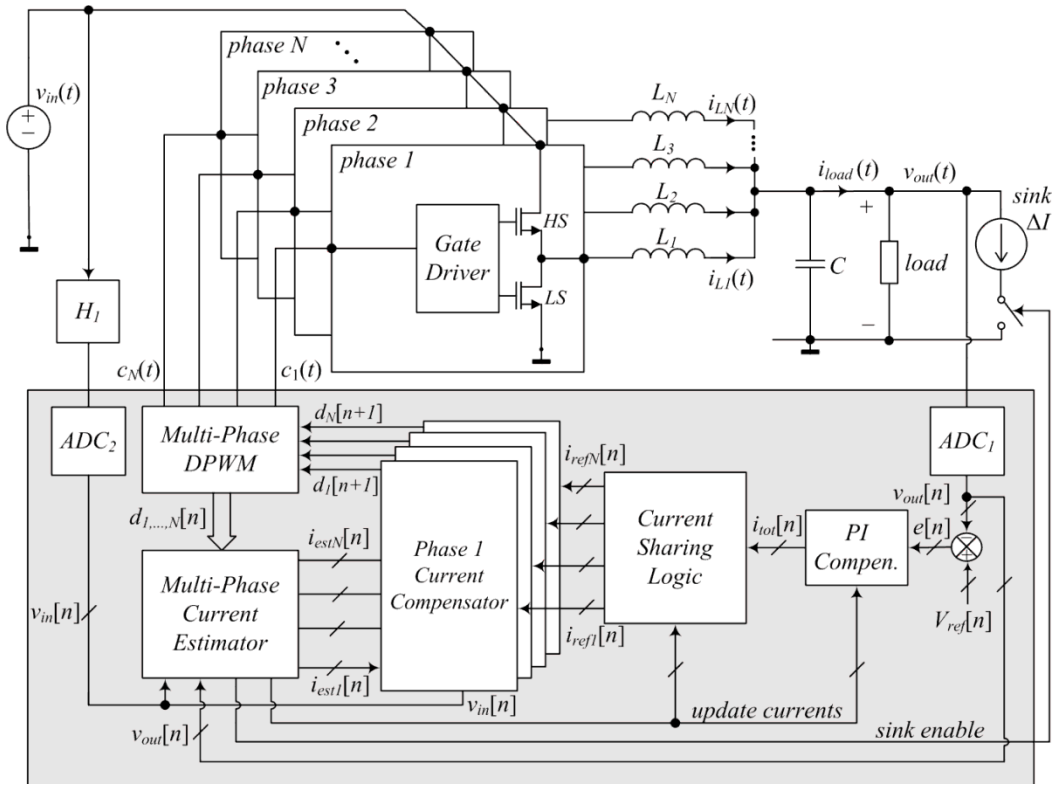
Principles for the inductor volume reduction/elimination :

- *Current division (reduction of the inductor current), will see that it does not actually reduce the output filter inductor (common misconception)*

- *Inductor volt-second swing reduction (novel converter topologies)*

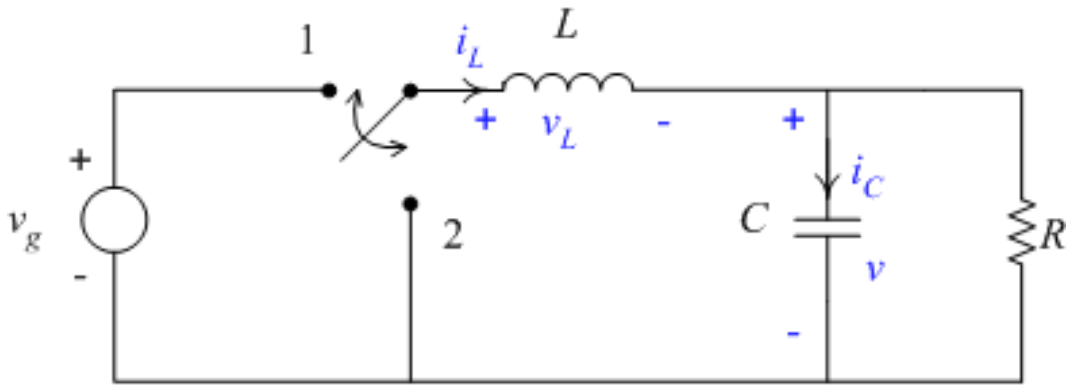
Main focus

Current Sharing – Basic Principle

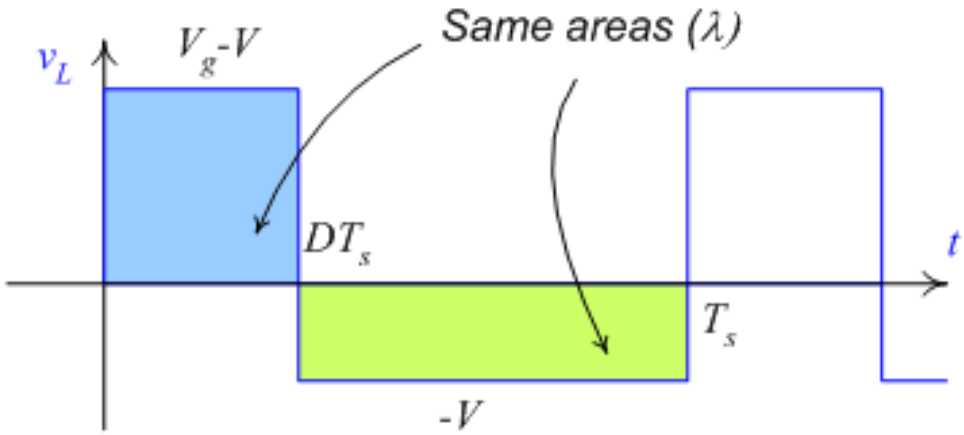


- Each phase conducts 1/N of the current of the original converter

Current Ripple

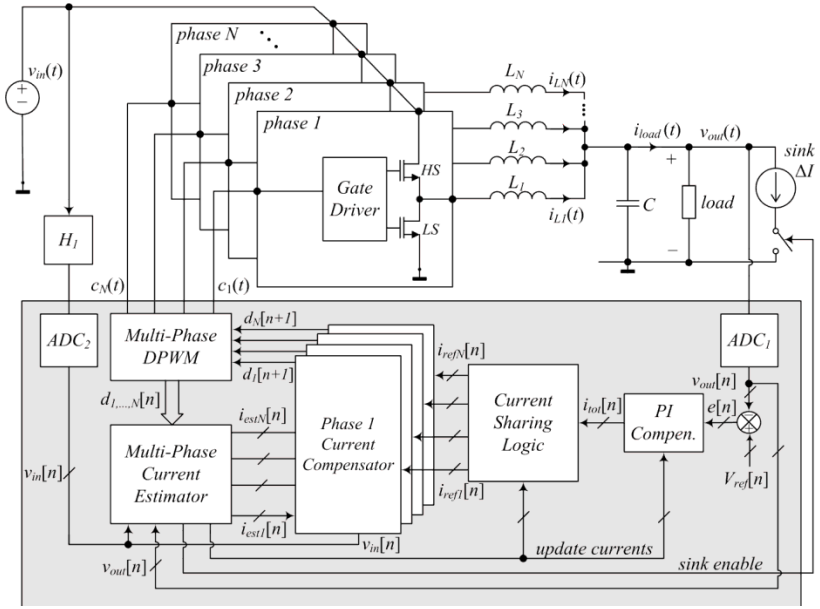


$$\Delta I_L = \frac{(V_g - V)DT_s}{L} = \frac{V(1-D)T_s}{L}$$



Current ripple influences the rms current (conduction) losses and output capacitor ripple.

Inductor Volume Reduction – Basic Principles

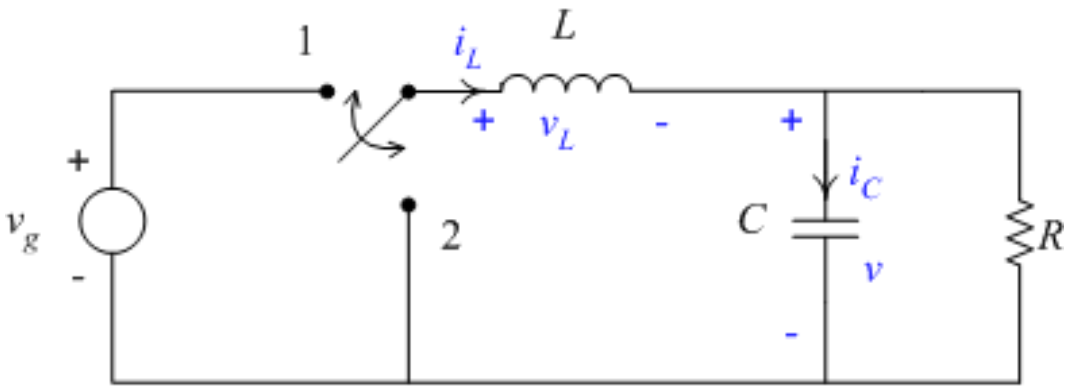


$$Volume\_L \approx k_2 N \left(\frac{1}{2}(NL) \left(\frac{I}{N} \right)^2 \right)$$

The same total inductor volume as for the original case

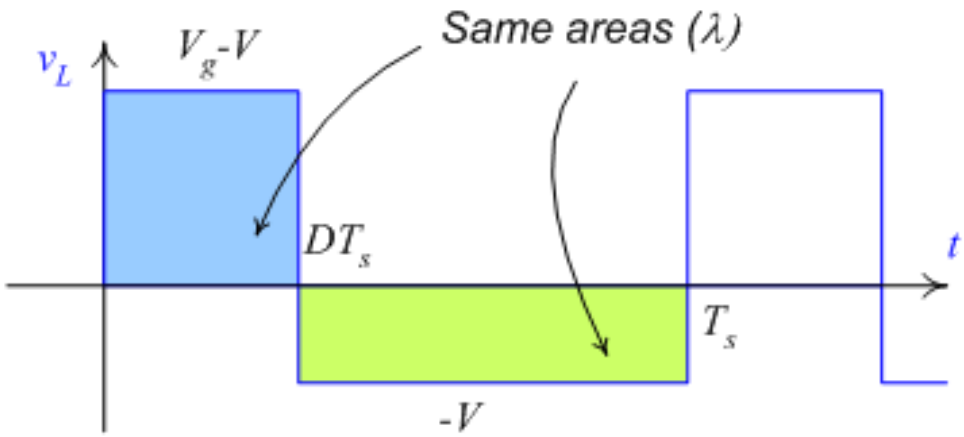
- To have the same total ripple the inductor in each phase needs to be N times larger
- However, the input filter is reduced significantly

Flux Linkage Minimization



$$\Delta I_L = \frac{(V_g - V)DT_s}{L} = \frac{V(1-D)T_s}{L}$$

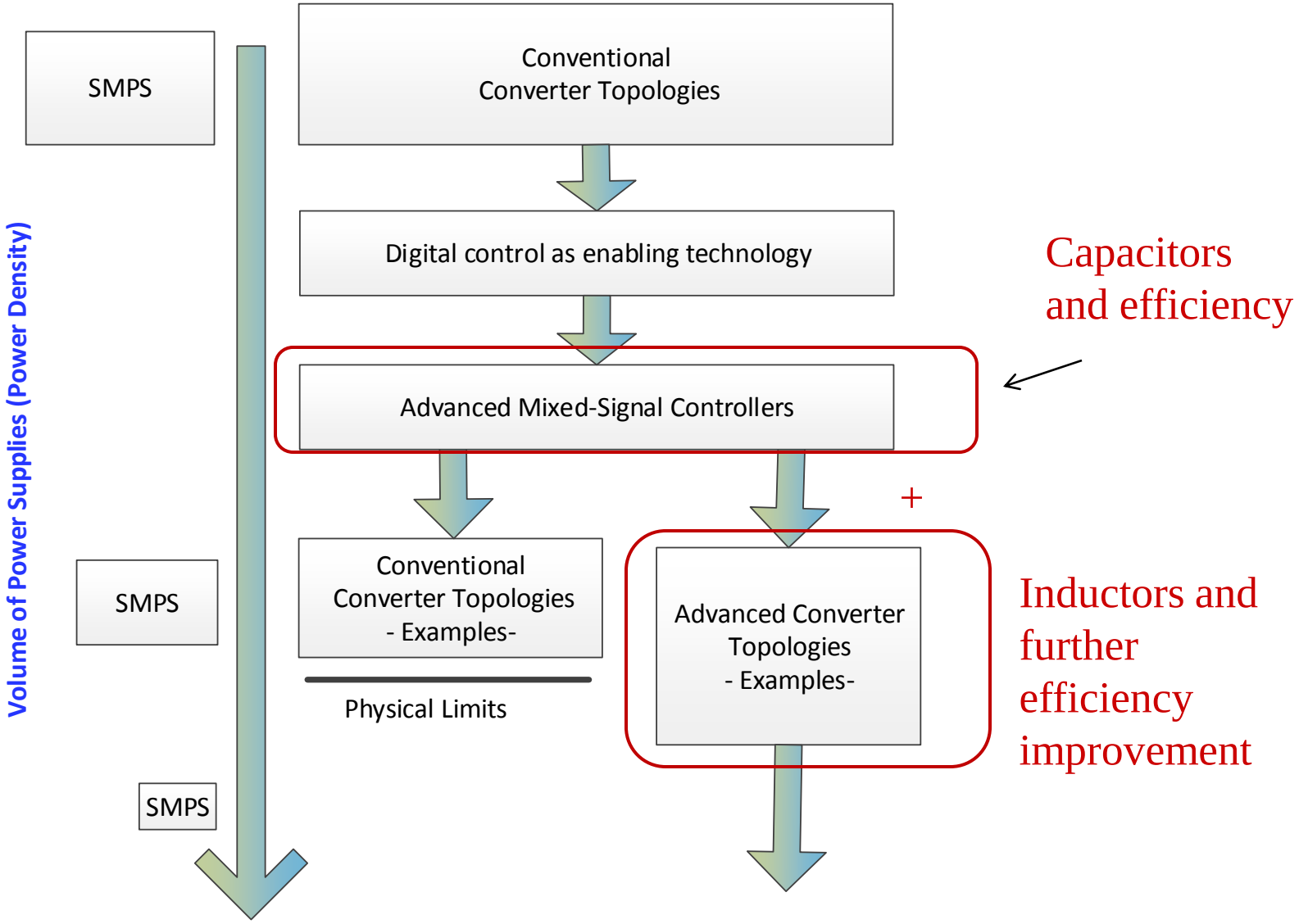
To reduce the inductor we can reduce the flux linkage λ



- Conventional solutions try to increase the switching frequency (reduce *Ts*)
- As we will see λ can be also reduced by changing converter topologies

focus

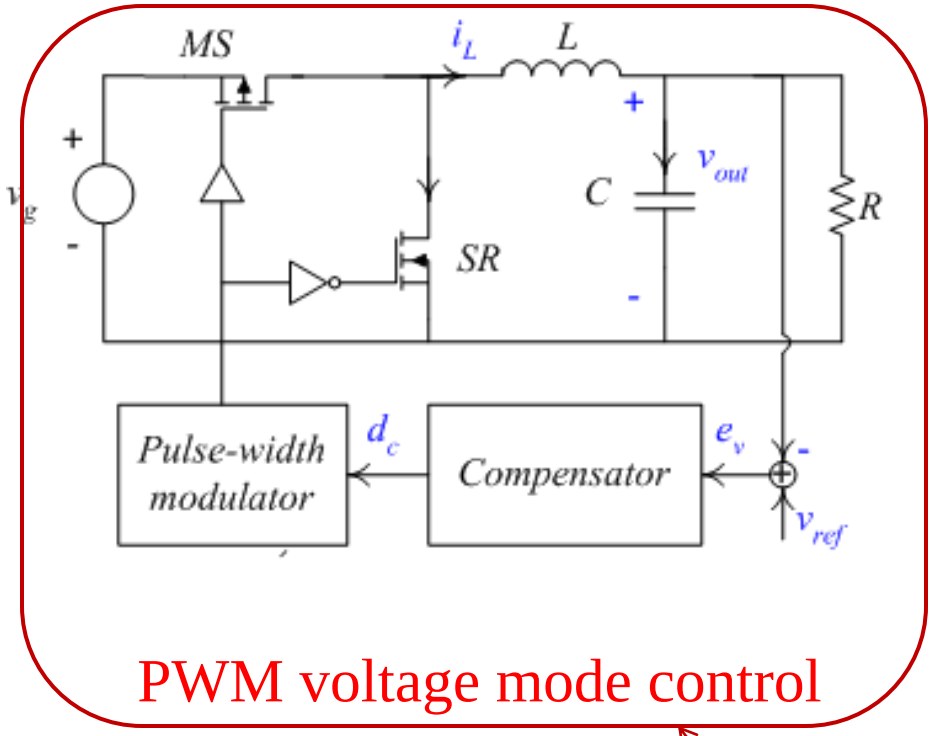
Volume Reductions Addressed Through Seminar



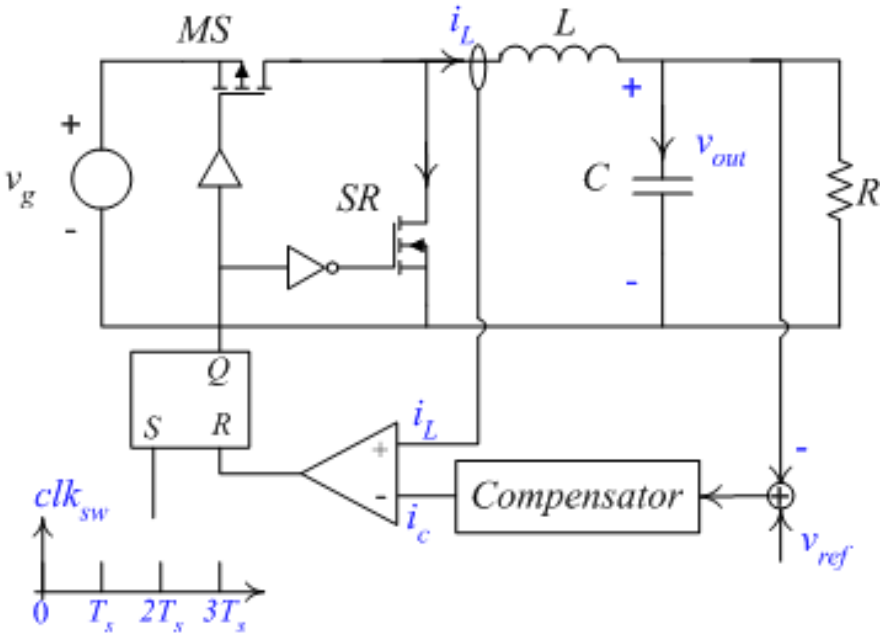
Part II

Controller Design: Review of Conventional Analog Controller Design, Analog Implementation, Digital Controller Design and Digital Implementation

Review of Analog Controller Implementation



PWM voltage mode control



Current programmed mode

Voltage mode control taken as an example, the principles can be extended to other control methods. In fact the other methods often result in simpler system dynamics.

Controller Design - Overview

- *Dc and ac equivalent circuit modeling of converters*
- *Compensator design and analog controller implementation*
- *Modification of the model to accommodate digital controller implementation*
- *Limit cycling and other quantization effects*
- *Digital compensator design and practical implementation*

DC and Small-Signal ac Modeling, Converter Transfer Functions

Review of Modeling Steps

- *Converter in equilibrium and average values*
- *The small-ripple approximation, inductor volt-second balance, and capacitor-charge balance (conversion ratio and average currents)*
- *Dc equivalent circuits and modeling of losses*
- *Ac equivalent circuit modeling and converter transfer functions, modeling of basic functional blocks*
- *Compensator design and analog controller implementation*

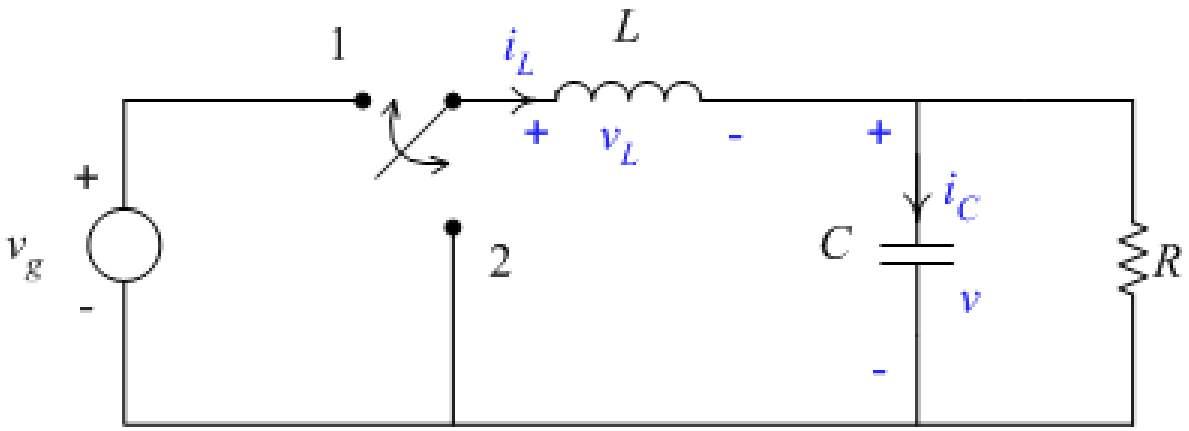
DC Modeling – Converters in Equilibrium

Three basic principles of the SMPS analysis

1. The small-ripple approximation
2. Inductor volt-second balance
3. Capacitor-charge balance

These three principles are applicable for all converter topologies and used for both dc and ac analysis and modeling.

DC Modeling: Small-Ripple Approximation (SRA)



$0 < t \le DTs$ *"on state" the switch is in position 1*

$DTs < t \le Ts$ *"off state" the switch is in position 2*

$V = DVg$ ←——— Intuitively

We approximate

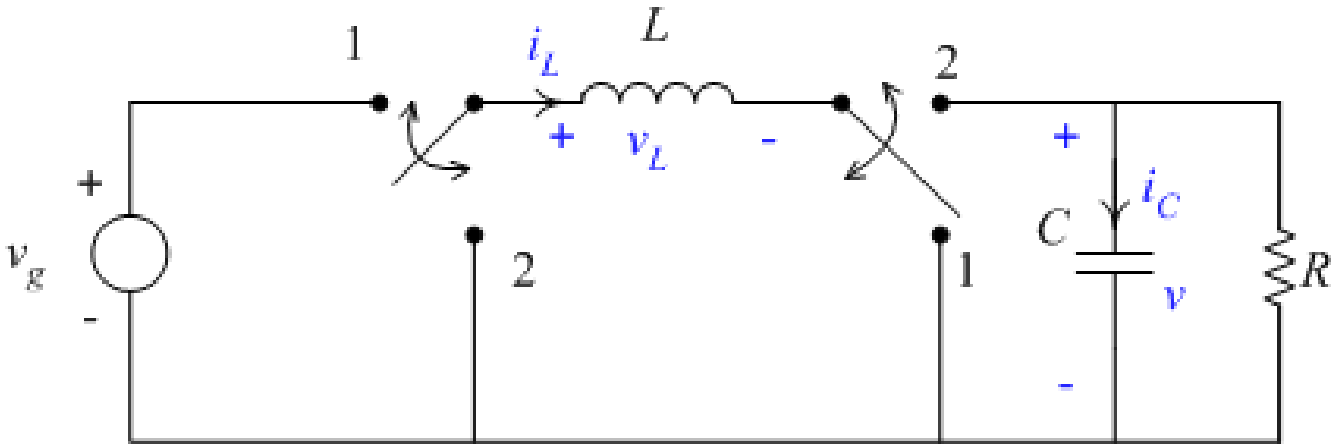
$$v(t) = V + v_{ripple} \approx V$$

The small-ripple approximation (SRA) !

D is duty ratio, $0 \le D \le 1$

$D' = 1 - D$

DC Modeling: Small-Ripple Approximation (SRA)

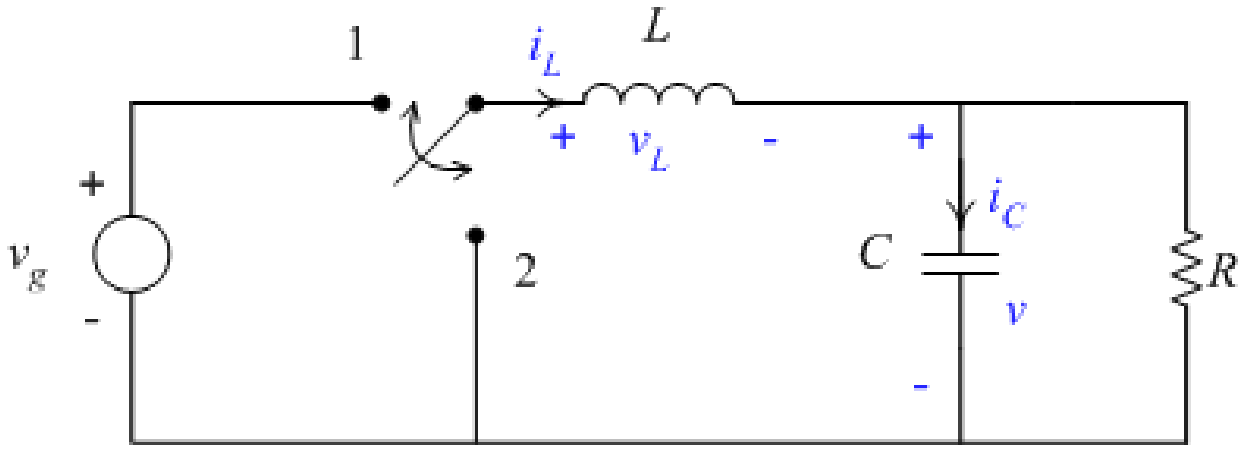


$0 < t \le DTs$ *"on state" the switches are in position 1*

$DTs < t \le Ts$ *"off state" the switches are in position 2*

$$V = f\{D, Vg\} = ?$$

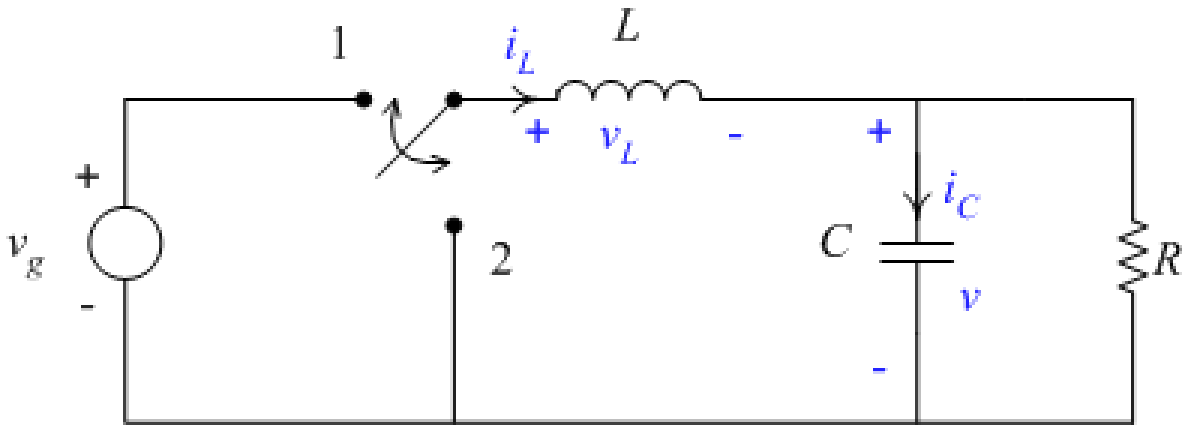
DC Modeling: Inductor Volt-Second Balance

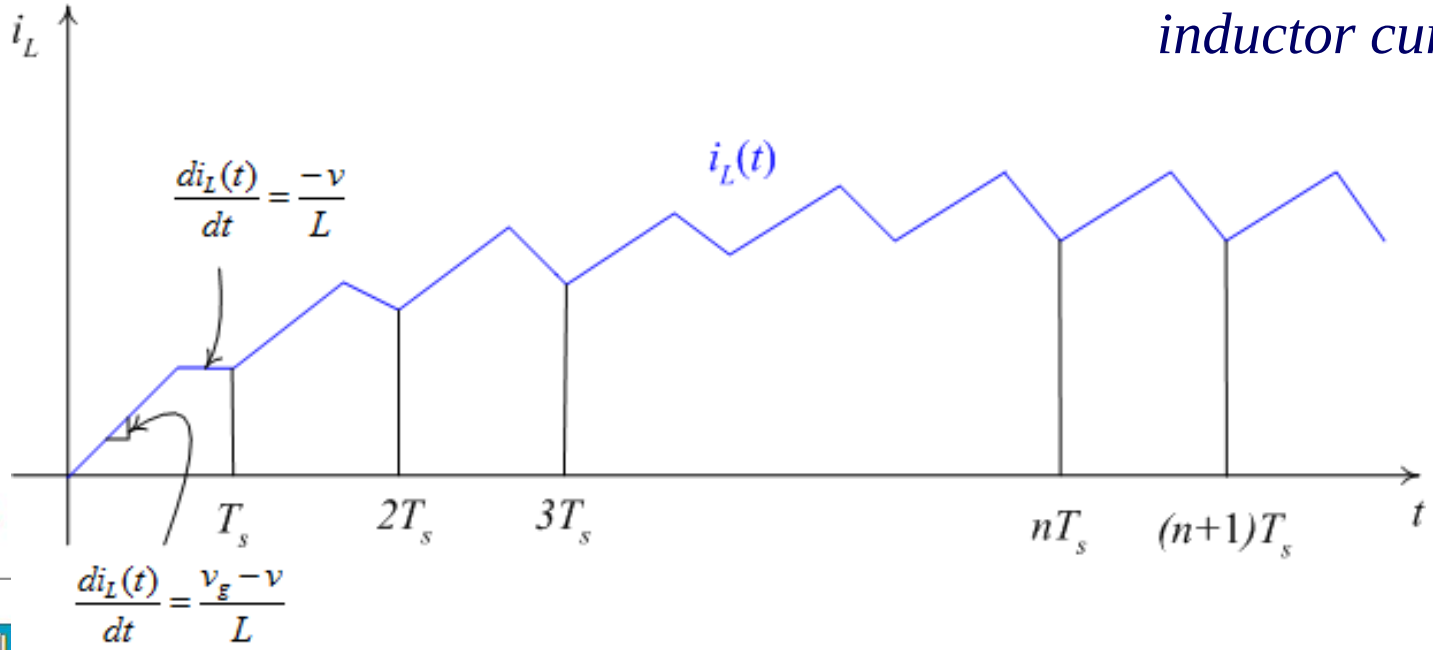


$0 < t \le DTs$ *"on state" the switch is in position 1* $v_L = v_g - v$

$DTs < t \le Ts$ *"off state" the switch is in position 2* $v_L = -v$

Inductor Volt-Second Balance: Initial Current Waveform





Equilibrium

$$i_L(nT_s) = i_L((n+1)T_s)$$

No net increase of the inductor current

Inductor Volt-Second Balance

$$i_L(nT_s) = i_L((n+1)T_s) \longrightarrow i_L((n+1)T_s) = \frac{1}{T_s}\int_{nTs}^{(n+1)Ts} v_L(t)dt + i_L(nTs)$$

$=0$

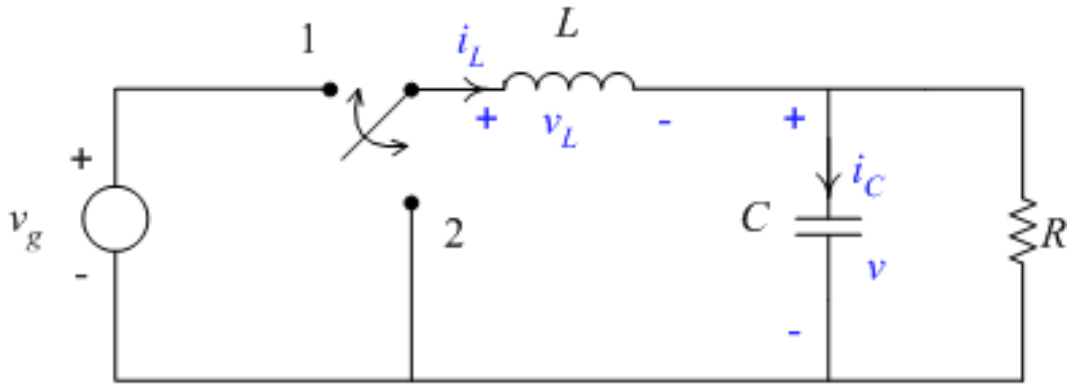
For already established equilibrium

$$\langle v_L(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{Ts} v_L(t)dt = 0$$

Inductor volt-second balance

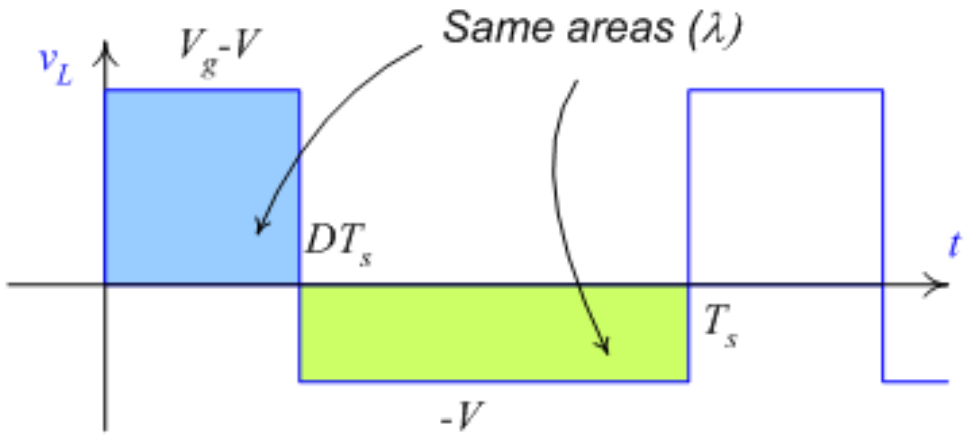
In steady-state the average value of the inductor voltage over one switching cycle is zero!

Combining SRA and Inductor Volt Second Balance



Small-ripple approximation

$$v(t) \approx V$$
$$v_g(t) \approx V_g$$



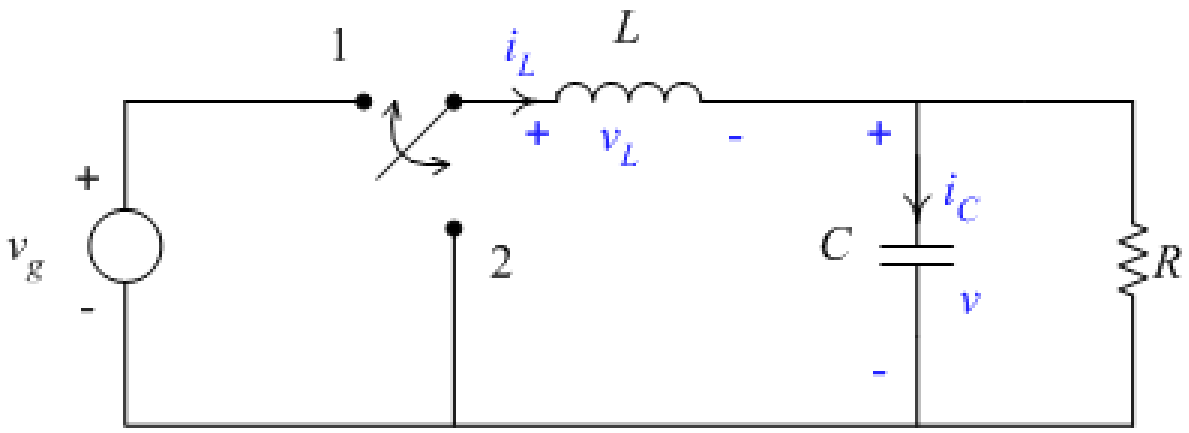
Inductor volt-second balance

$$\langle v_L(t) \rangle_{Ts} = \frac{1}{T_s} \int_0^{Ts} v_L(t)dt =$$
$$= D(V_g - V) - D'V = 0$$

$$\Rightarrow DV_g = V$$

By using SRA and volt-second balance conversion ratio of every converter can be found in minutes.

Capacitor Charge Balance



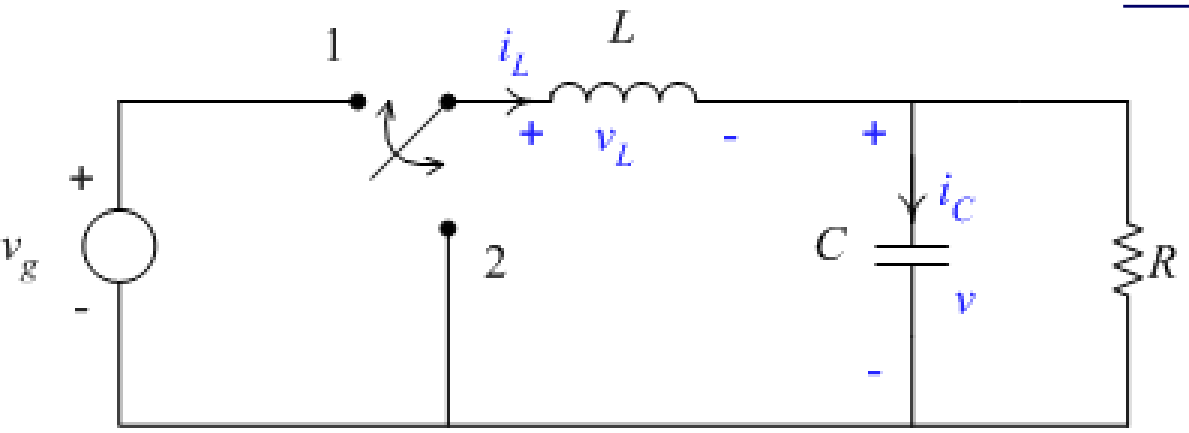
In equilibrium the output capacitor voltage is constant

$$\langle i_C(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{Ts} i_C(t)dt = 0$$

Capacitor –charge balance

In steady-state the average value of the capacitor current over one switching cycle is zero!

Combining Capacitor Charge Balance and SRA



Small-ripple approximation

$$0 < t \le DT_s$$

$$i_C(t) = i_L(t) - \frac{v}{R} \approx I_L - \frac{V}{R}$$

$$DT_s < t \le T_s$$

$$i_C(t) = i_L(t) - \frac{v}{R} \approx I_L - \frac{V}{R}$$

Capacitor –charge balance

$$\langle i_C(t) \rangle_{Ts} = \frac{1}{T_s} \int_0^{Ts} i_C(t)dt = D(I_L - V/R) + D'(I_L - V/R) = 0$$

$$\Rightarrow I_L = \frac{V}{R}$$

By combining SRA and capacitor-charge balance inductor currents of each converter can be found quickly.

General Algorithm for the Calculations of Conversion Ratio and Inductor Currents

1. *Arbitrary assign voltages to all capacitors and currents to inductors*

2. *Draw equivalent circuits for both portions of the switching interval:*

   - *Express inductor voltages in terms of the input and capacitor voltages*

   - *Express capacitor currents in terms of inductor currents and v/R, (or output currents)*

3. *Apply small-ripple approximation (SRA)*

$$v(t) = V + v_{ripple} \approx V \qquad i_L(t) = I_L + i_{ripple} \approx I_L$$

General Algorithm for the Calculations of Conversion Ratio and Inductor Currents

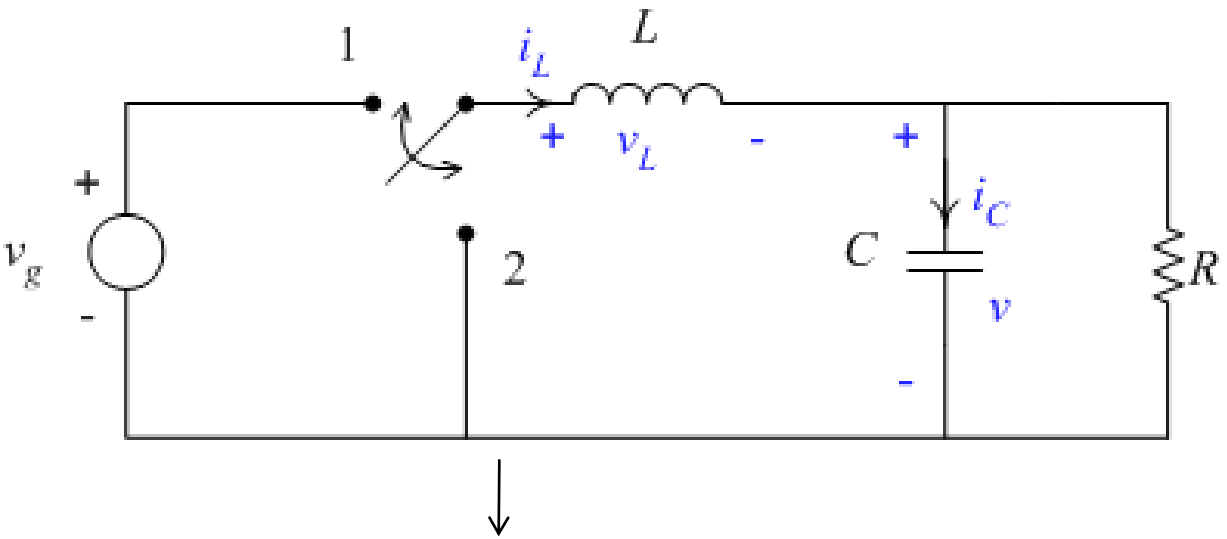
4. Apply inductor volt-second balance to find the conversion ratio

$$\langle v_L(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{Ts} v_L(t)dt = 0$$

5. Apply capacitor charge balance to find inductor currents

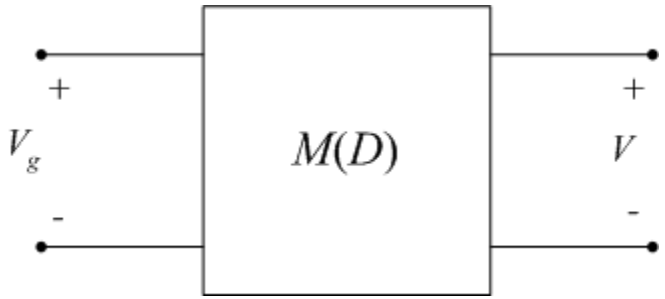
$$\langle i_C(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{Ts} i_C(t)dt = 0$$

Buck Converter



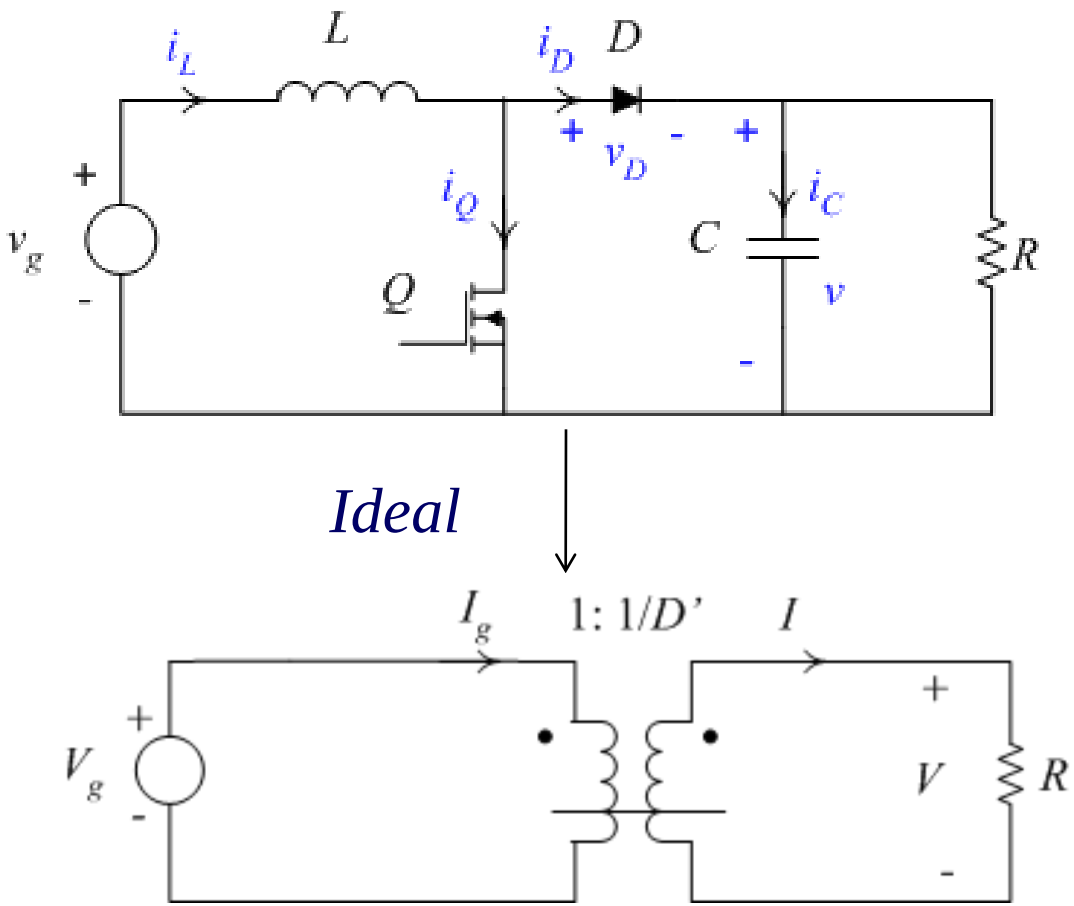
$$DV_g = V$$

$$I_L = \frac{V}{R}$$



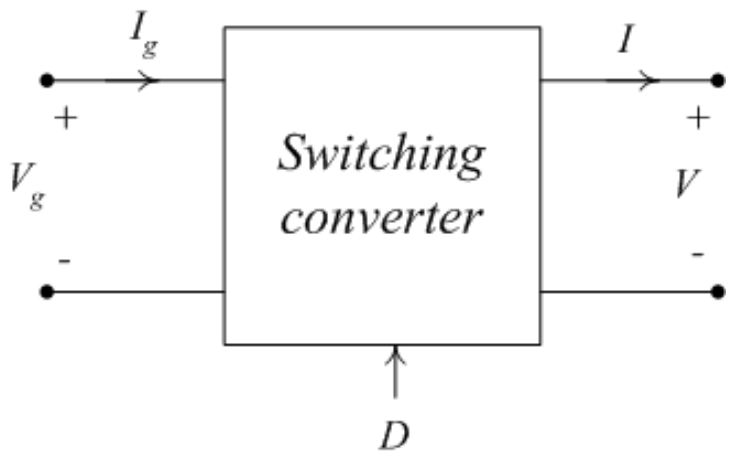
$$M(D) = D$$

Ideal Boost Example



Inclusion of Losses and DC Equivalent Circuits

DC Transformer Model

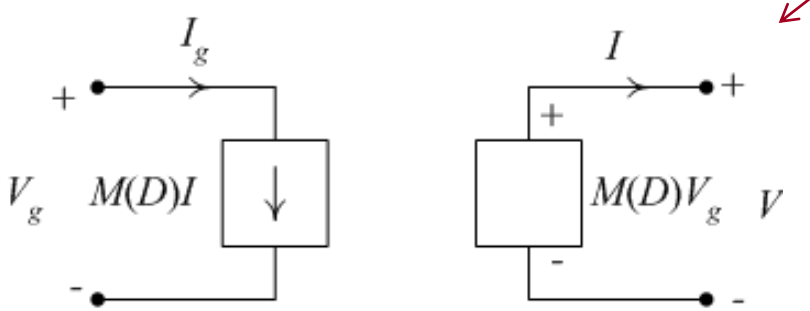


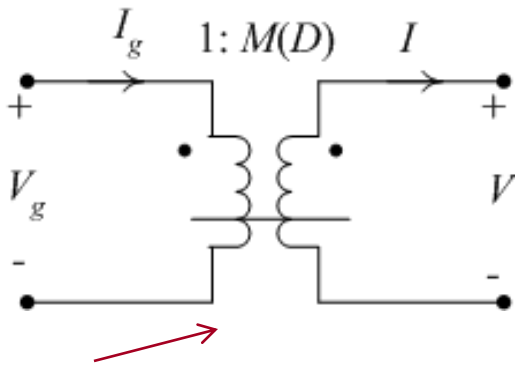
In the ideal, i.e. lossless, case

$$P_{in} = P_{out} \Rightarrow V_g I_g = VI$$

$$V = M(D)V_g$$

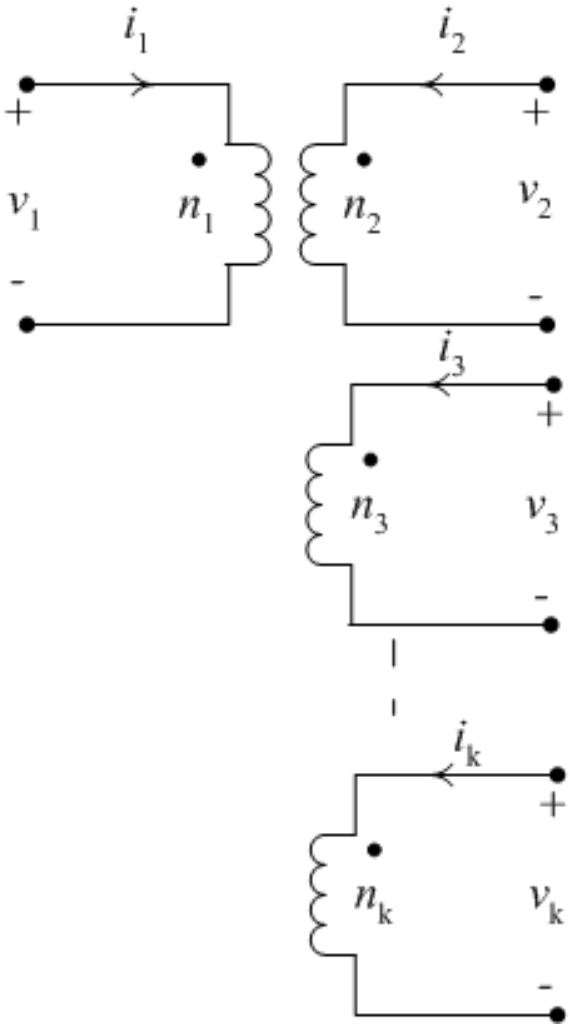
$$I_g = M(D)I$$





A dc-dc converter behaves as a "dc transformer" whose conversion ratio is controllable.

Transformers: Basic Rules and Labeling Convention



Element constrains

$$\frac{v_1}{n_1} = \frac{v_2}{n_2} = \frac{v_3}{n_3} = \ldots = \frac{v_k}{n_k}$$

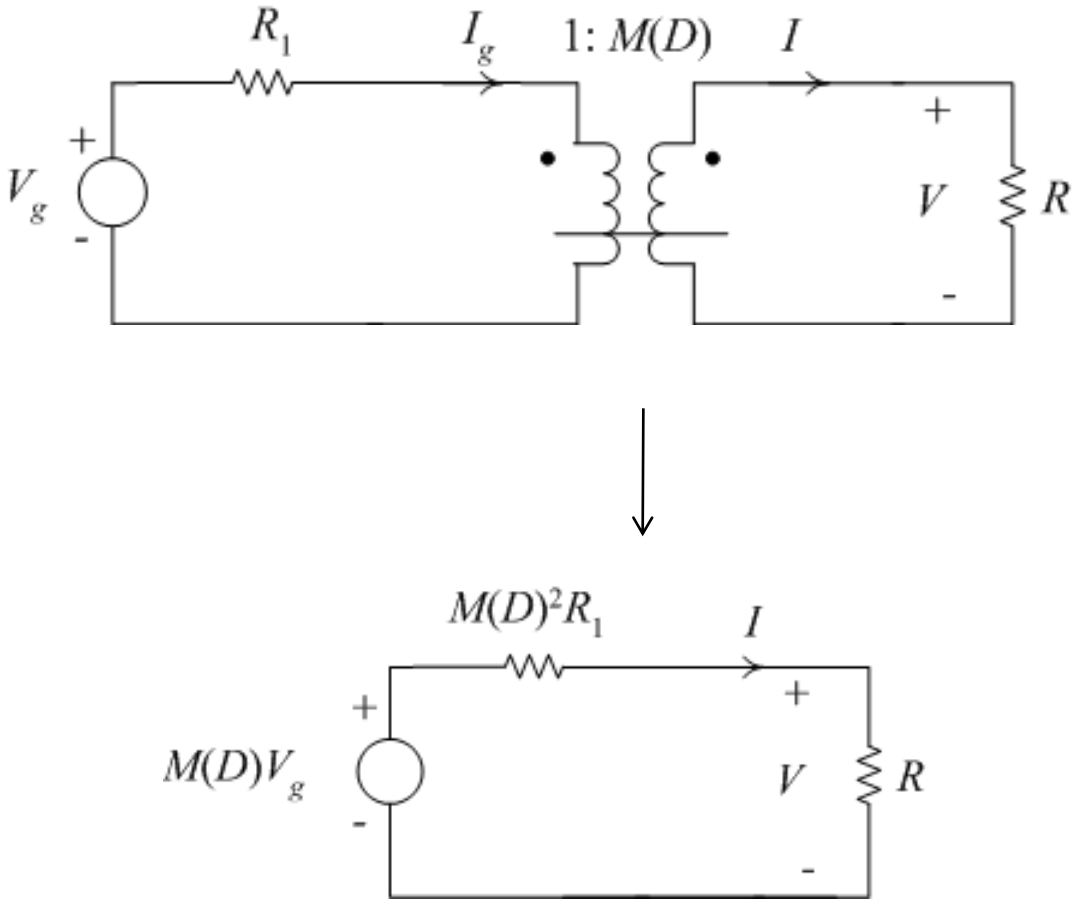
$$n_1 i_1 + n_2 i_2 + n_3 i_3 + \ldots + n_k i_k = 0$$

Two-winding case

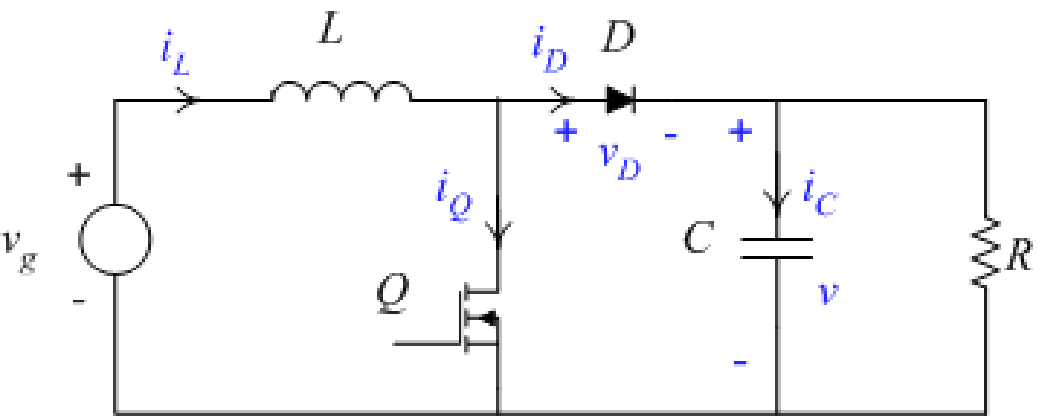
$$v_1 \frac{n_2}{n_1} = v_2$$

$$i_2 = -\frac{n_1}{n_2} i_1$$

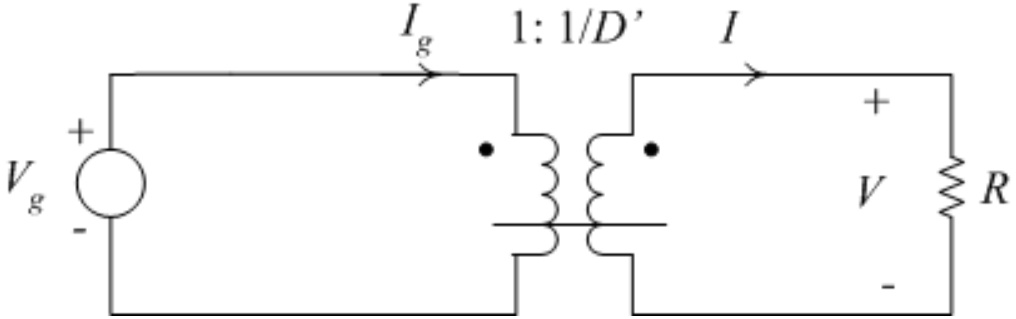
Transformers: Basic Rules and Labeling Convention



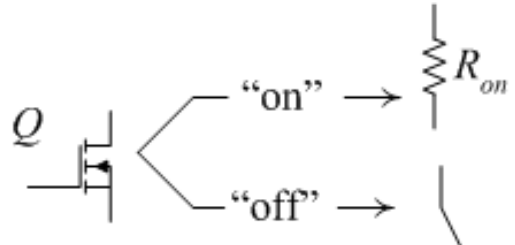
Modeling of Conduction Losses

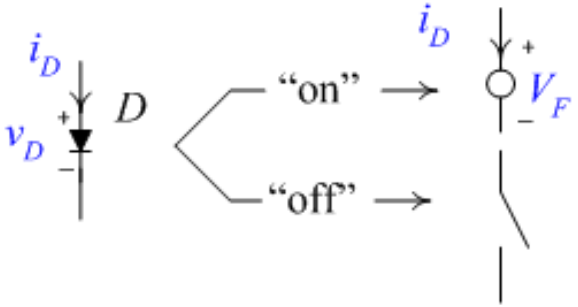


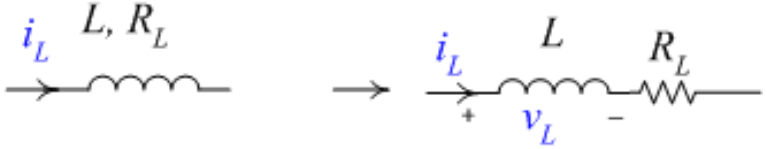
Ideal



Components models that include losses





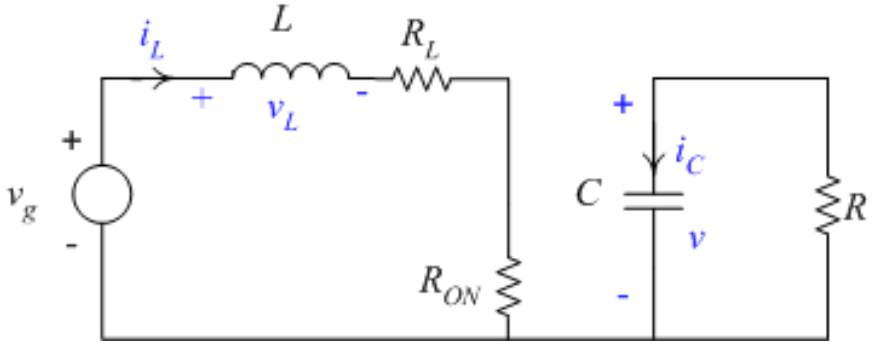


Inclusion of Losses and Construction of an Equivalent Circuit

- *Again, we apply small-ripple approximation, inductor volt-second balance, and capacitor charge balance*
- *Unlike in the ideal case, volt-second balance, and capacitor charge balance equations are not independent. The current going through resistive components causes voltage drop that affects inductor voltage.*
- *Need to construct equivalent circuits corresponding to volt-second balance and capacitor charge balance equations and solve them.*
- *Equation describing average input current is also very useful*

Volt-Second Equations and SRA

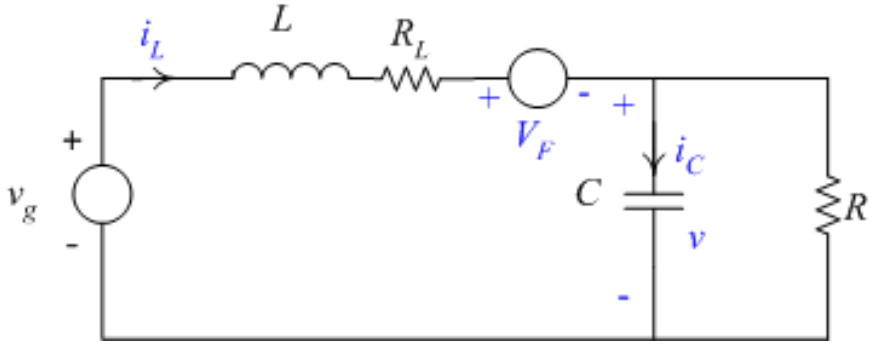
$0 < t \le DT_s$



$$v_L(t) = v_g(t) - i_L(t)_L - i_L(t)R_{ON} \approx$$

$$\approx V_g - I_L R_L - I_L R_{ON}$$

$DT_s < t \le T_s$



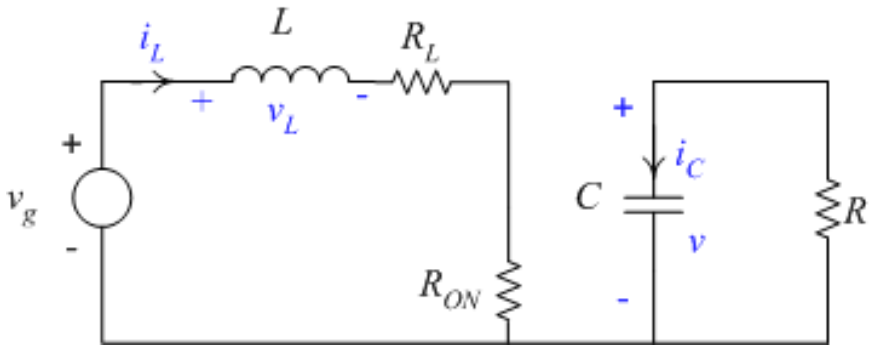
$$v_L(t) = v_g(t) - i_L(t)R_L - V_F - v(t) \approx$$

$$\approx V_g - I_L R_L - V_F - V$$

$$\langle v_L(t) \rangle_{Ts} = \frac{1}{T_s} \int_0^{Ts} v_L(t)dt = V_g - R_L I_L - DR_{on} I_L - D'V_F - D'V = 0$$

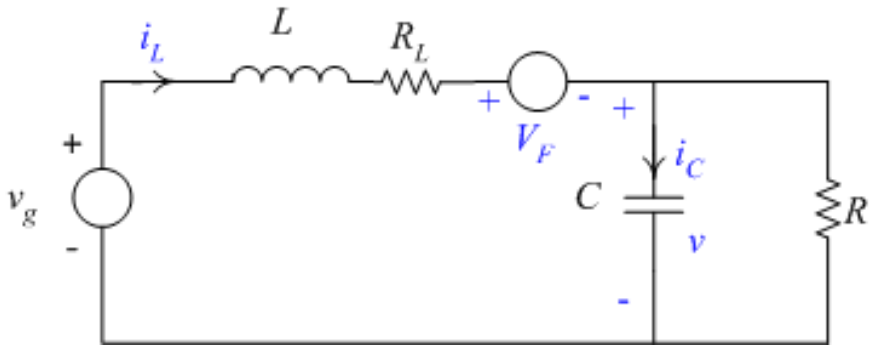
Capacitor Charge Balance & SRA

$0 < t \le DT_s$



$$i_C(t) = -\frac{v(t)}{R} = -\frac{V}{R}$$

$DT_s < t \le T_s$

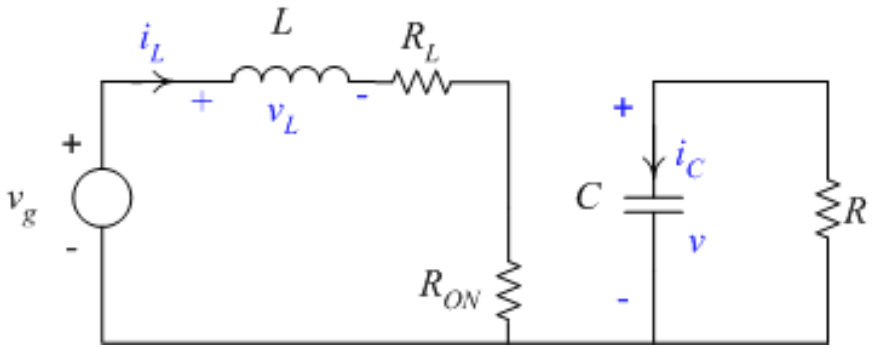


$$i_C(t) = i_L(t) - \frac{v(t)}{R} = I_L - \frac{V}{R}$$

$$\left\langle i_C(t) \right\rangle_{Ts} = D' I_L - \frac{V}{R} = 0$$

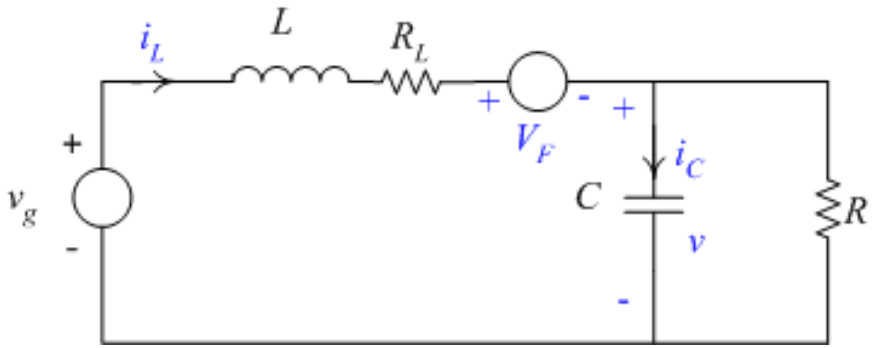
Average Input Current & SRA

$0 < t \le DT_s$



$$i_g(t) = i_L(t) = I_L$$

$DT_s < t \le T_s$



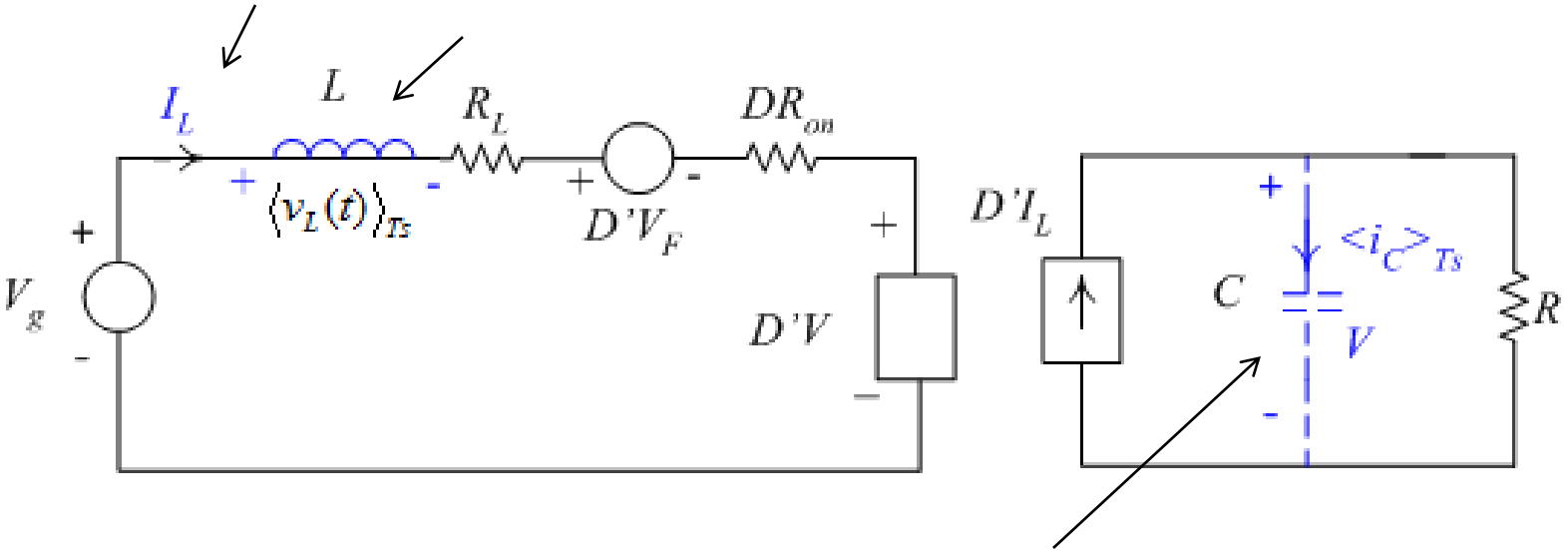
$$i_g(t) = i_L(t) = I_L$$

$$\left\langle i_g(t) \right\rangle_{Ts} = I_L$$

Construction of Equivalent Circuits

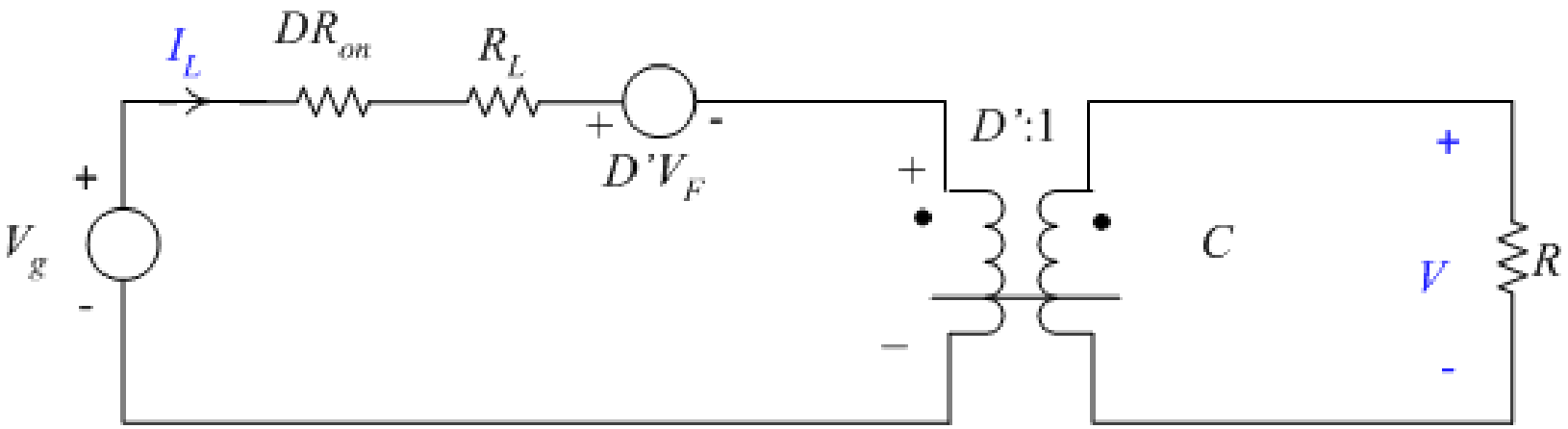
$$\langle i_g(t)\rangle_{Ts} = I_L$$

$$\langle v_L(t)\rangle_{Ts} = V_g - R_L I_L - DR_{on} I_L - D'V_F - D'V = 0$$



$$\langle i_C(t)\rangle_{Ts} = D' I_L - \frac{V}{R} = 0$$

DC Equivalent Circuit

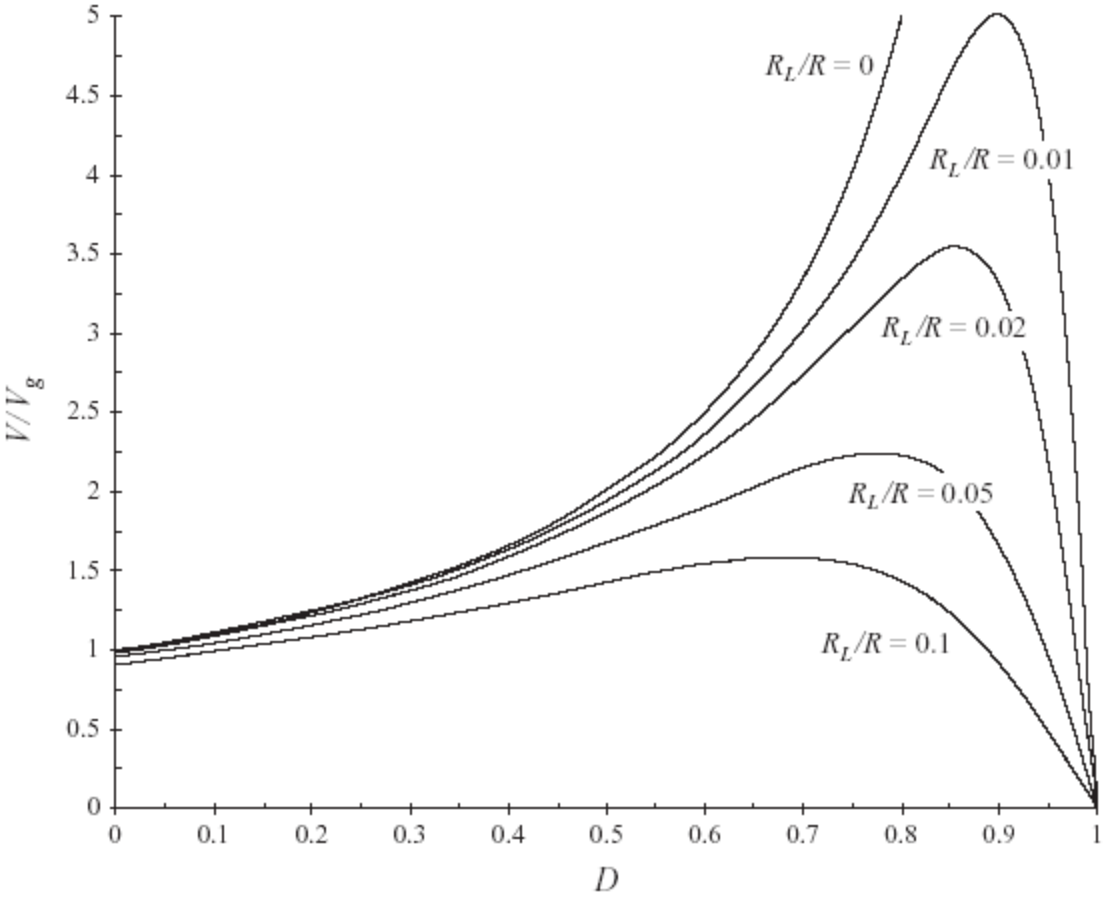


Conversion ratio of a realistic boost converter

$$\frac{V}{V_g} = \frac{1}{D'}\left(1 - \frac{D'V_F}{V_g}\right)\frac{1}{1 + \frac{R_L + DR_{on}}{D'^2 R}}$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{1 - \frac{D'V_D}{V_g}}{1 + \frac{R_L + DR_{on}}{D'^2 R}}$$

Conversion ratio of an Realistic Boost



General Algorithm for the Construction of Equivalent Circuit

1. *Draw equivalent circuits for both portions of the switching interval:*
   - *Include "on" and "off" models of components*
   - *Arbitrary assign inductor current and capacitor voltages*

2. *Express inductor voltages in terms of the input and capacitor voltages, products of resistive elements and inductor currents, and diode voltage drops.*

3. *Express capacitor currents in terms of inductor currents and v/R, (or output currents)*

4. *Write expressions for the input current in terms of inductor currents.*

General Algorithm for the Construction of Equivalent Circuit

5. Apply small-ripple approximation (SRA)

$$v(t) = V + v_{ripple} \approx V \qquad i_L(t) = I_L + i_{ripple} \approx I_L \qquad v_g(t) = V_g + v_{g\_ripple} \approx V_g$$

6. Apply inductor volt-second balance

$$\langle v_L(t) \rangle_{Ts} = \frac{1}{T_s} \int_0^{Ts} v_L(t)dt = 0$$

7. Apply capacitor charge balance

$$\langle i_C(t) \rangle_{Ts} = \frac{1}{T_s} \int_0^{Ts} i_C(t)dt = 0$$

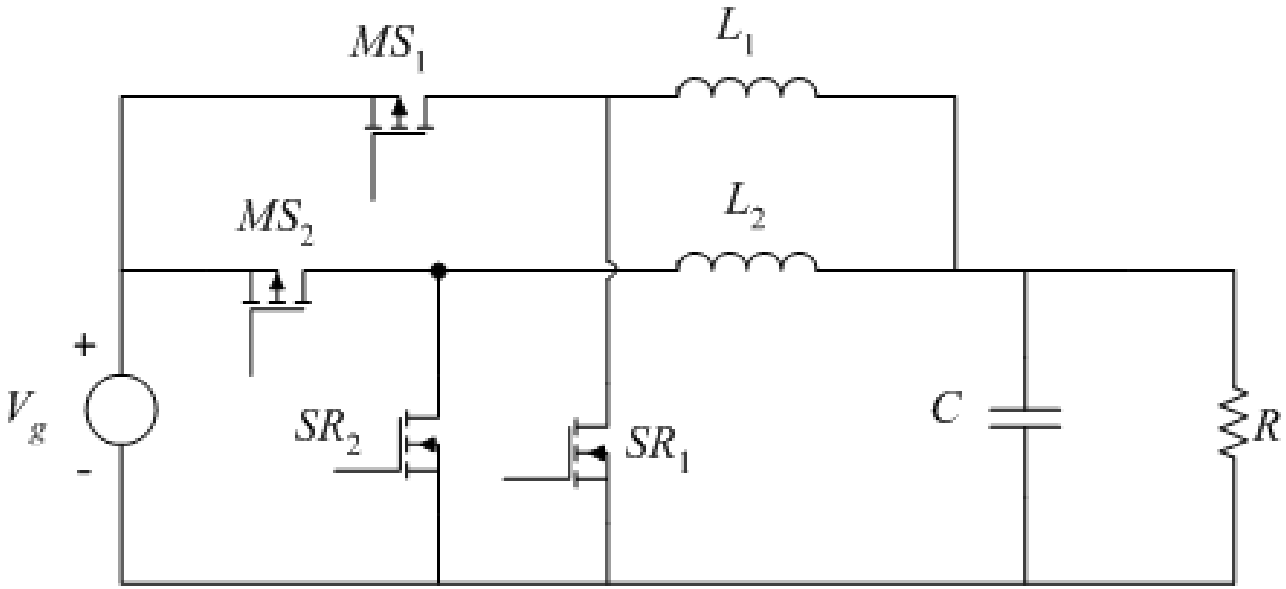
General Algorithm for the Calculations of Conversion Ratio and Inductor Currents

8. *Find average value of the input current (usually not zero)*

$$\left\langle i_g(t) \right\rangle_{Ts} = \frac{1}{T_s} \int_0^{Ts} i_g(t)dt$$

9. *From equations obtained through steps 6 to 8 construct an equivalent circuit*

Example: Realistic Interleaved Buck Converter

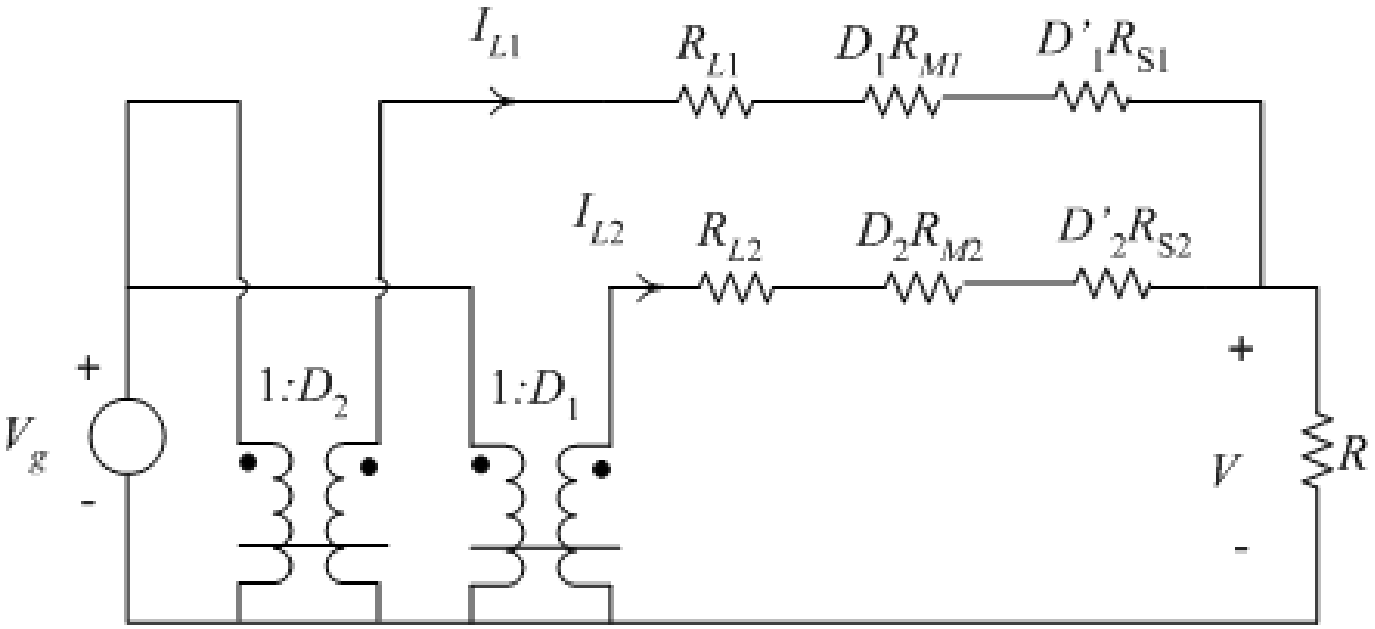


$0 < t \le D_1 T_s$ MS_1 *is in "on state"*

$0 < t \le D_2 T_s$ MS_2 *is in "on state"*

All transistors and inductors have non-zero resistances

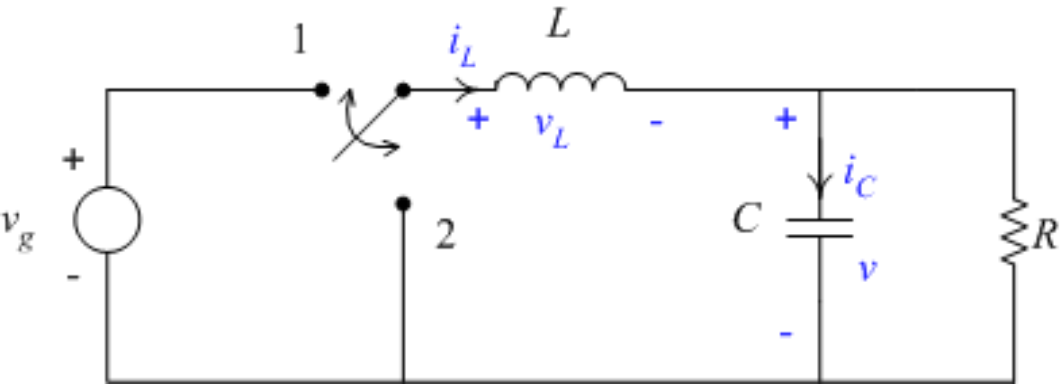
Example: Realistic Interleaved Buck Converter - Equivalent Circuit -



Can be used for power components selection, current sharing analysis, efficiency analysis….

AC Equivalent Circuits Modeling and Converter Transfer Functions

Power Stage Modeling: Game Plan



Time varying nonlinear circuit

Linear time invariant ac equivalent circuit

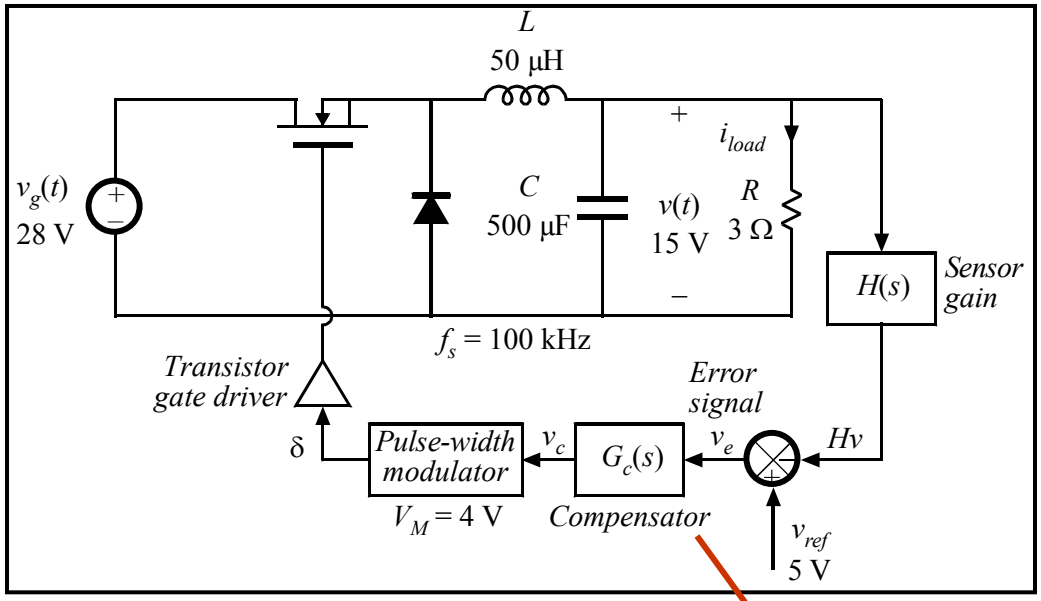
Transfer functions:

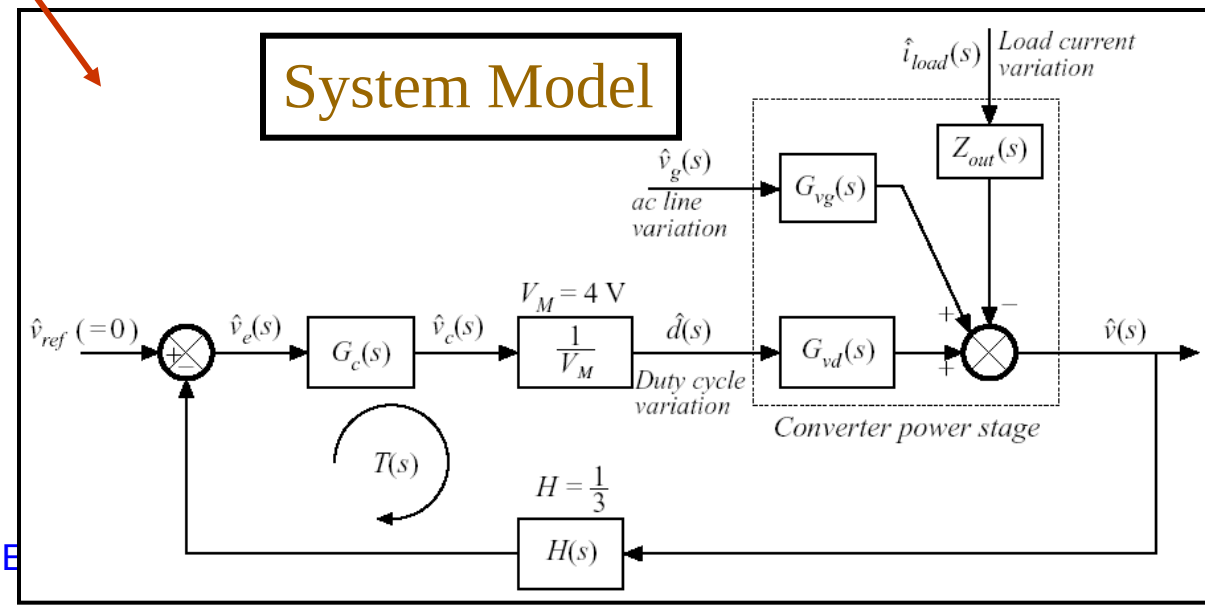
Control-to-output t.f.

Input-to-output t.f.

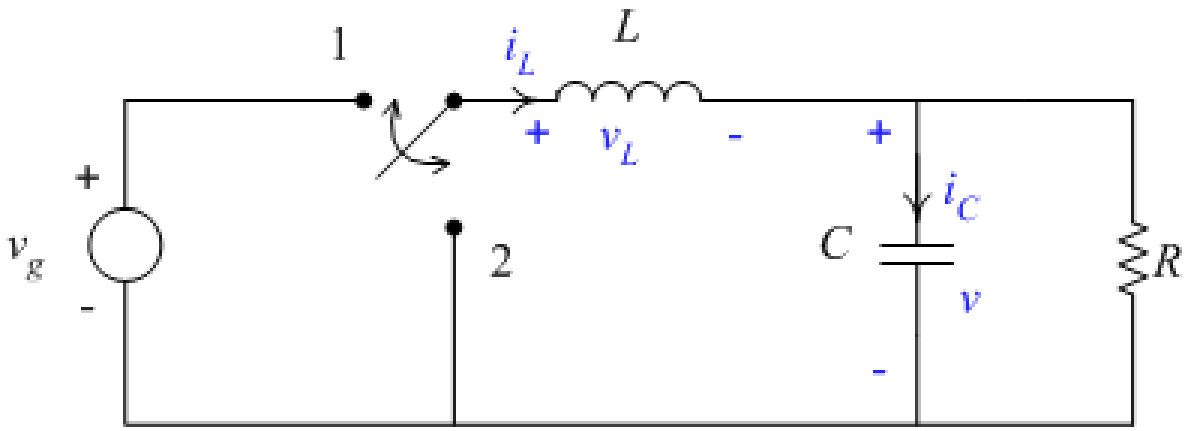
Output impedance

Power Stage Modeling: Game Plan





AC Behavior



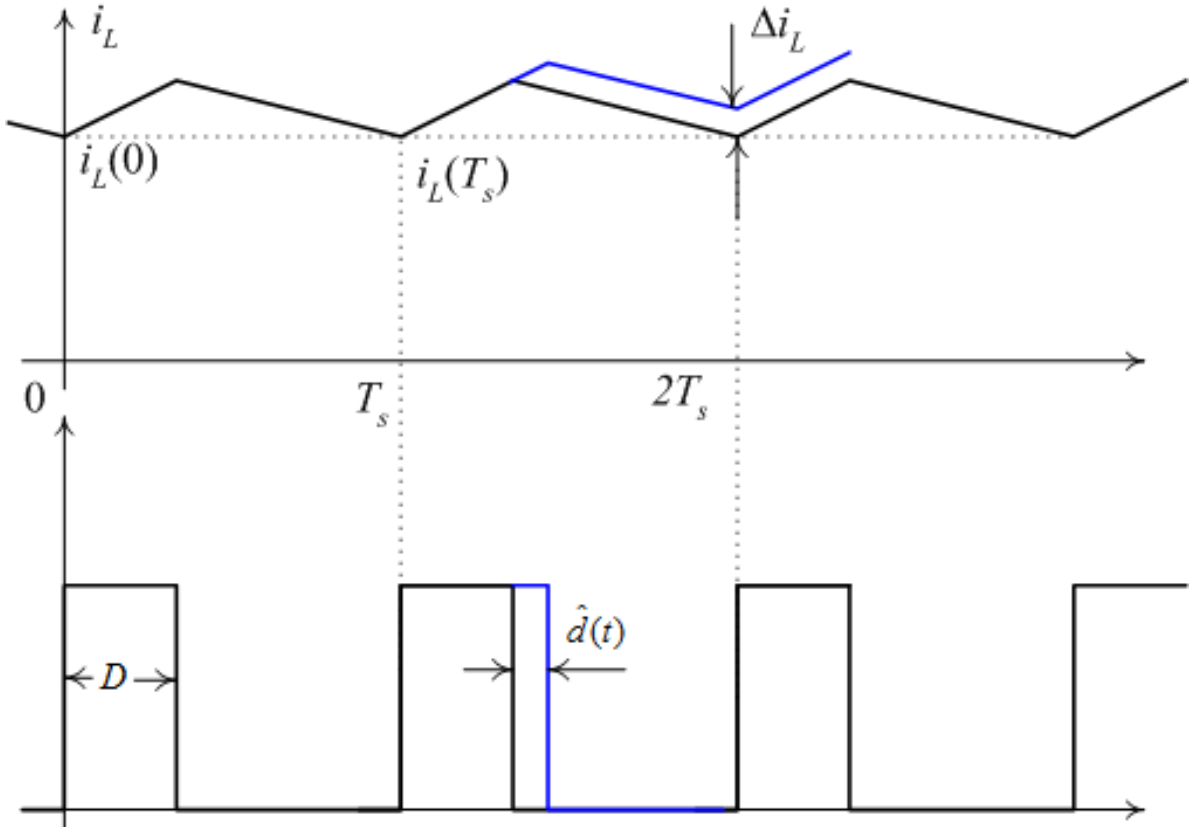
$$V = DV_g \quad DC\ equations$$

$$d(t) = D_0 + D_m \sin(\omega t)$$

$$v(t) \neq d(t)V_g$$

For ac, the results of dc analysis usually cannot be directly applied

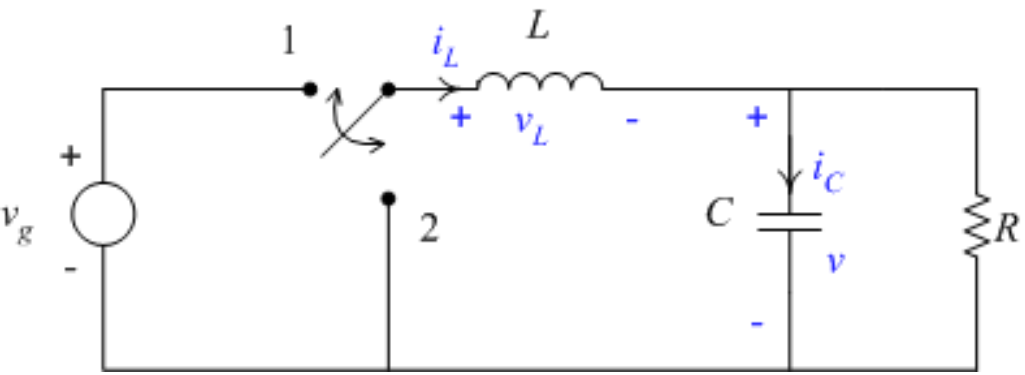
Perturbation Effect



- *Averaging works and removes switching frequency ripple well.*
- *Volt-second balance and capacitor charge balance are not valid anymore*

$$0 \neq \frac{1}{T}\int_{nTs}^{(n+1)Ts} v_L(t)dt = \langle v_L(t)\rangle_{Ts} = L\frac{d\langle i_L(t)\rangle_{Ts}}{dt}$$

Creation of a Linear Time-Invariant Eq. Circuit (Reminder)



Time varying nonlinear circuit

↓

Averaging over Ts

↓

Averaged time-invariant equations

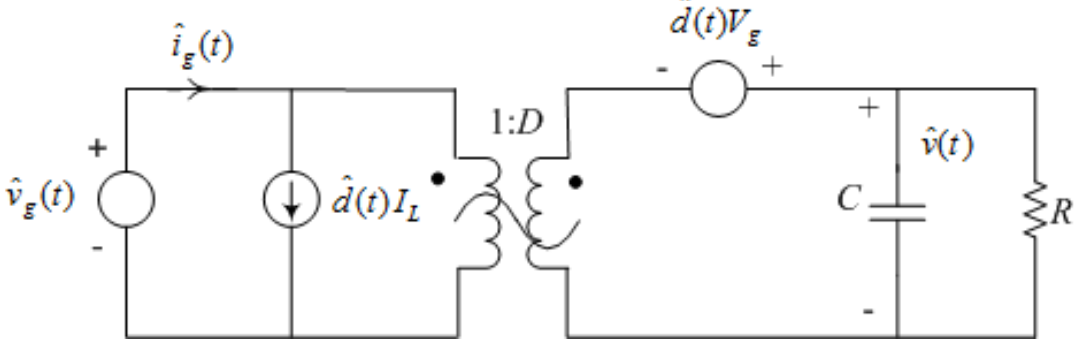
Linearization

Linear time-invariant equations

↓

Construction of eq. circuit

↓



Three Basic Techniques Used in the Construction of AC Equivalent Circuit

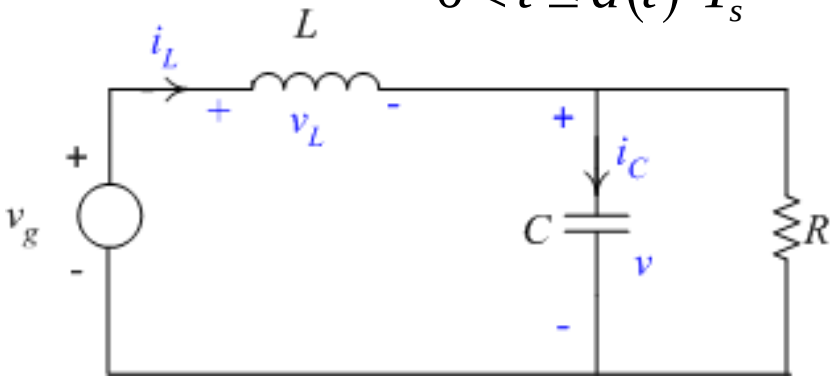
1. *Averaging that eliminates switching ripple and the time varying nature of the circuit*

2. *Mathematical, i.e. analytical, perturbation that emulates effect of small signal variation around the operating point*

3. *Linearization that allows us to construct a time-invariant nonlinear model*

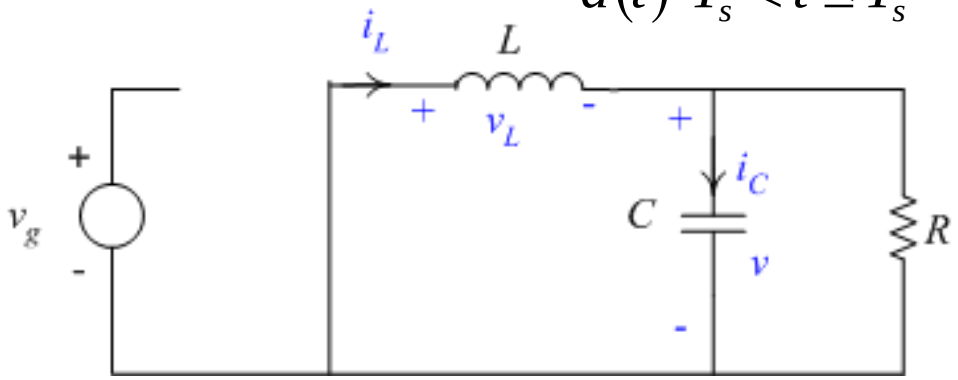
Creation of a Small-Signal Eq. Circuit for a Buck Converter (Averaging Inductor Waveforms)

$$0 < t \le d(t)\cdot T_s$$



$$v_L(t) = v_g(t) - v(t)$$

$$d(t)\cdot T_s < t \le T_s$$



$$v_L(t) = -v(t)$$

$$\left\langle v_L(t)\right\rangle_{Ts} = L\frac{d\left\langle i_L(t)\right\rangle_{Ts}}{dt} = d(t)\cdot\left\langle v_g(t)\right\rangle_{Ts} - \left\langle v(t)\right\rangle_{Ts} \neq 0$$

Perturbation and Linearization

$$\left\langle v_L(t)\right\rangle_{Ts} = L\frac{d\left\langle i_L(t)\right\rangle_{Ts}}{dt} = d(t)\cdot\left\langle v_g(t)\right\rangle_{Ts} - \left\langle v(t)\right\rangle_{Ts} \neq 0$$

Perturbation

$$d(t) = D + \hat{d}(t) \qquad D >> \hat{d}(t)$$

$$\left\langle v(t)\right\rangle_{Ts} = V + \hat{v}(t) \qquad V >> \hat{v}(t)$$

$$\left\langle i_L(t)\right\rangle_{Ts} = I_L + \hat{i}_L(t) \qquad I_L >> \hat{i}_L(t)$$

$$\left\langle i_g(t)\right\rangle_{Ts} = I_g + \hat{i}_g(t) \qquad I_g >> \hat{i}_g(t)$$

Combining Perturbation & Averaging Results

$$L\frac{d\left(I_L+\hat{i}_L(t)\right)}{dt}=\left(D+\hat{d}(t)\right)\cdot\left(V_g+\hat{v}_g(t)\right)-\left(V+\hat{v}(t)\right)$$

Dc terms

2nd order terms

$$L\frac{dI_L}{dt}+L\frac{d\hat{i}_L}{dt}=DV_g-V+D\cdot\hat{v}_g(t)+\hat{d}(t)V_g-\hat{v}(t)+\hat{d}(t)\hat{v}_g(t)$$

1st order terms

This equation is still time varying nonlinear, due to the 2nd order terms

Linearization

$$L\frac{dI_L}{dt}+L\frac{d\hat{i}_L}{dt}=DV_g-V+D\cdot\hat{v}_g(t)+\hat{d}(t)V_g-\hat{v}(t)+\hat{d}(t)\hat{v}_g(t)$$

$=0$

Multiplication of two small terms

$$L\frac{dI_L}{dt}=DV_g-V=0$$

Dc terms, give us dc solution

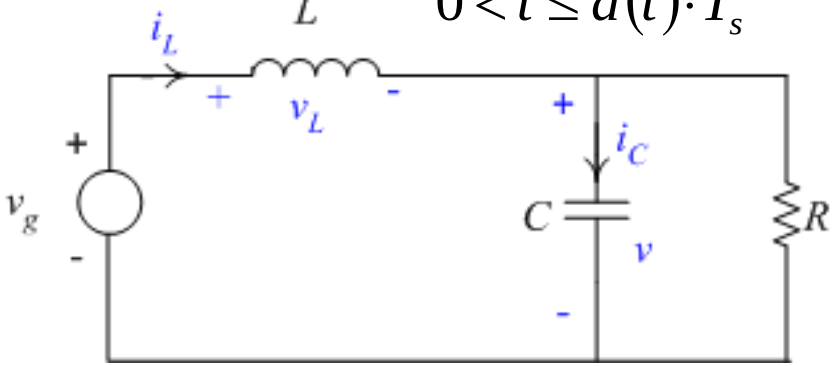
$$L\frac{d\hat{i}_L}{dt}=D\cdot\hat{v}_g(t)+\hat{d}(t)V_g-\hat{v}(t)$$

1st order terms: linear time-invariant equations

The 1st order terms are used for construction of an equivalent circuit

Capacitor and Input Current Averaging

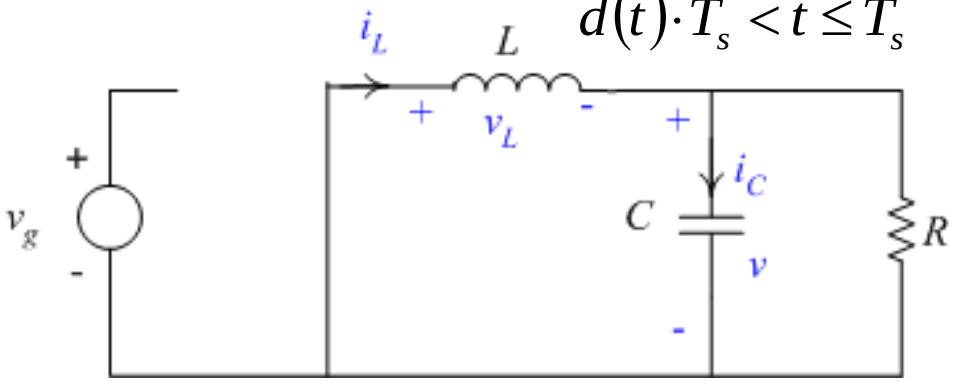
$0 < t \le d(t)\cdot T_s$



$$i_c(t) = i_L(t) - \frac{v(t)}{R}$$

$$i_g(t) = i_L(t)$$

$d(t)\cdot T_s < t \le T_s$



$$i_c(t) = i_L(t) - \frac{v(t)}{R}$$

$$i_g(t) = 0$$

$$\left\langle i_C(t)\right\rangle_{Ts} = C\frac{d\left\langle v(t)\right\rangle_{Ts}}{dt} = \left\langle i_L(t)\right\rangle_{Ts} - \left\langle v(t)\right\rangle_{Ts}/R$$

$$\left\langle i_g(t)\right\rangle_{Ts} = d(t)\cdot\left\langle i_L(t)\right\rangle_{Ts}$$

Perturbation and Linearization

$$C\frac{d\left(V+\hat{v}(t)\right)}{dt}=\left(I_L+\hat{i}_L(t)\right)-\frac{V+\hat{v}(t)}{R}$$

Capacitor current

$$I_g+\hat{i}_g(t)=(D+\hat{d}(t))\cdot(I_L+\hat{i}_L(t))$$

Input current

$$C\frac{d\hat{v}(t)}{dt}=\hat{i}_L(t)-\frac{\hat{v}(t)}{R}$$

1st order terms for capacitor current

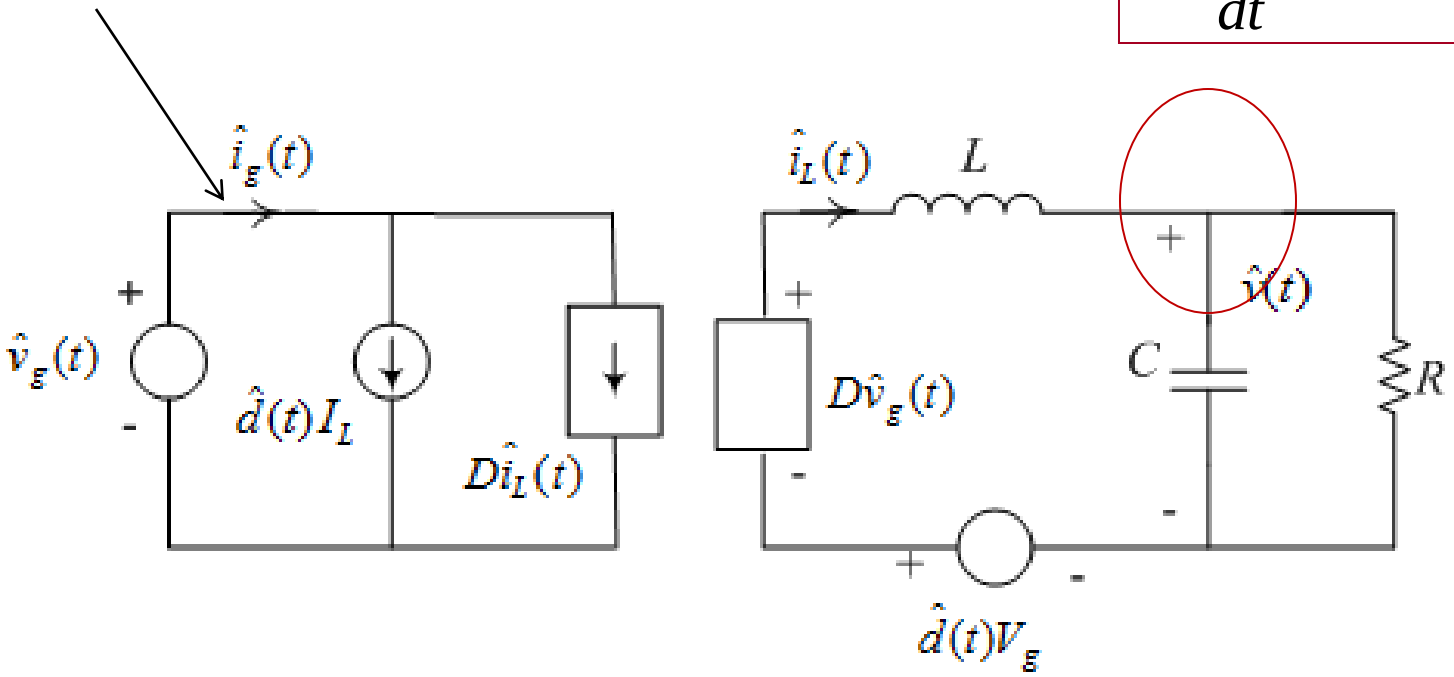
$$\hat{i}_g(t)=\hat{d}(t)\cdot I_L+D\cdot\hat{i}_L(t)$$

1st order terms for the input current

Construction of AC Equivalent Circuit

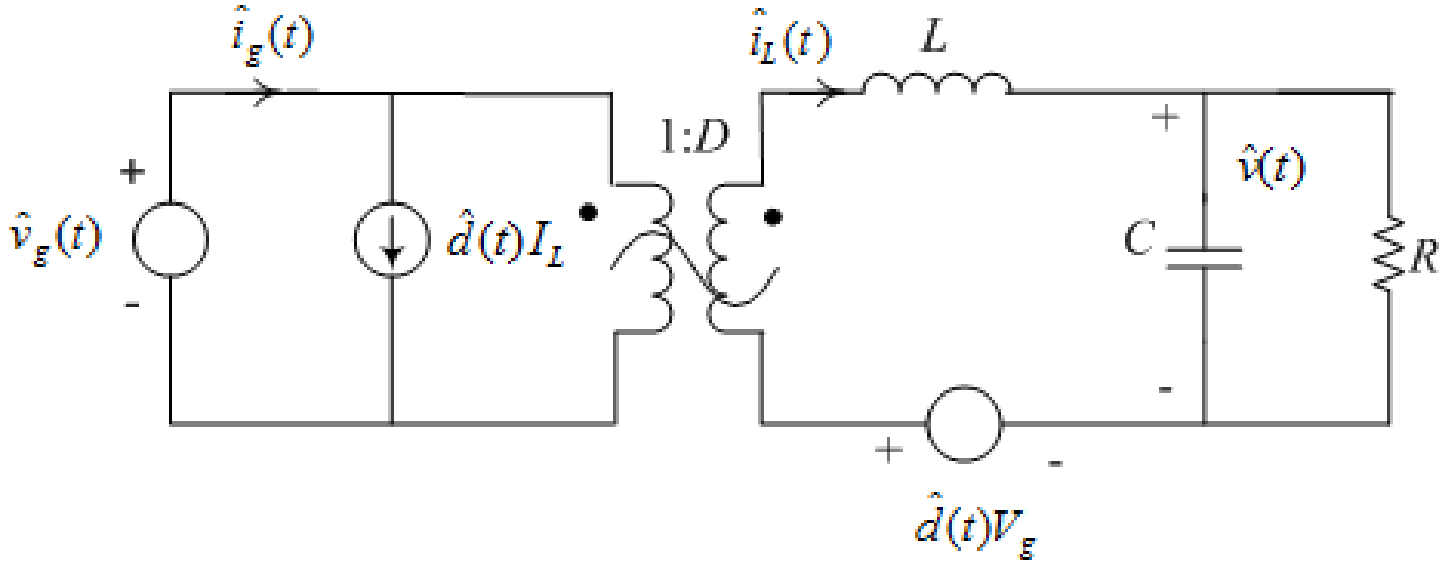
$$\hat{i}_g(t) = \hat{d}(t) \cdot I_L + D \cdot \hat{i}_L(t)$$

$$C\frac{d\hat{v}(t)}{dt} = \hat{i}_L(t) - \frac{\hat{v}(t)}{R}$$

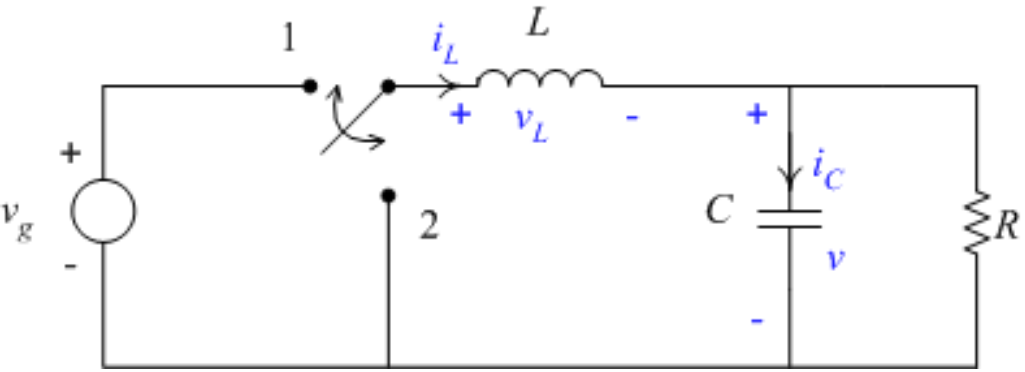


$$L\frac{d\hat{i}_L}{dt} = D \cdot \hat{v}_g(t) + \hat{d}(t)V_g - \hat{v}(t)$$

AC Equivalent Circuit of a Buck Converter



Summary of the Steps



Time varying nonlinear circuit

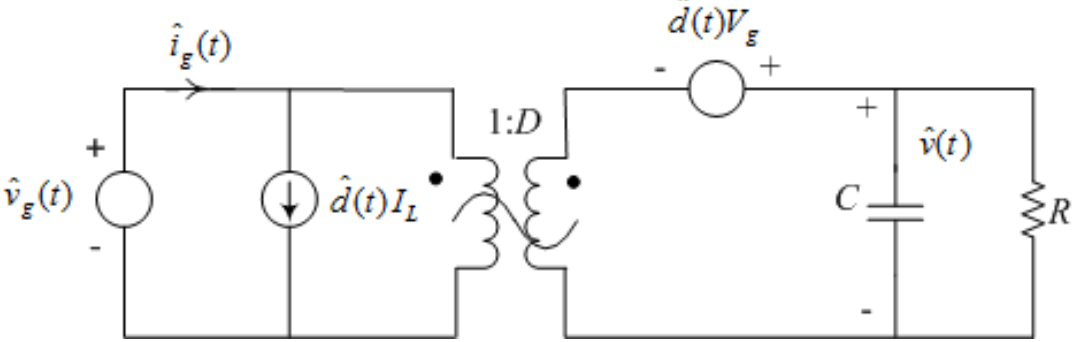
Averaging over Ts

Averaged time-invariant equations

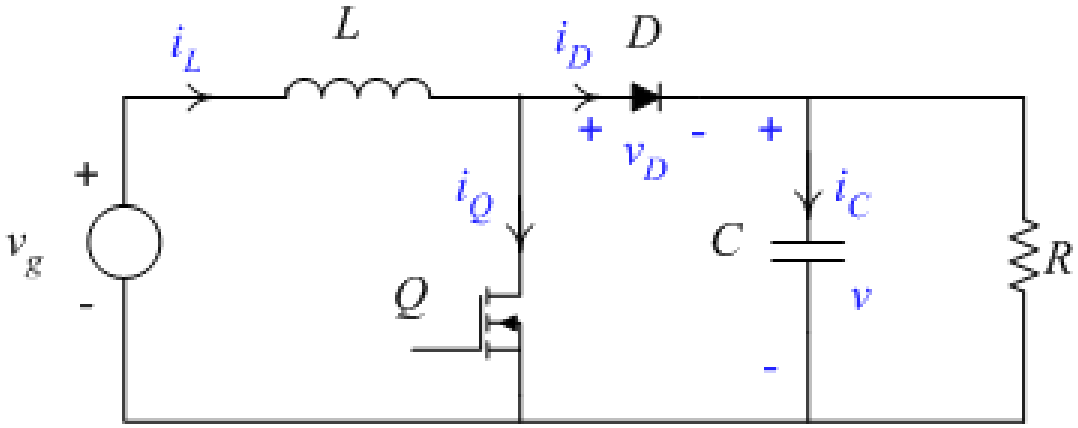
Linearization

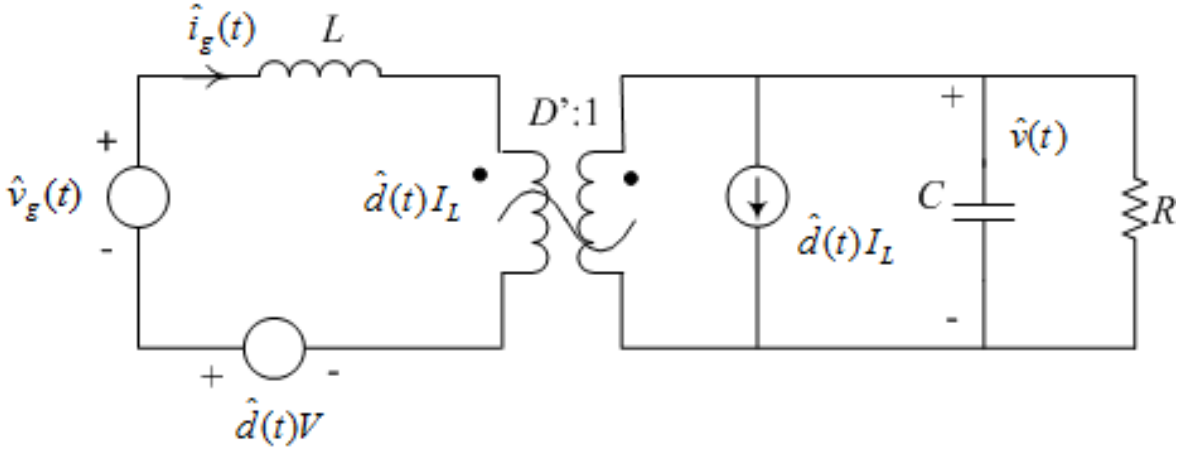
Construction of eq. circuit

Linear time-invariant equations



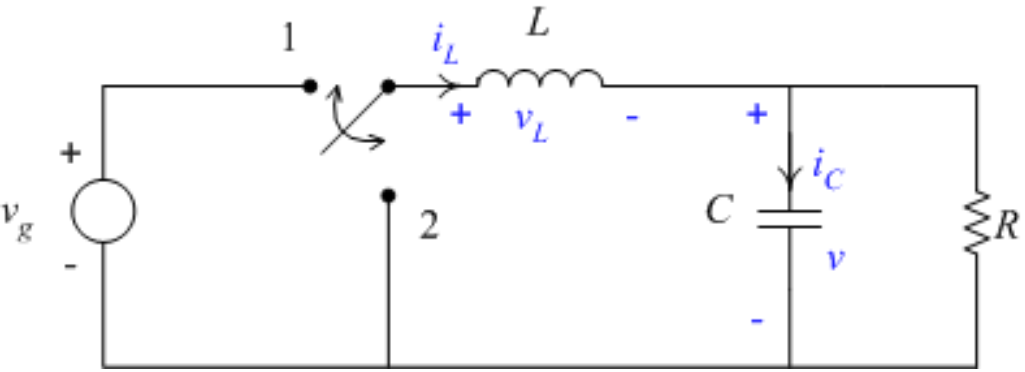
Boost Converter Example





Converter Transfer Functions

Creation of a Linear Time-Invariant Eq. Circuit



Time varying nonlinear circuit

↓

Averaging over Ts

↓

Averaged time-invariant equations

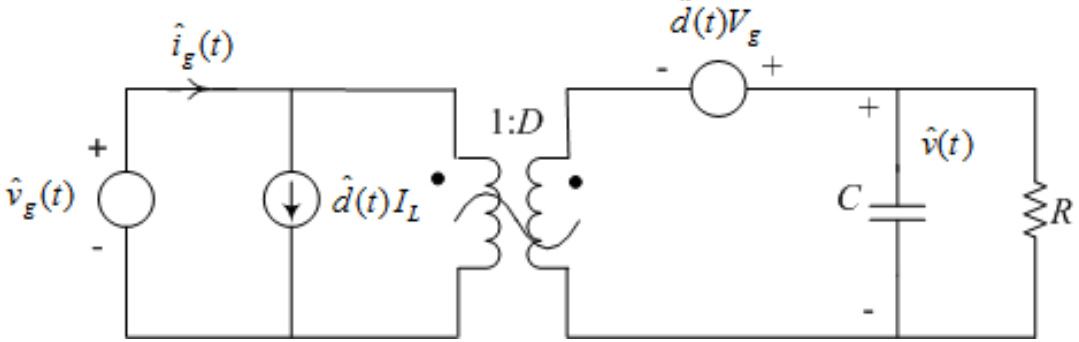
Linearization

Linear time-invariant equations

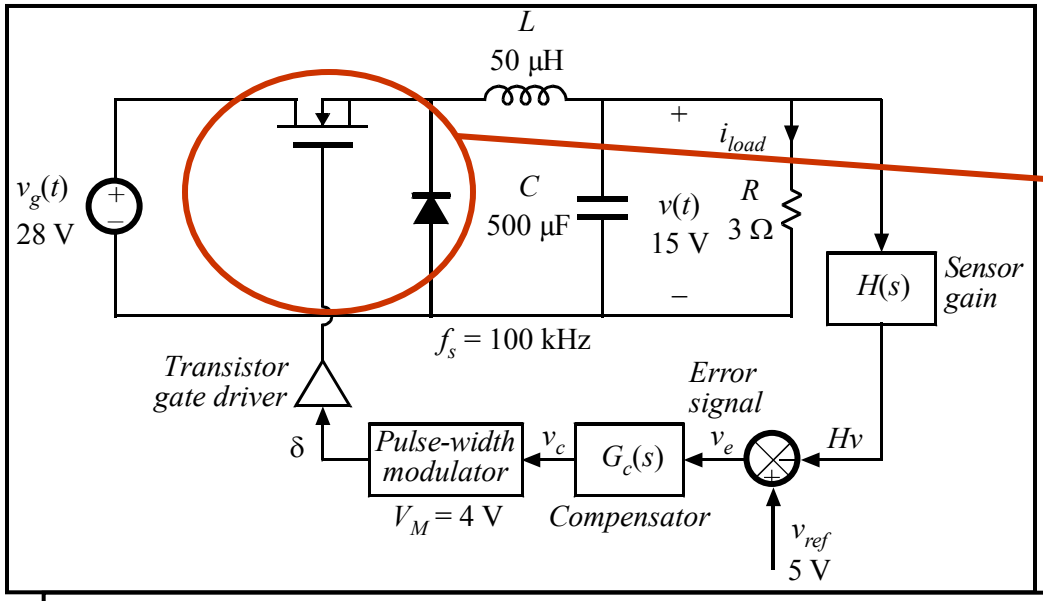
↓

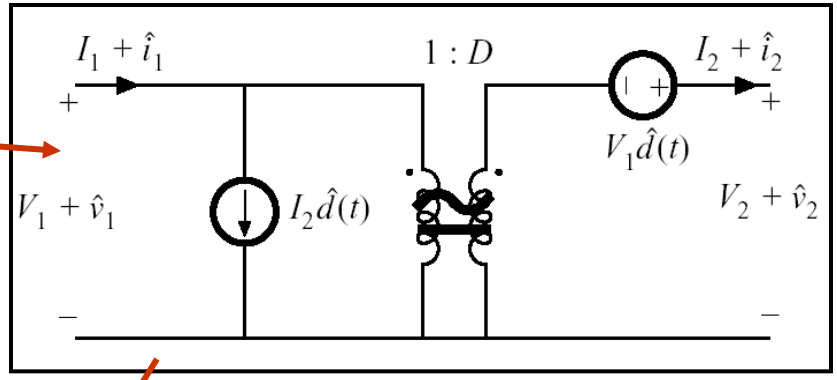
Construction of eq. circuit

↓

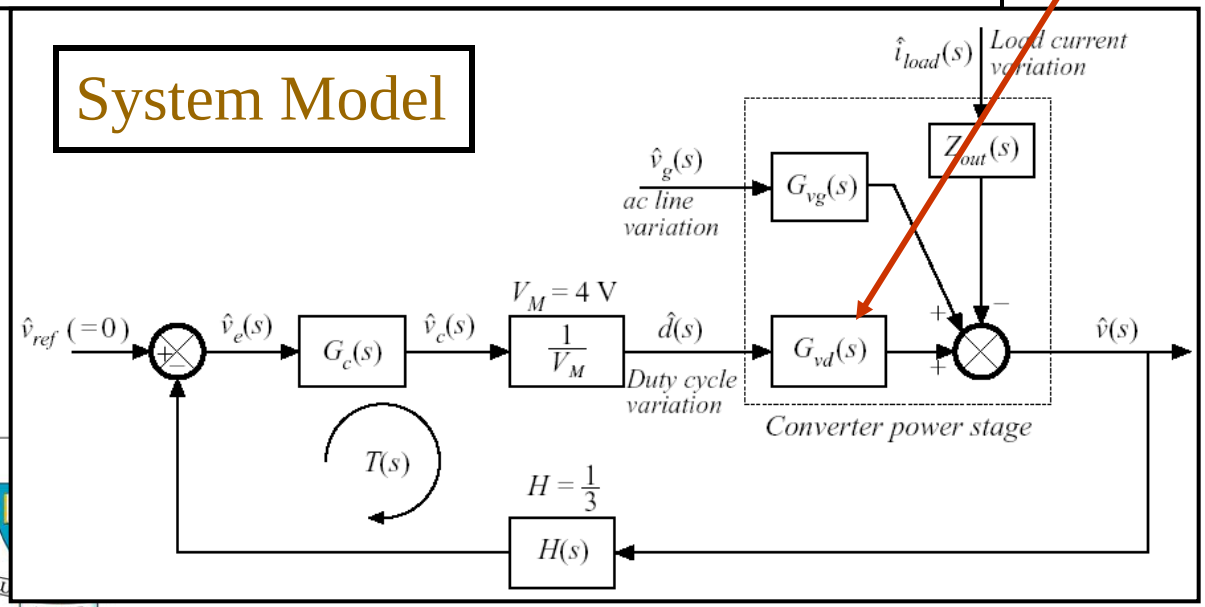


Buck Converter Example



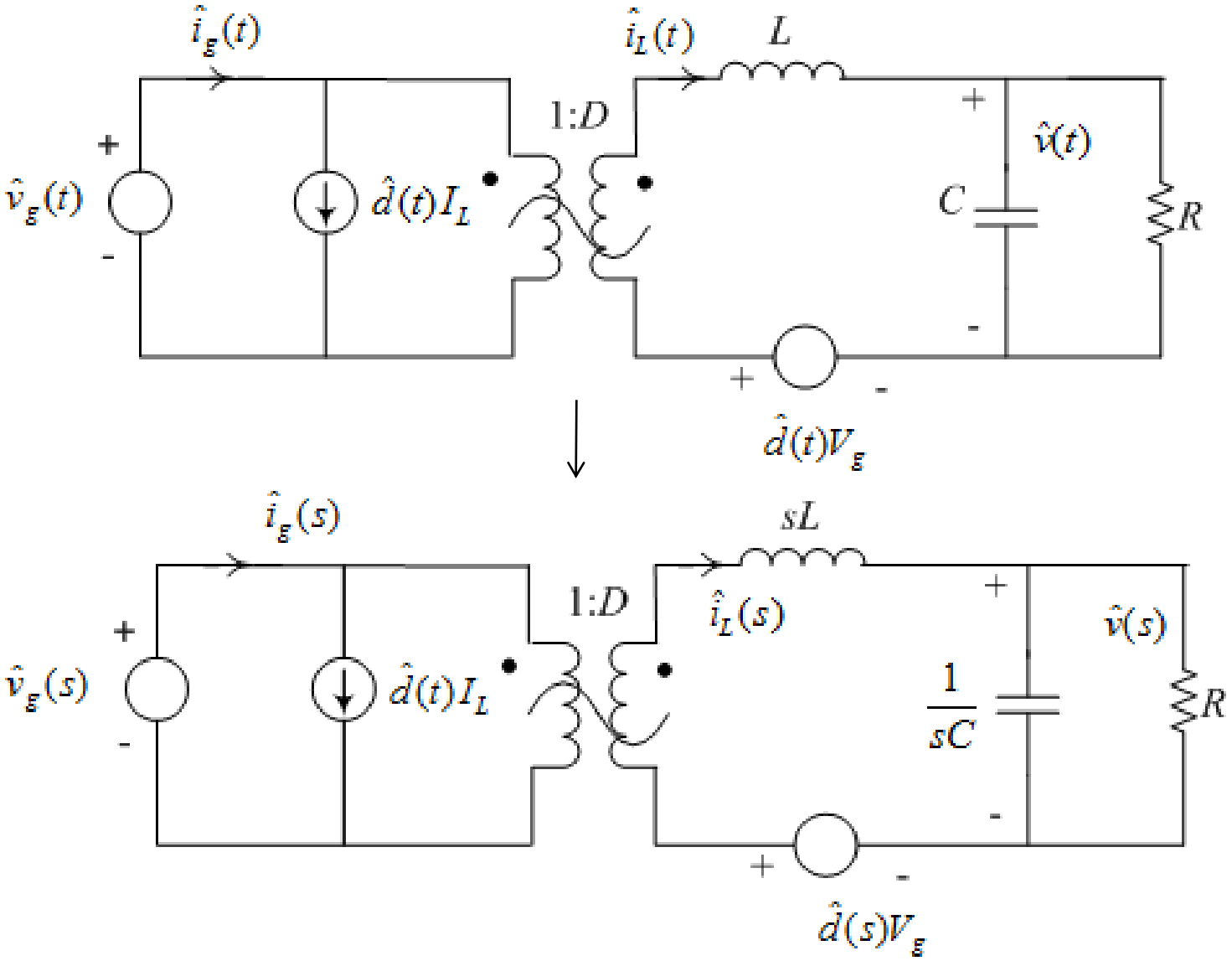


Gvd, Gvg and Zout

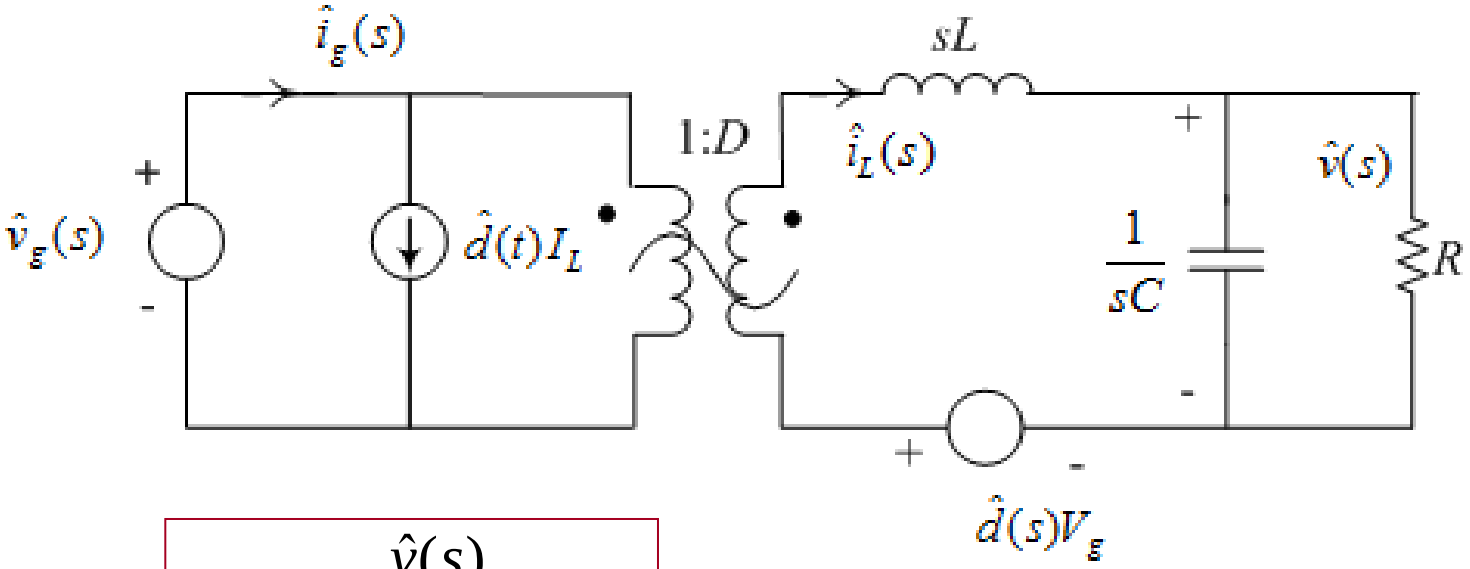


Averaged-switch model of Buck converter (with models of all common topologies readily available, including extensions for conduction & switching losses and CCM/DCM operating modes)

Transfer Into the s-domain



Basic Transfer Functions



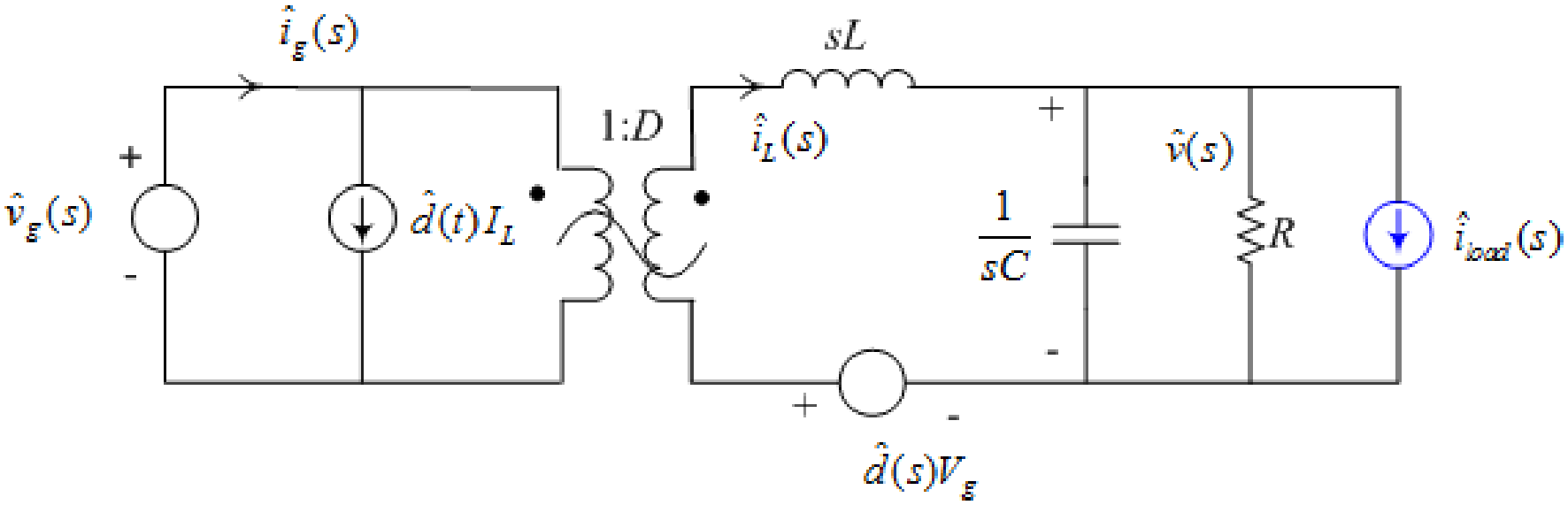
$$G_{vc}(s) = \frac{\hat{v}(s)}{\hat{d}(s)}\Big|_{v_g(s)=0,}$$

Control-to-output

$$G_{vc}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)}\Big|_{d(s)=0}$$

Input-to-output

Basic Transfer Functions



$$Z_{out}(s) = -\frac{\hat{v}(s)}{\hat{i}_{load}(s)}\Big|_{v_g(s)=0, d(s)=0}$$

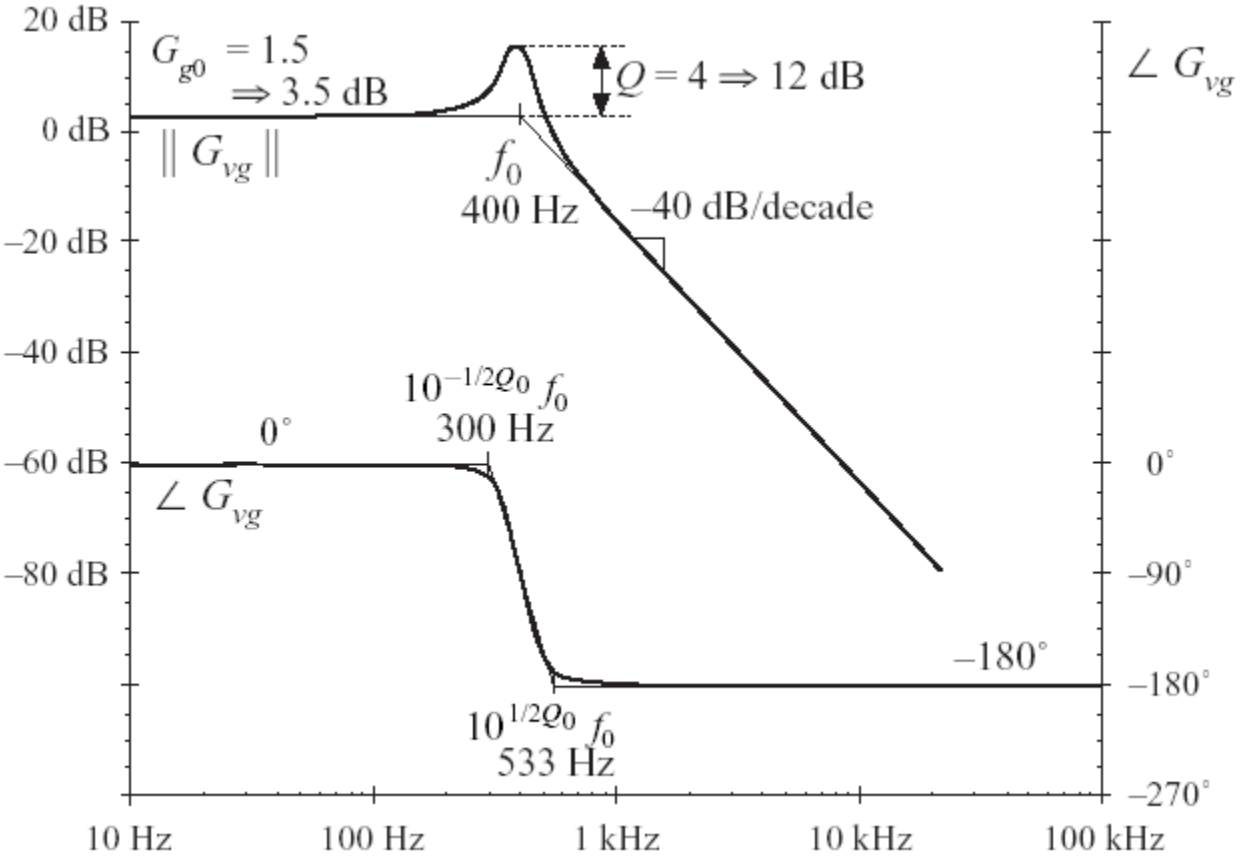
Output impedance

$$Z_{in}(s) = \frac{\hat{v}_g(s)}{\hat{i}_g(s)}\Big|_{v_g(s)=0, d(s)=0, i_{load}(s)=0}$$

Input impedance

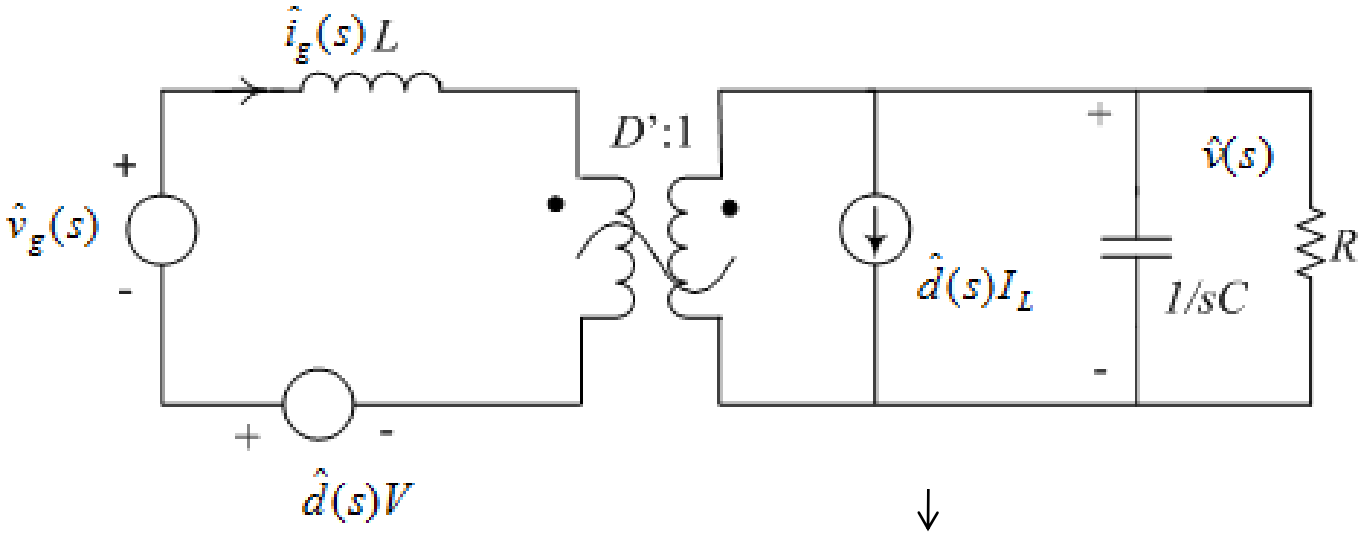
Typical Transfer Functions

$$G_{vg}(s) = \frac{G_{g0}}{1 + \frac{s}{Q\omega_0} + \frac{s}{\omega_0^2}}$$



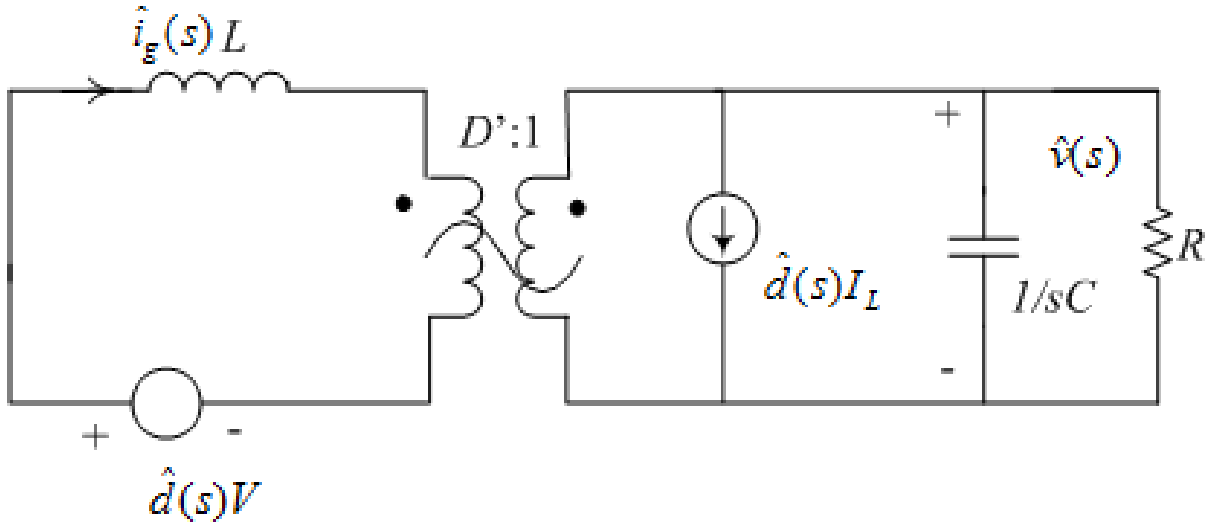
Control-to-output transfer function of buck-type converters have similar shape

Right-Half Plane Zero in Boost Type Converters

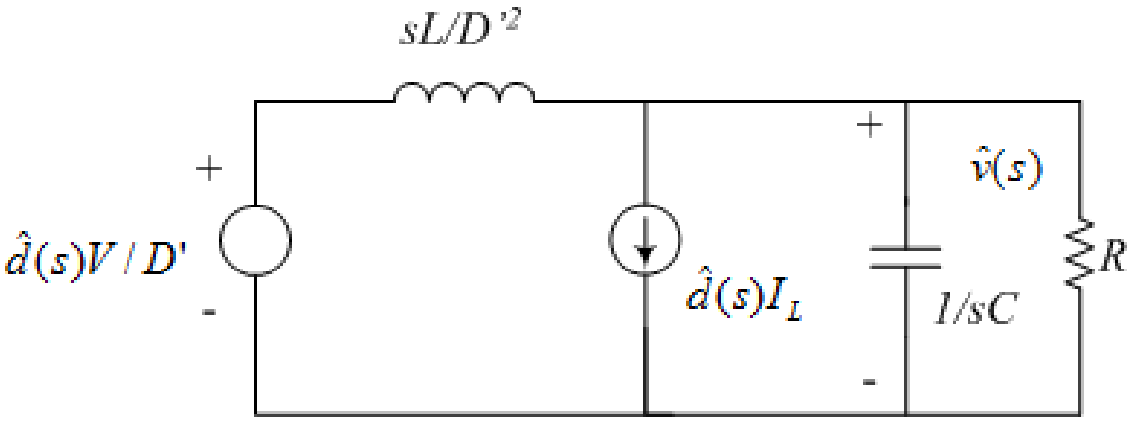


$$G_{vc}(s) = \frac{\hat{v}(s)}{\hat{d}(s)}\Big|_{v_g(s)=0,}$$

?

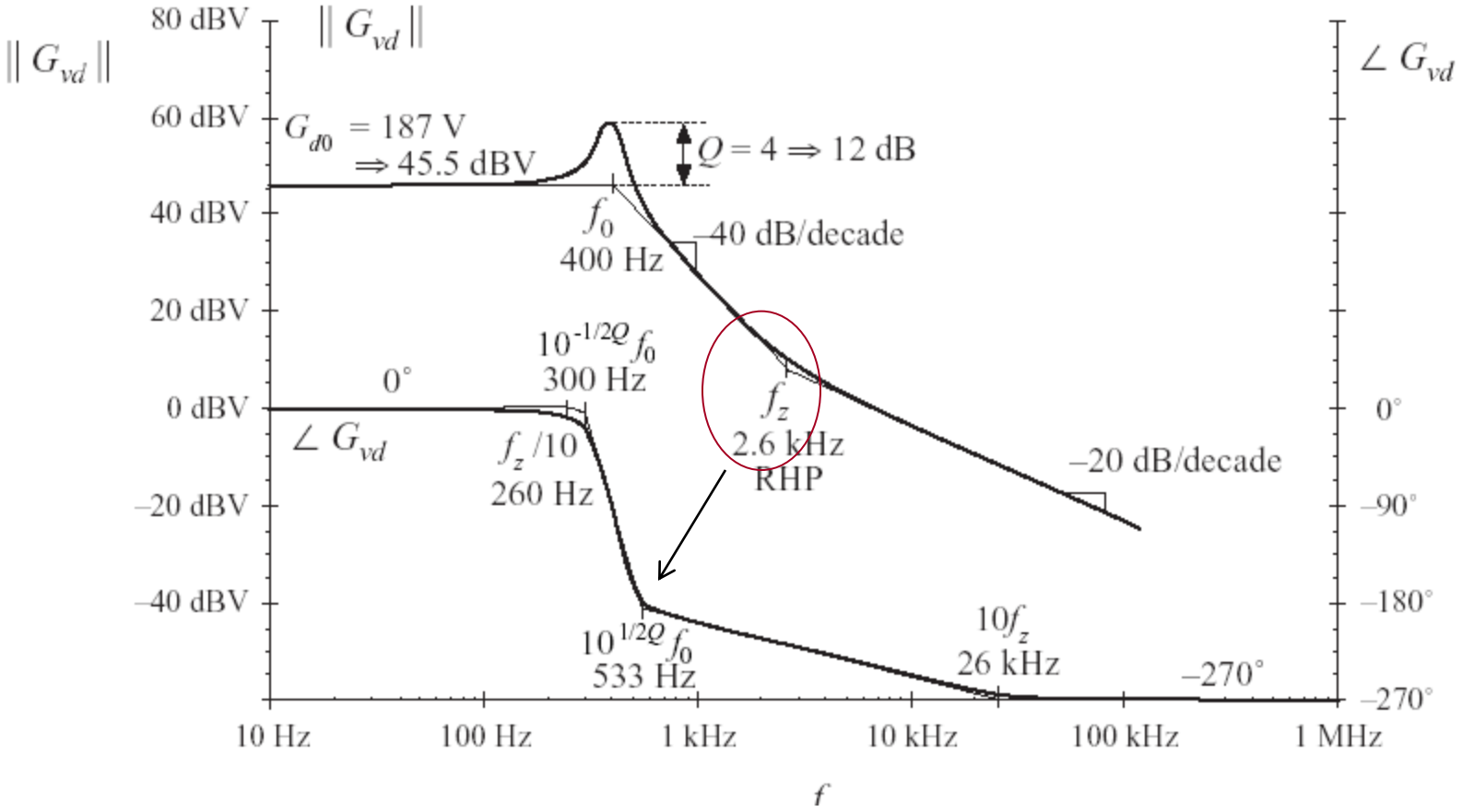


Right-Half Plane Zero

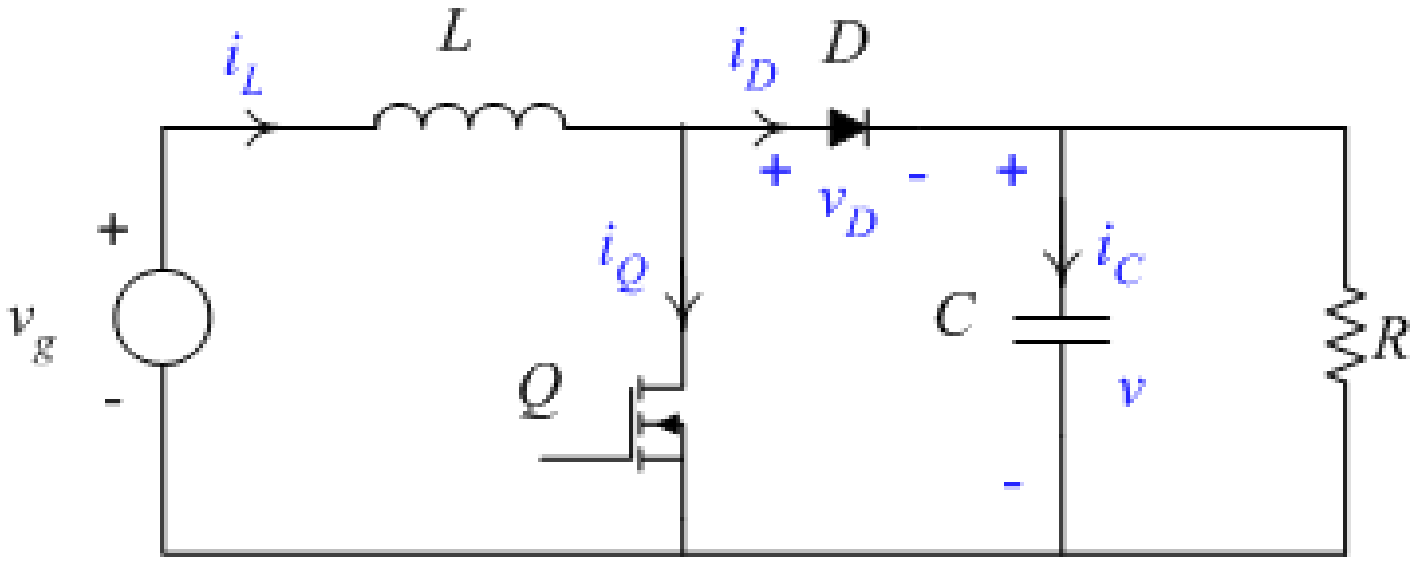


$$G_{vc}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = G_{d0} \frac{\left(1 - \frac{s}{\omega_z}\right)}{1 + \frac{s}{Q\omega_0} + \frac{s}{\omega_0^2}}$$

Right-Half Plane Zero

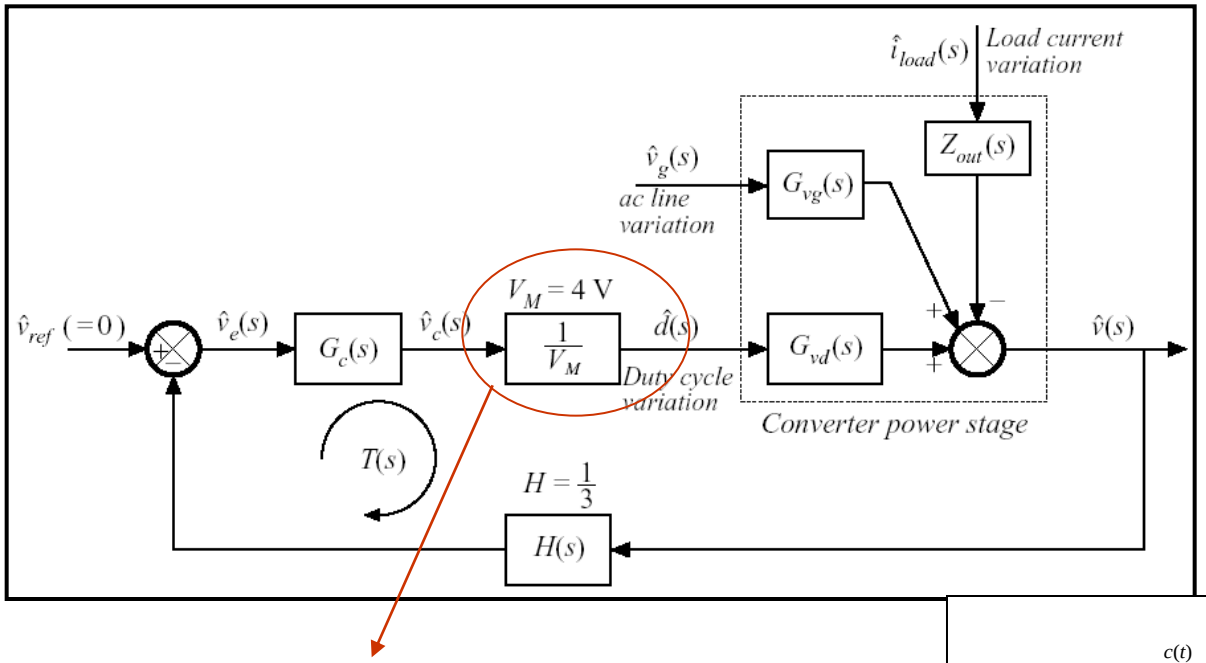


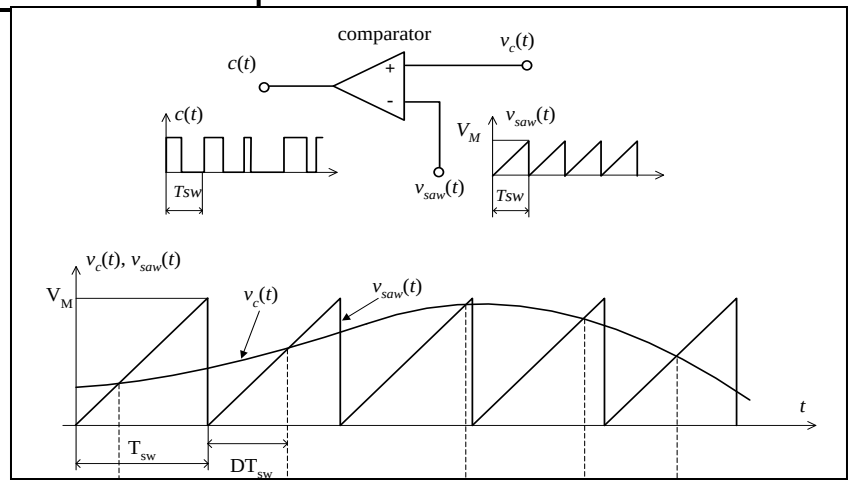
Explanation of RHZ in Indirect Energy Tr. Converers



For an initial load change Q turns on for a longer period, as a result, initially the capacitor is left without help of inductor and the voltage drops even further (until Q is turned off again)

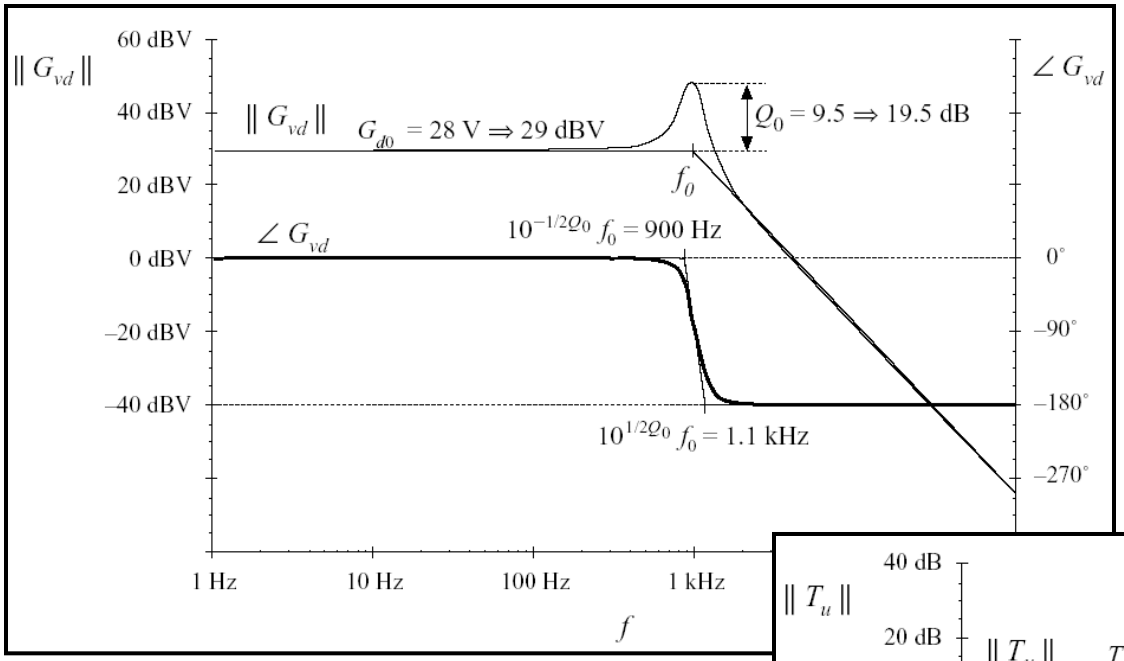
Modeling of Pulse Width Modulator





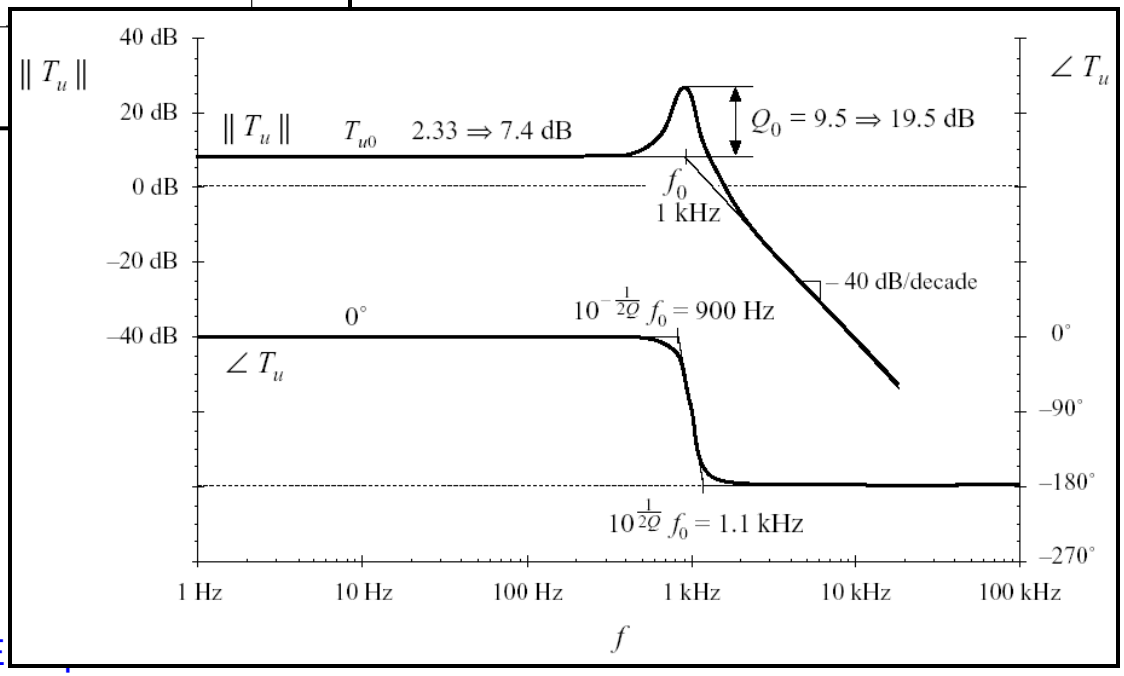
$$G_{pwm}(s) = \frac{1}{V_M},$$

Frequency Analysis



Determine the key characteristics in the control-to-output transfer function, $G_{vd}(s)$

$$G_{vd}(s) = \frac{v}{d}$$

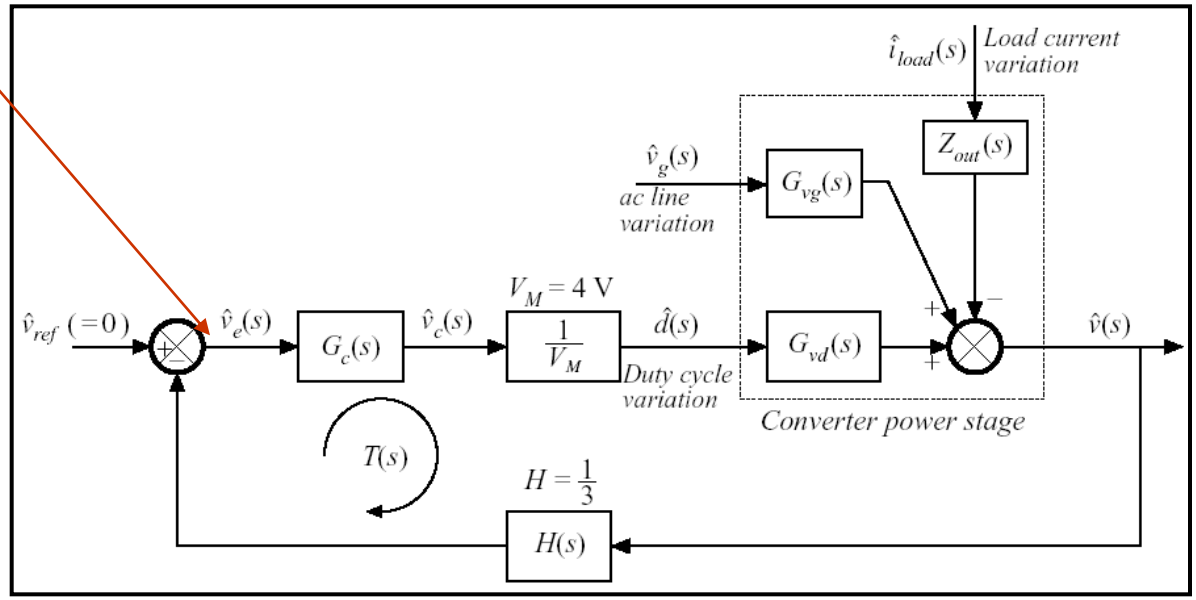


Analyze the uncompensated loop-gain to determine the desired compensator response

$$T_u(s) = \frac{H(s)G_{vd}(s)}{V_M}$$

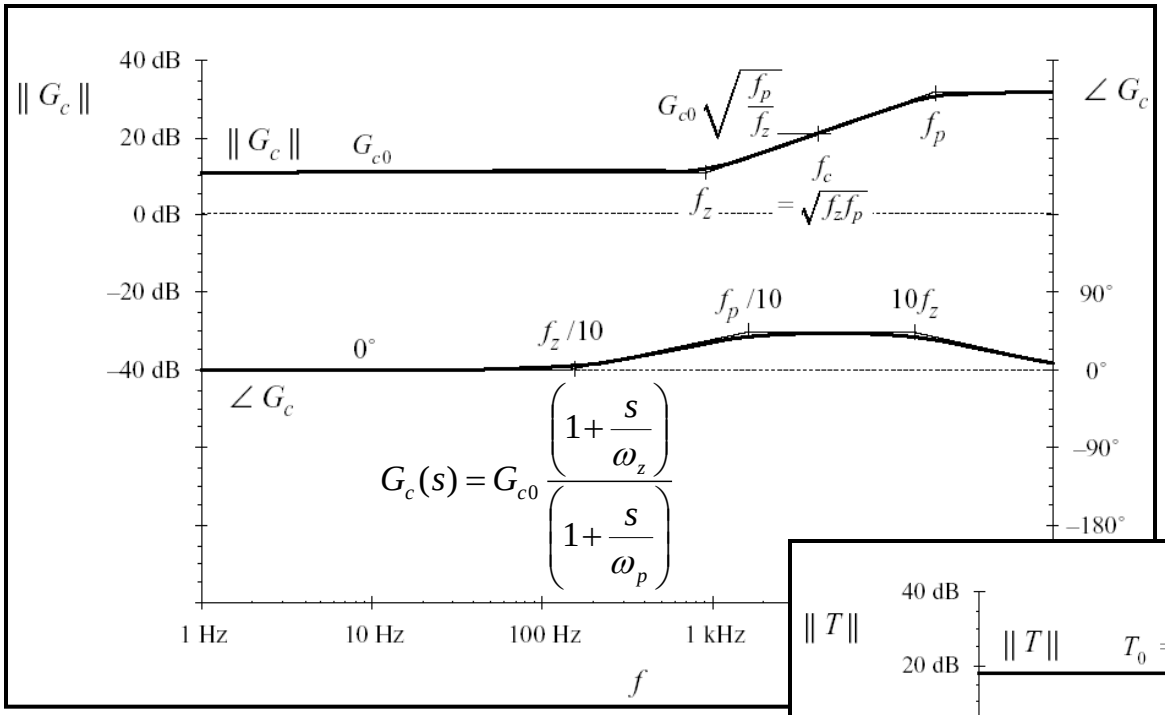
On-Paper Compensator Design Integral Part

$$G_c(s) = \frac{v_c}{v_o} = \frac{\omega_k}{s} \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$$

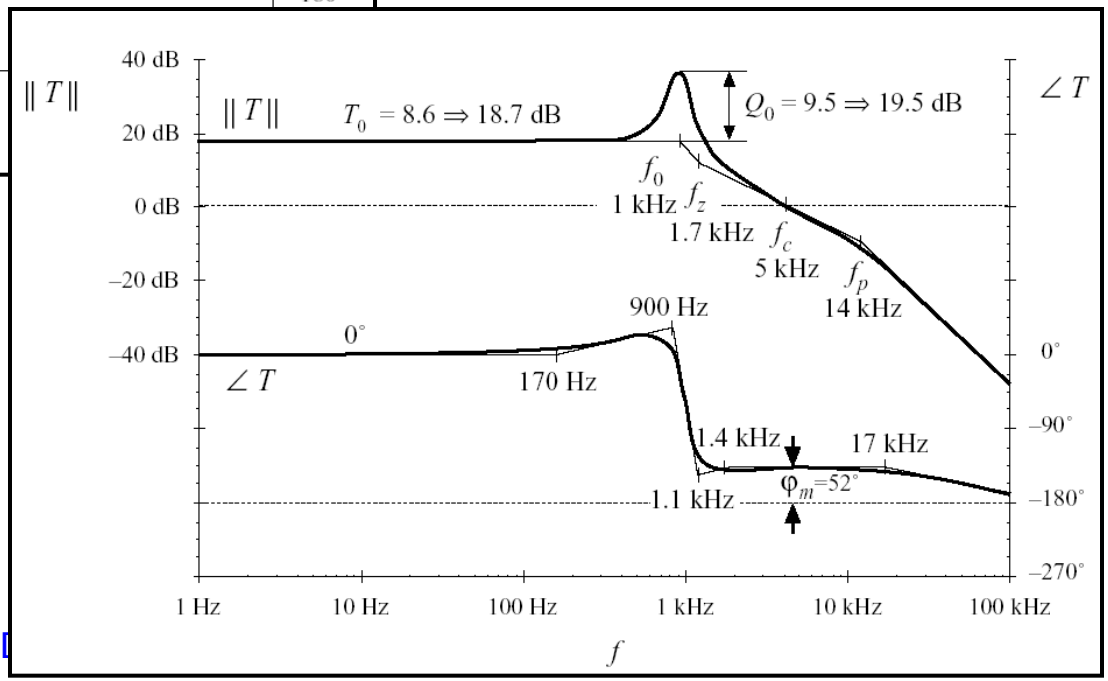


Pole at zero causes infinite DC gain => forces zero error

"On-Paper" Compensator Design PD Part



A typical PD (lead) compensator with pole & zero centered around the crossover frequency f_c and separated according to desired phase improvement



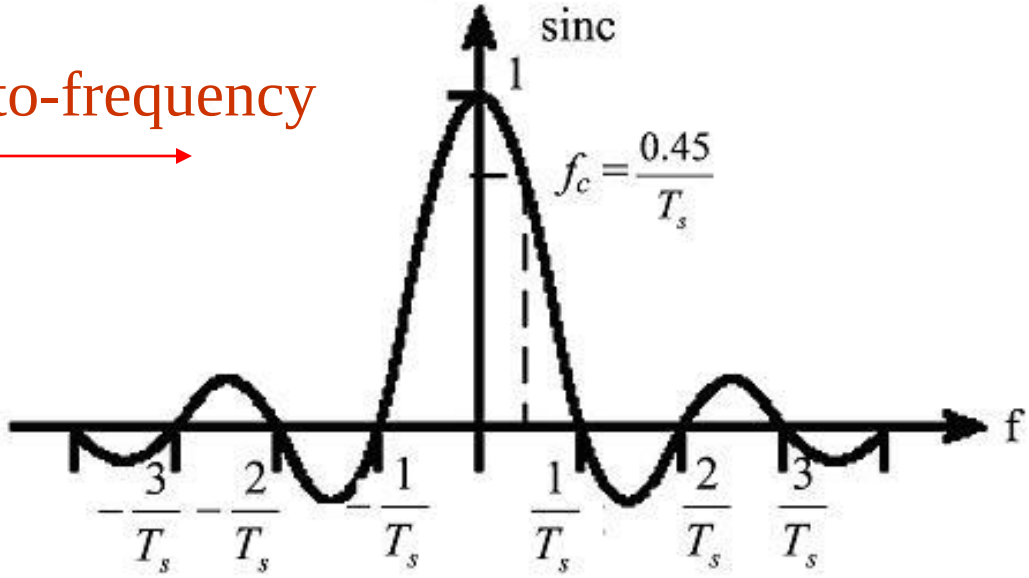
Model Limitations

- *Valid for frequencies much smaller than the switching frequency, approximately up to $f_{sw}/10$. Still very efficient in ripple elimination.*

$$\langle i_L(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt$$

$$\langle v(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{T_s} v(t)dt$$

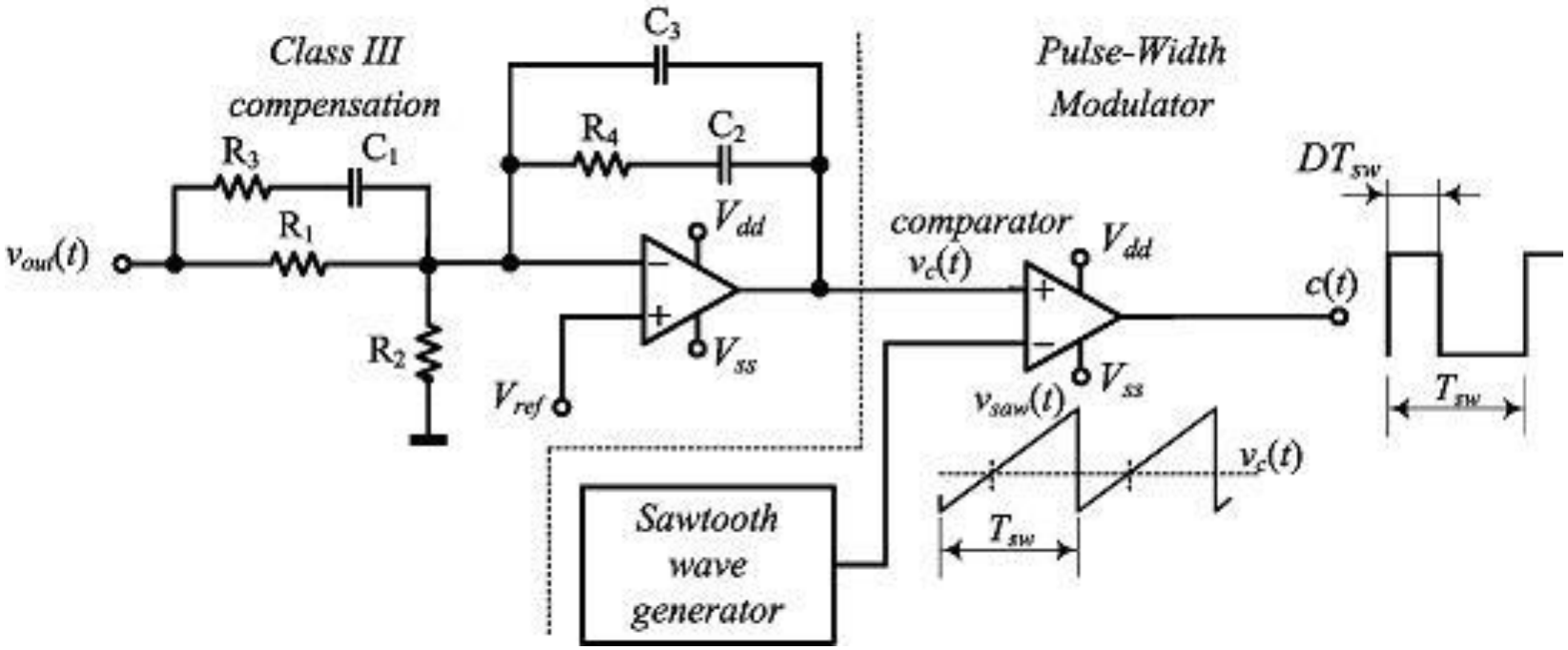
Time-to-frequency



- *The analysis is applicable for small variations around a steady state operating point*

Practical Implementation

Conventional (Analog) Implementation

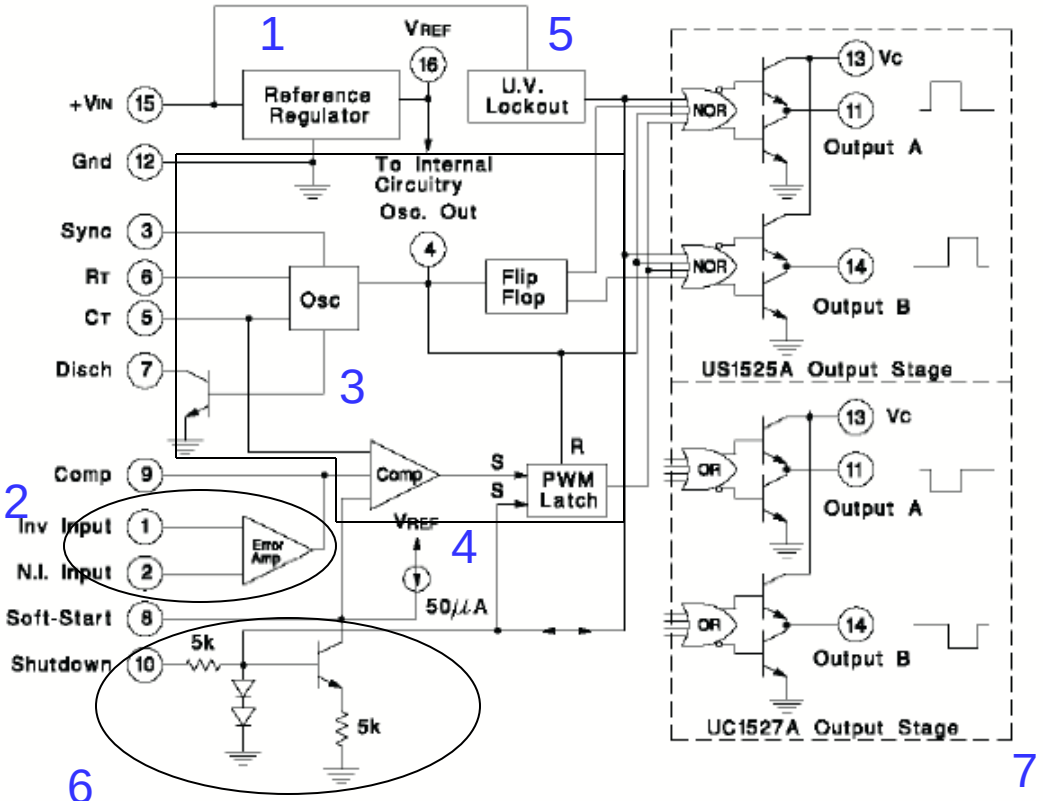


-An analog compensator can be implemented with few Op. Amps, a comparator and several passive components.

- Conventional modeling approach has limited validity, both in terms of frequency and current variations

Analog Controller IC (One of the Very First)

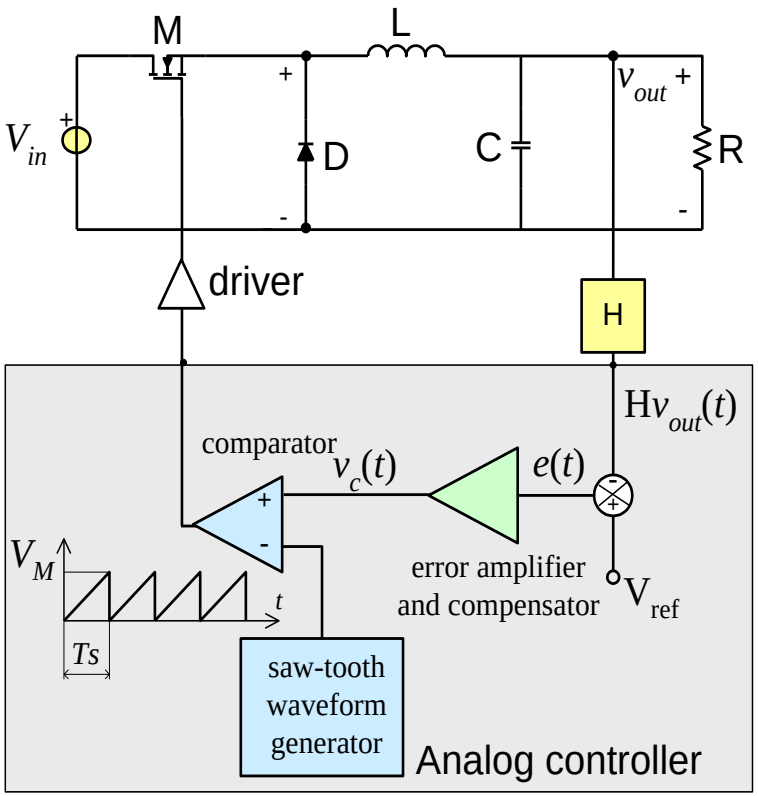
UC3525 – simplified block diagram

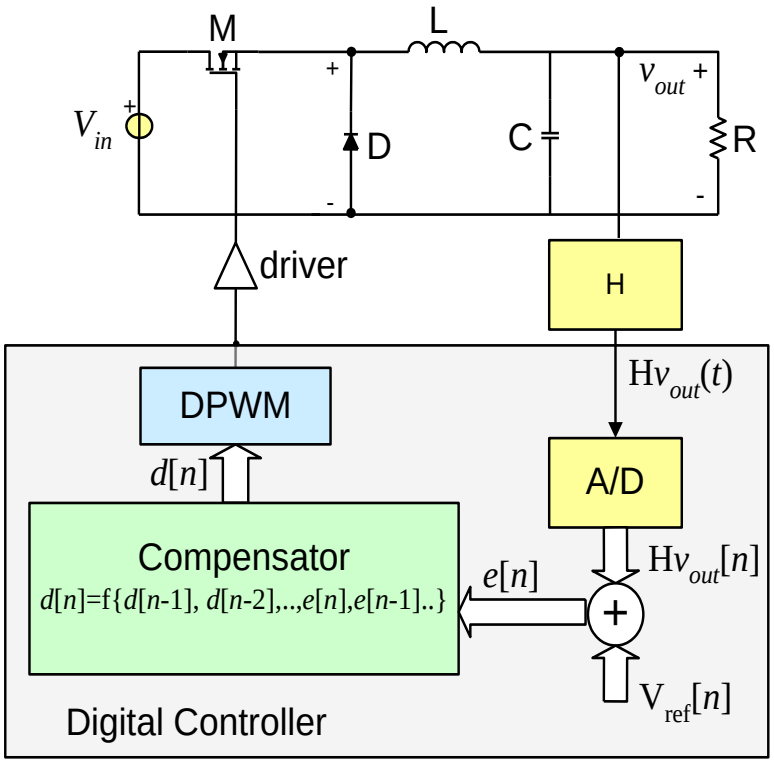


1. Voltage reference 1.7 V, 3 V, or 5.1 V
2. Error amplifier (a compensator can be built around it)
3. Pulse-width modulator
4. Soft start-up
5. Under-voltage protection
6. External shut-down
7. Output stage

Digital Controllers: Design and Practical Implementation

Controller Implementation Analog vs. Digital





Analog Implementation

Digital Implementation

Current Situation and Motivation for Using Digital

- Currently, most o solutions for low and medium SMPS utilize analog controller in higher power kWs digital
- Emerging GaN and SiC devices expected to operate at very high frequencies (existing digital controllers might not be fast enough)
- Motivation for moving/finding high-frequency digital solutions

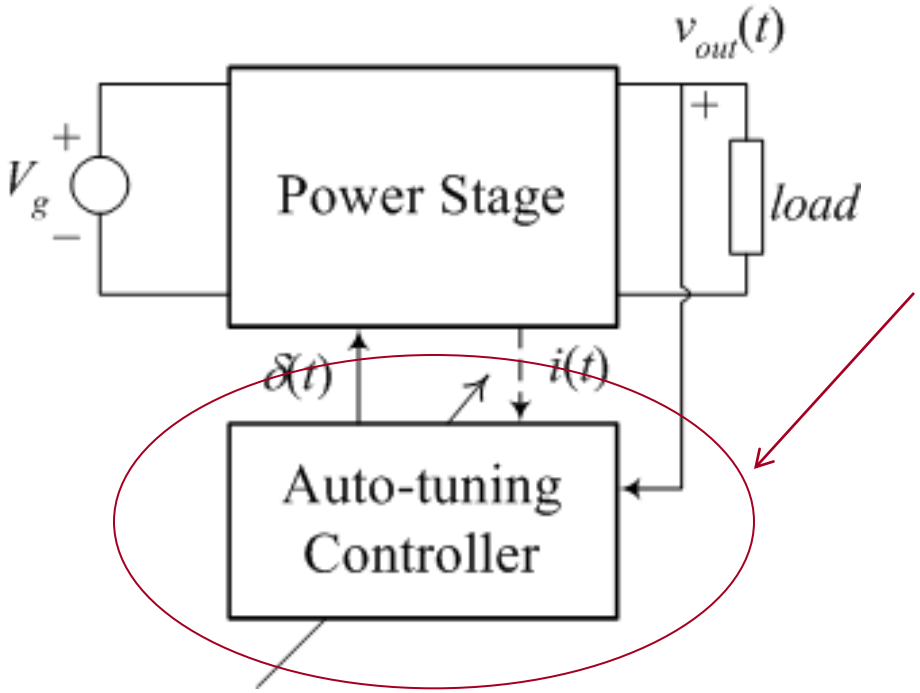
Performance and functionality

- Utilization of auto-tuning and auto learning techniques
- Fault-tolerant operation
- Dynamic response and efficiency improvements

Reduction of fabrication expenses and reliability improvement

- Design portability and fast development
- Monolithic integration on system level

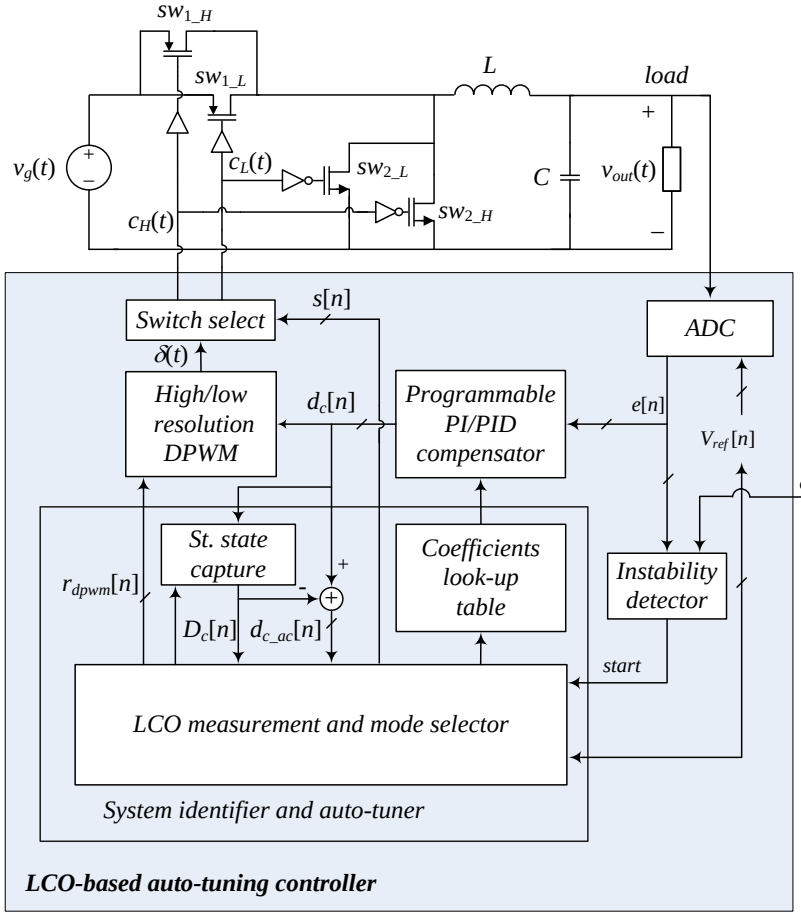
On-Line Auto-Calibration (Plug and Play)

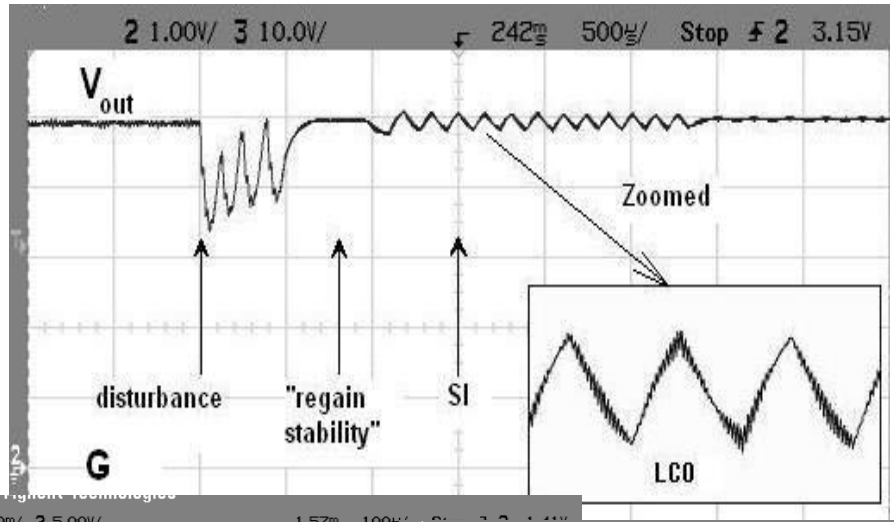


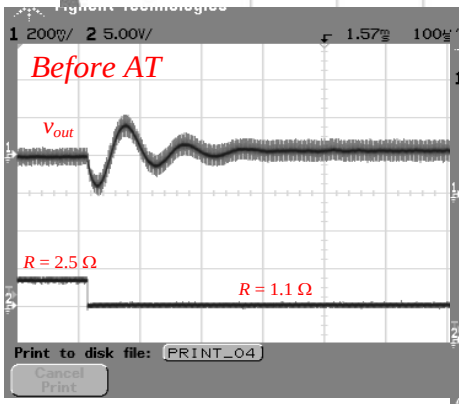
Performs system identification (without direct measurement) and consequent controller self-adjustment

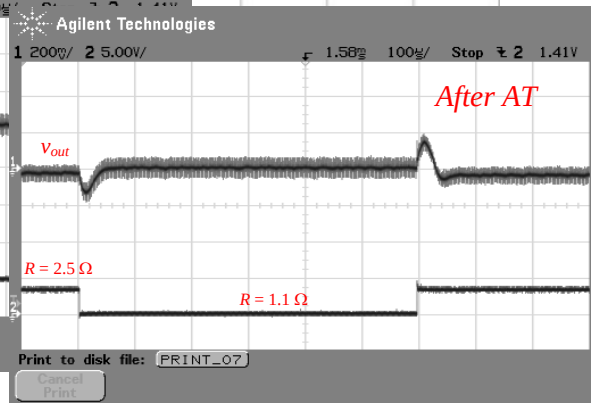
1. *Identification of LC product and on-line compensator adjustments*
2. *Load prediction (estimation) and multi-mode operation improving power processing efficiency*

On-Line Auto-Calibration (Plug and Play)





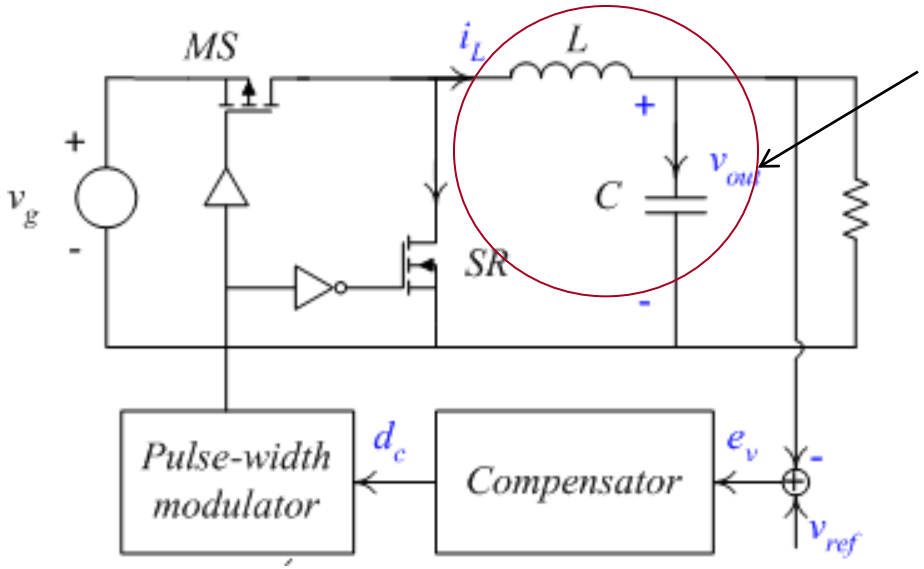




On-line adjustment of controller parameters and multi-mode operation result in better dynamic response and improved efficiency

Ultra-Fast Transient Response

The fastest possible transient response to load changes

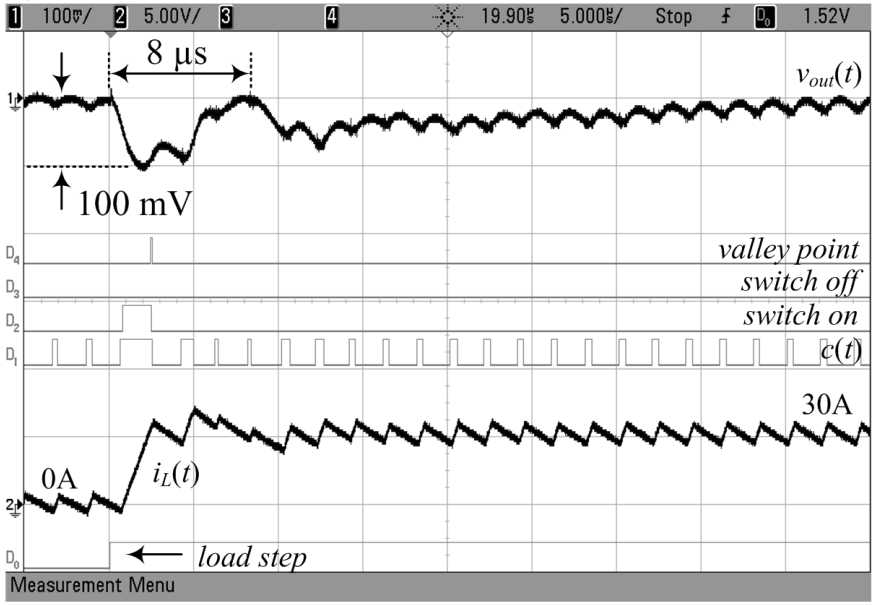


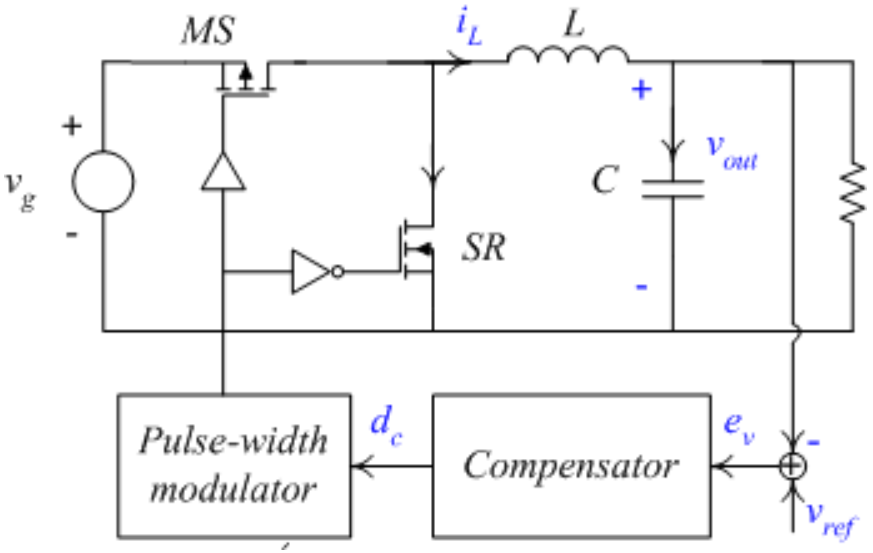
The size depends on the system dynamics (even more than on the ripple)

Utilize digital signal processing to achieve dynamic response approaching physical limitations of a given power stage.

Ultra-Fast Transient Response

The fastest possible transient response to load changes





Utilize digital signal processing to achieve dynamic response approaching physical limitations of a given power stage.

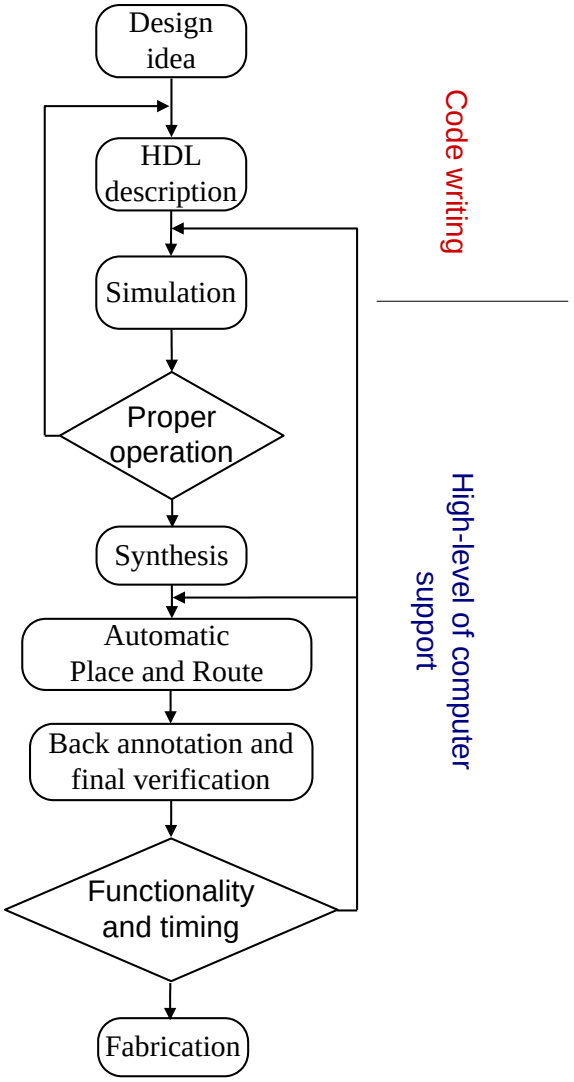
Motivation for Going Digital - Implementation

Implementation (Using HDL)

- Fast development

(highly automated process)

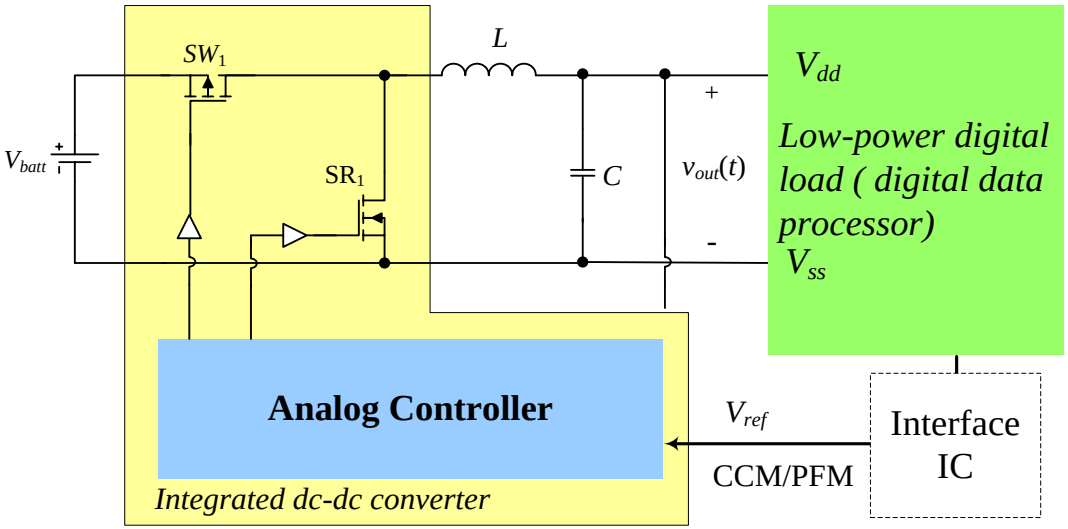
- Design process is independent on implementation technology, temper.



Digital controllers can be more reliable, implemented with a smaller number of components, and developed faster.

Reduction of Fabrication Expenses and Reliability Improvements

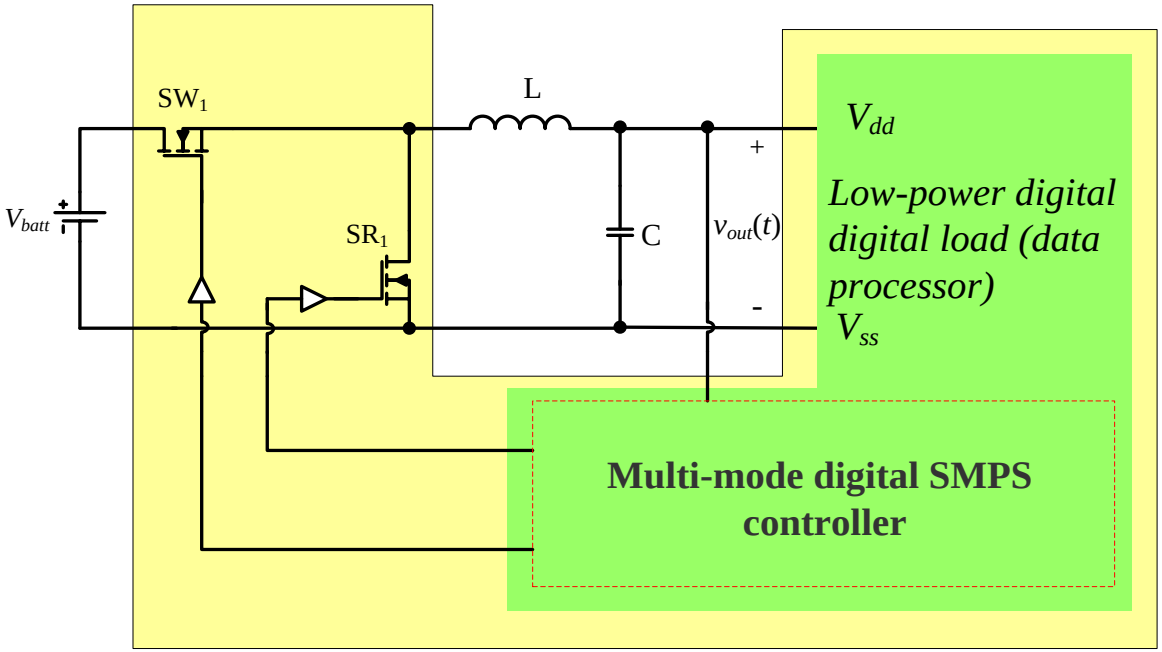
A supply for a digital load/ existing analog solutions



- Three chip solutions implemented in different technologies usually used (low flexibility, significant size, reliability)
- Difficulties in implementing power management techniques such as dynamic and adaptive voltage scaling (AVS/DVS)

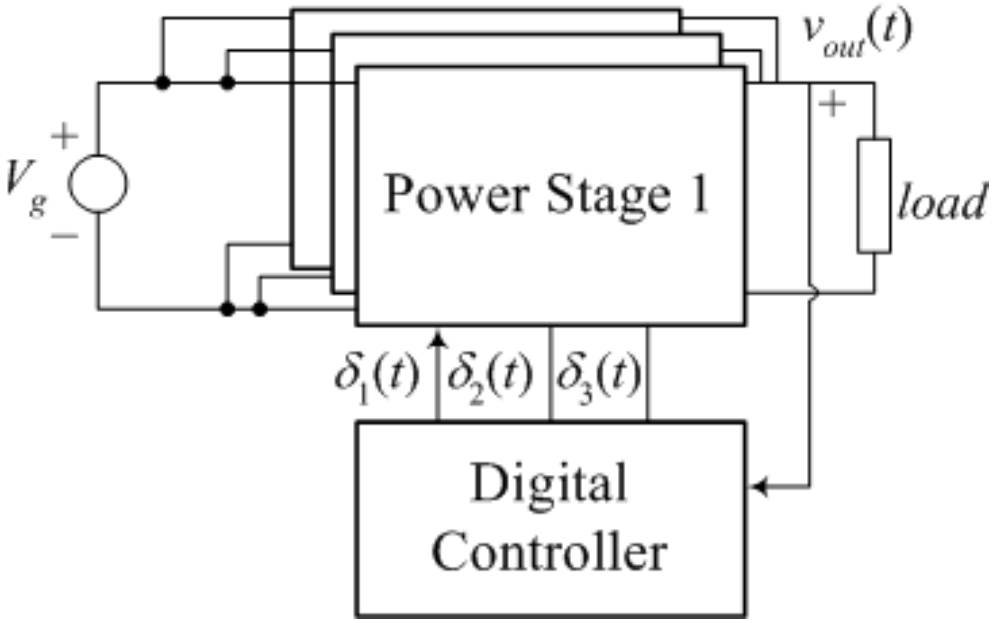
Reduction of Fabrication Expenses and Reliability Improvements

Power supply for a digital load – a possible digital implementation



A single or a two-chip realization possible. Results in reduced size, improved reliability, better synchronization of modern electronic loads and their supply systems.

Remote Current and Temperature Estimation

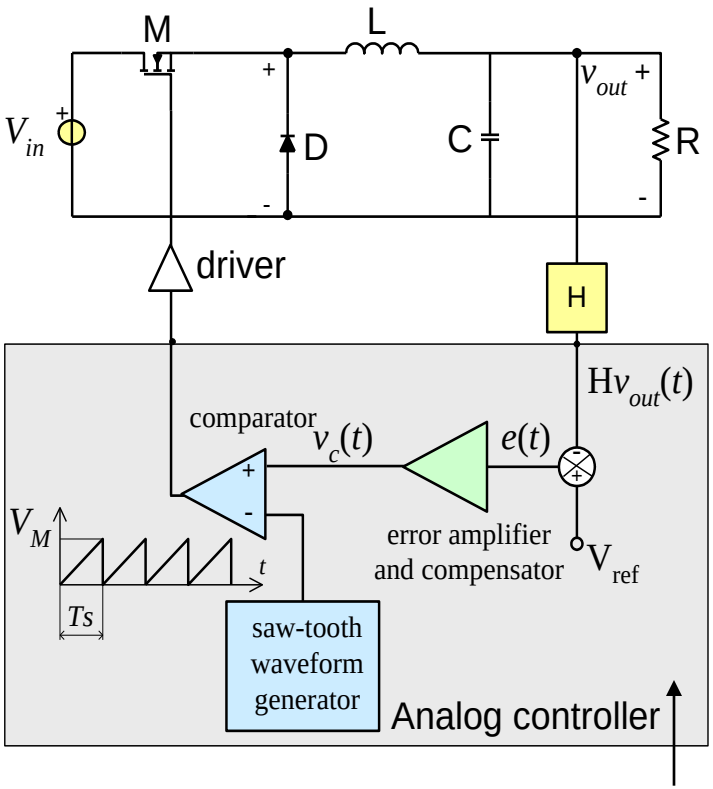


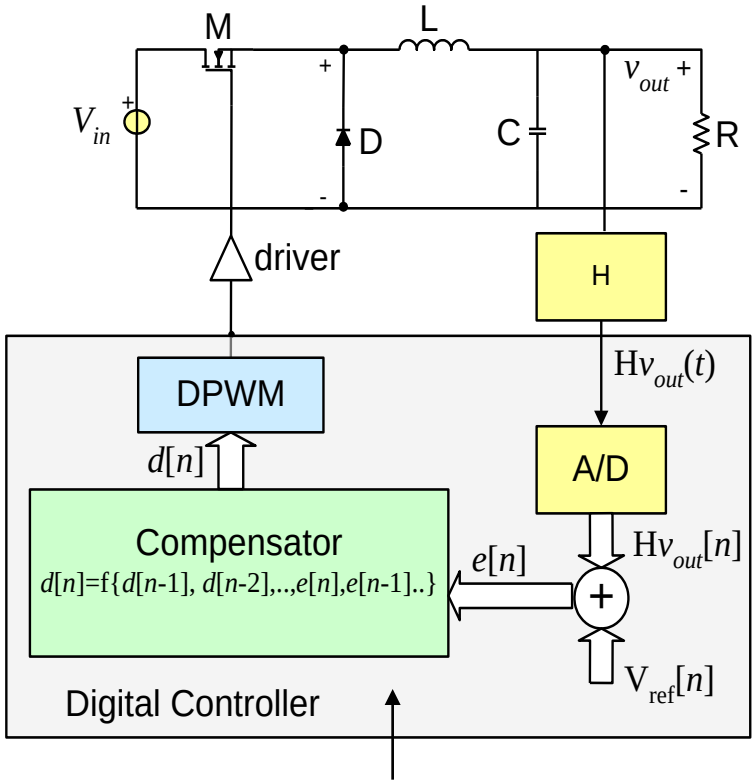
Due to parameter variations currents mismatch occurs

Information contained in digital loop used to provide desired current sharing and temperature monitoring.

The reasons for not going into digital (Design Challenges)

Design Challenges, Analog vs. Digital: Silicon Area

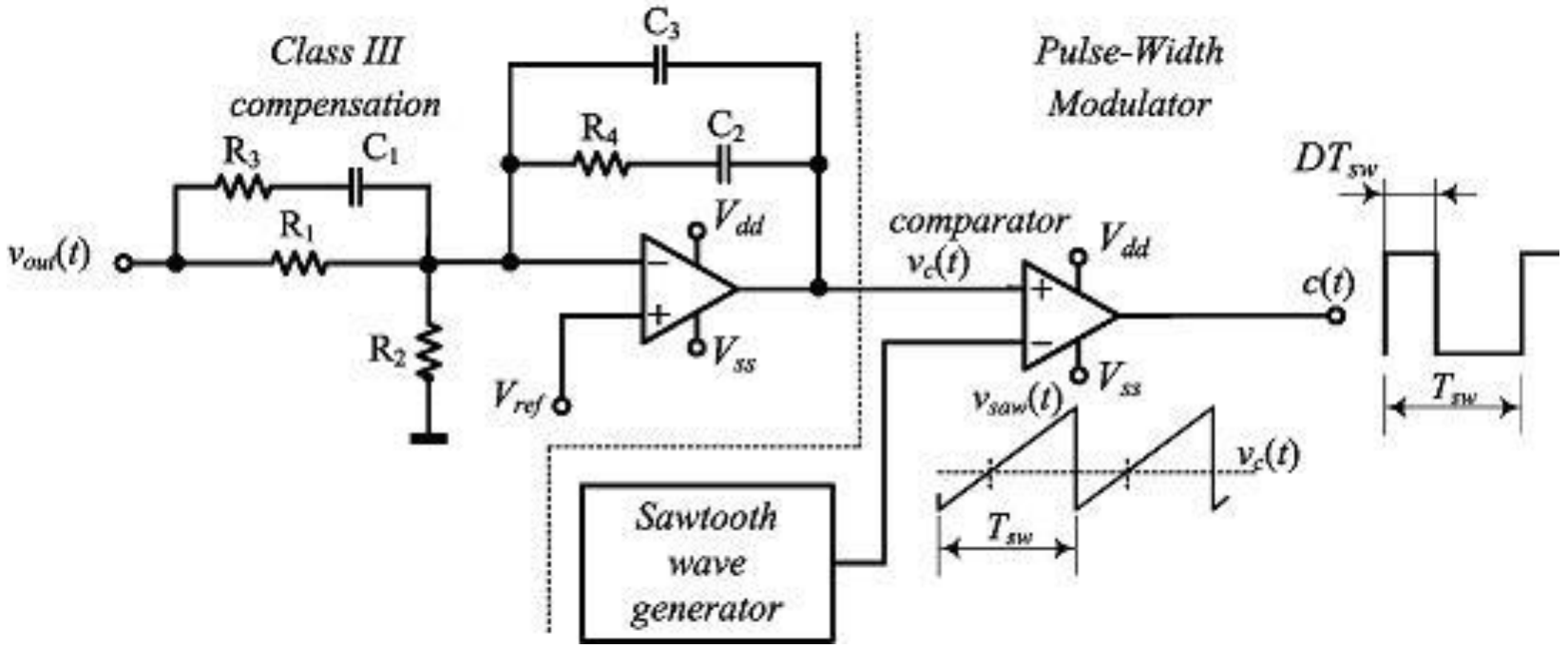




- *Basic control loop can be implemented with a small number of transistors*

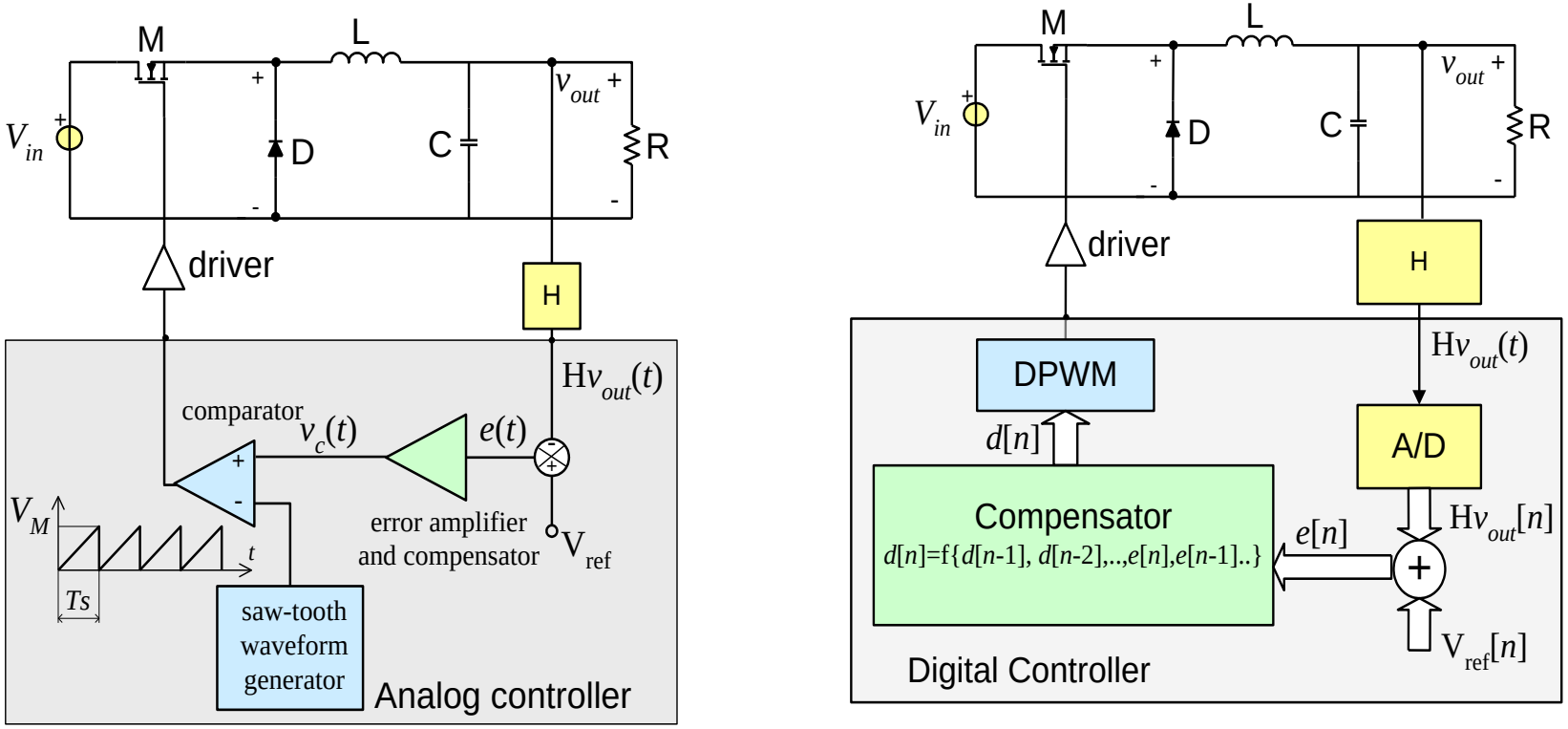
- *Each functional block usually requires larger number of transistors, then the entire analog controller.*

Digital Design Challenges: Silicon Area



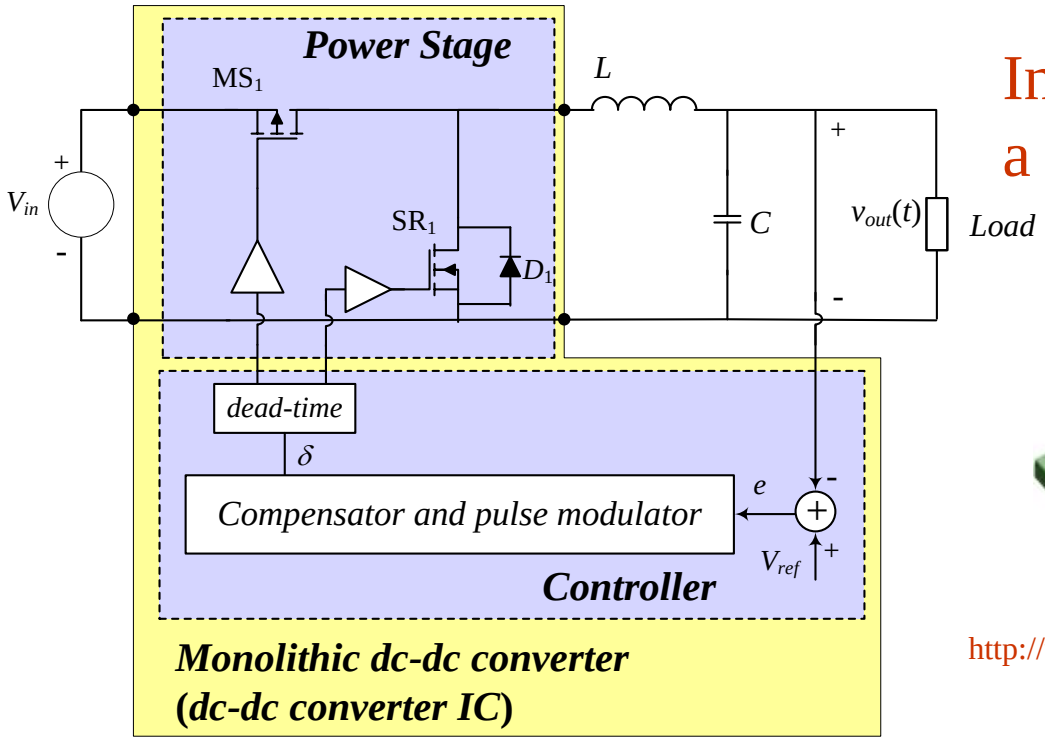
An analog compensator can be implemented with few Op. Amps, a comparator and several passive components

Design Challenges Controller's Power Consumption



- *Power consumption of digital controllers could be much higher (will be addressed soon). In many cases it can exceed that of the supplied load, reducing overall system efficiency and/or limiting maximum switching frequency.*

On-Chip Integrated DC-DC Converter



Integrated analog controller and a 5 MHz / 0.5 W power stage[1]

http://www.ti.com/graphics/folders/partimages/TPS82671.jpg

- For low-power SMPS, existing commercial digital controllers could be too slow and/or take much more power and silicon area than the analog solutions.
- All digital advantages might be lost due to overly expensive and bulky implementation.
- For emerging high frequency SiC/GaN devices the controllers might be slow.

Challenges of Digital Control in Higher Power Applications (Why it is Important to Find HF Hardware Eff. Solutions?)

- *Performance required for operation at high switching frequencies could be accomplished only with a very expensive and power hungry processors and ADCs .*

- *The power consumption of the processors exceeds, often exceeds, 100 W and the total price exceeds $100 (equivalent to the overall price of a 1,4 kW converter at a price of 7c/W – common price taken in industry today)*

- *The limitations of off-shelf (commercial ICs) digital solutions could prevent implementation of digital controllers for high power high frequency systems utilizing new devices (GaN and SiC)*

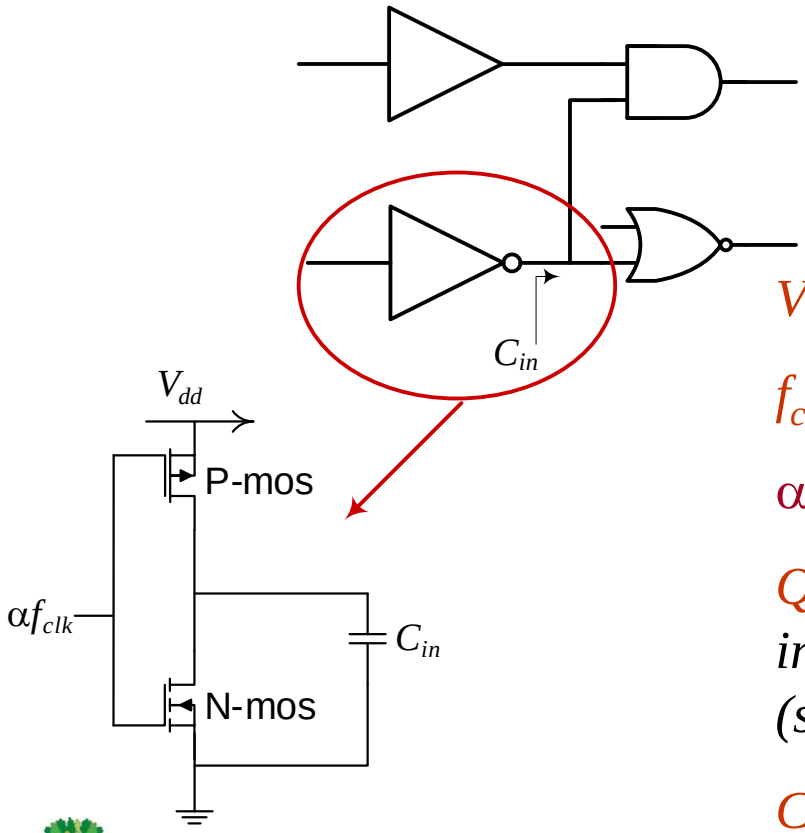
Game Plan

- *Gain a good understanding of the system and its physical limitations*
- *Review basic principles of efficient digital design, analyze minimal hardware requirements,*
- *Review of various digital controller architectures*
- *Going beyond feedback loop realization: i.e. practical implementation of smart controllers*

Sources of Losses and Basic Principles of Power and Silicon Area Efficient Digital Design

Review: Sources of Losses in Digital Circuits

Average losses of a logic gate



CMOS inverter

$$P_{dig} = P_{sw} + P_{sc} + P_{leakage} =$$

$$= \alpha C_{in} V_{dd}^{\ 2} f_{clk} + \alpha Q_{sc} V_{dd} f_{clk} + I_{leakage} V_{dd}$$

V_{dd} – *supply voltage*

f_{clk}- *system clock frequency*

α- *probability that the gate is active*

Q_{sc} – *charge through the device due to instantaneous conduction of both transistors (short circuit current)*

C_{in} – *Capacitive load seen by the inverter*

$I_{leakage}$ – *average leakage current caused by low threshold voltages of modern digital logic*

Review: Basic principles in efficient digital design

Total losses of a digital circuit

$$P_{tot} = \sum_{i=1}^{N} \left(\alpha_i C_i V_{dd}^{\ 2} f_{clk} + \alpha_i Q_{sc} V_{dd} f_{sw} + I_{leakage_i} V_{dd} \right)$$

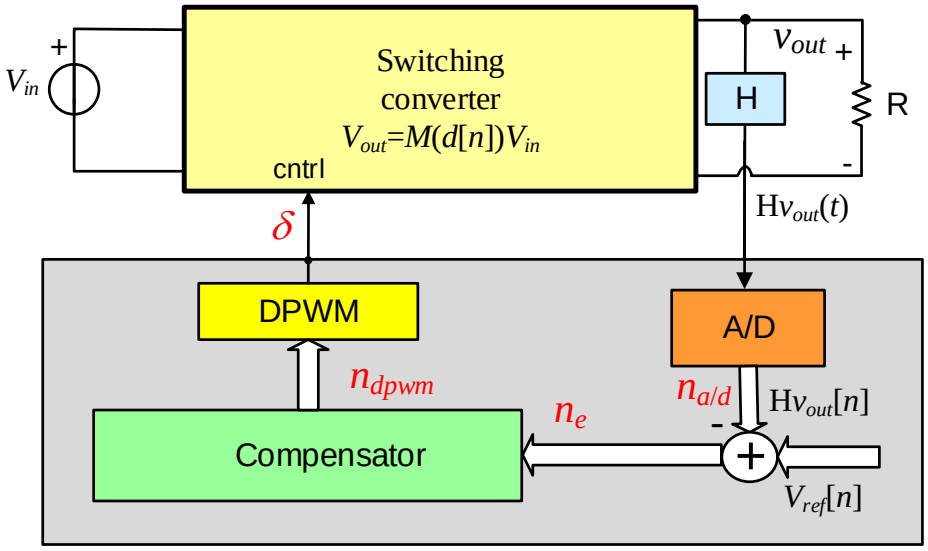
N – *total number of logic gates*

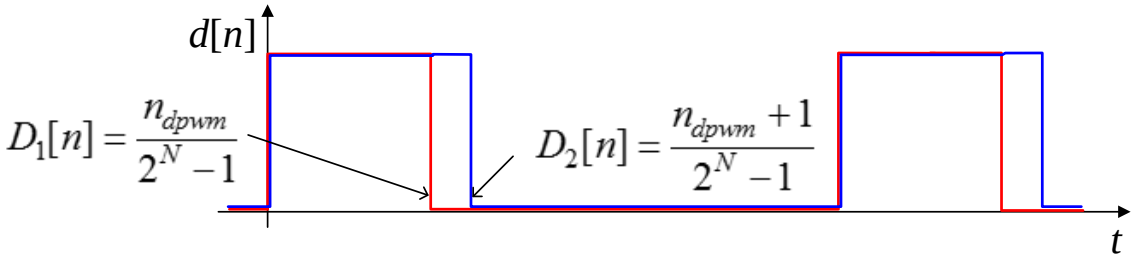
- *Decrease clock frequency*
- *Decrease the total number of logic gates*
- *Minimize the gates activity or number of gates switching frequently*

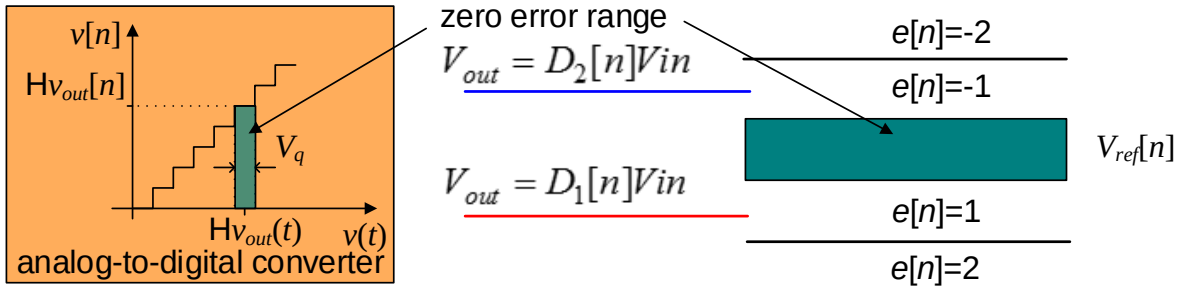
These 3 rules will be used throughout the whole design process.

Limit Cycling, Quantization Effects and Analysis of Minimal Hardware Requirements

Minimal Hardware Requirements (DPWM & A/D)

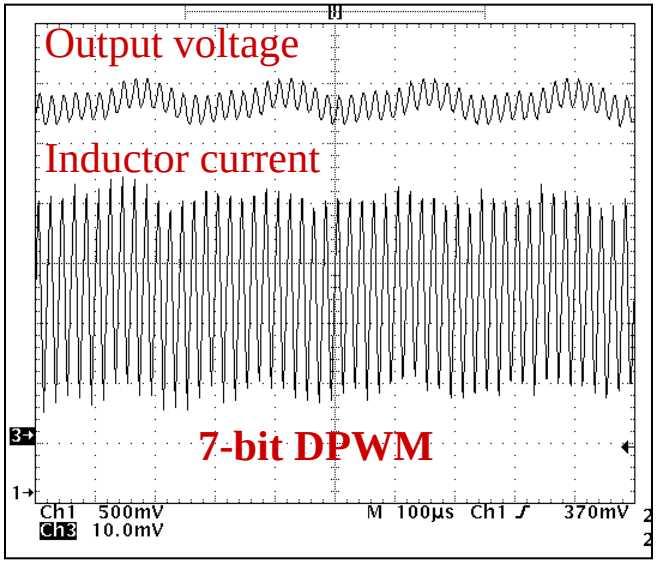




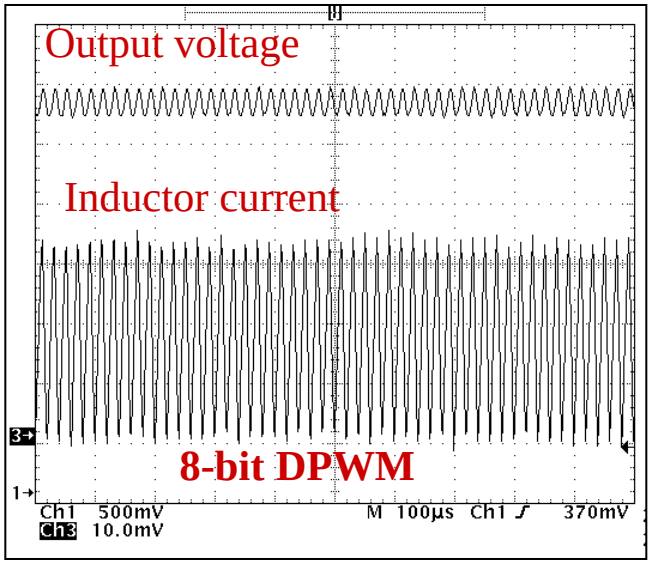


When the resolution of the DPWM is too coarse compared to that of the ADC limit-cycling oscillations can occur

Minimal resolution of the DPWM



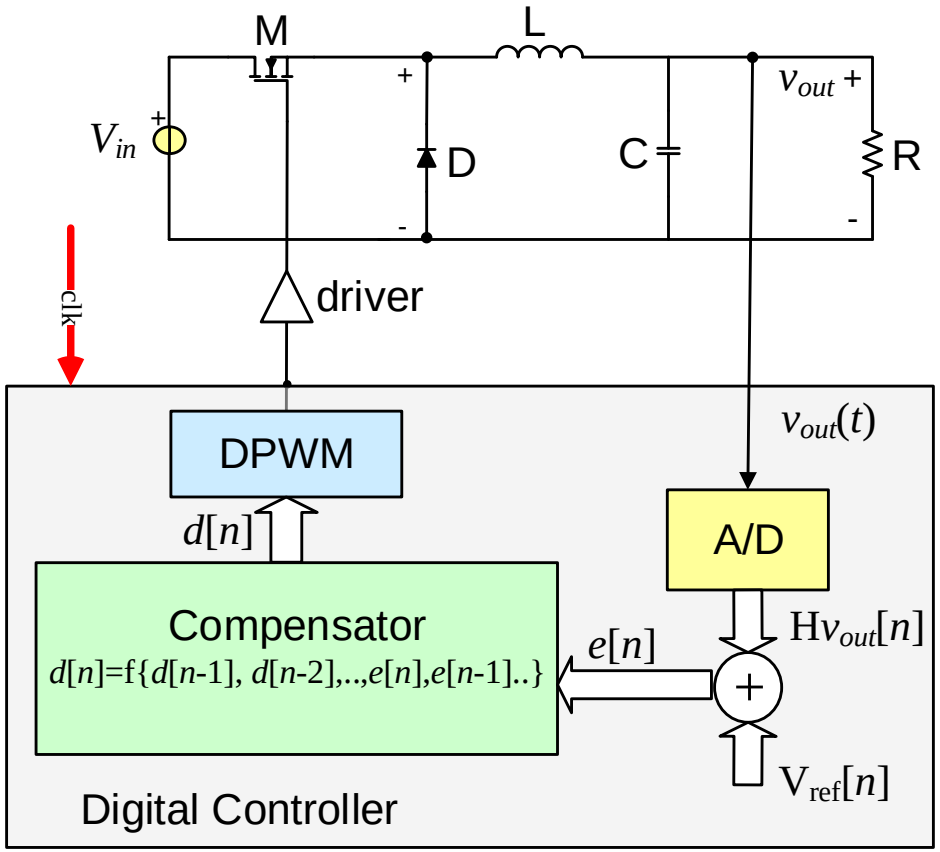
Insufficient DPWM resolution



Minimal DPWM resolution satisfied

- *Steady state condition for the LCO elimination*
- *Dynamic conditions*

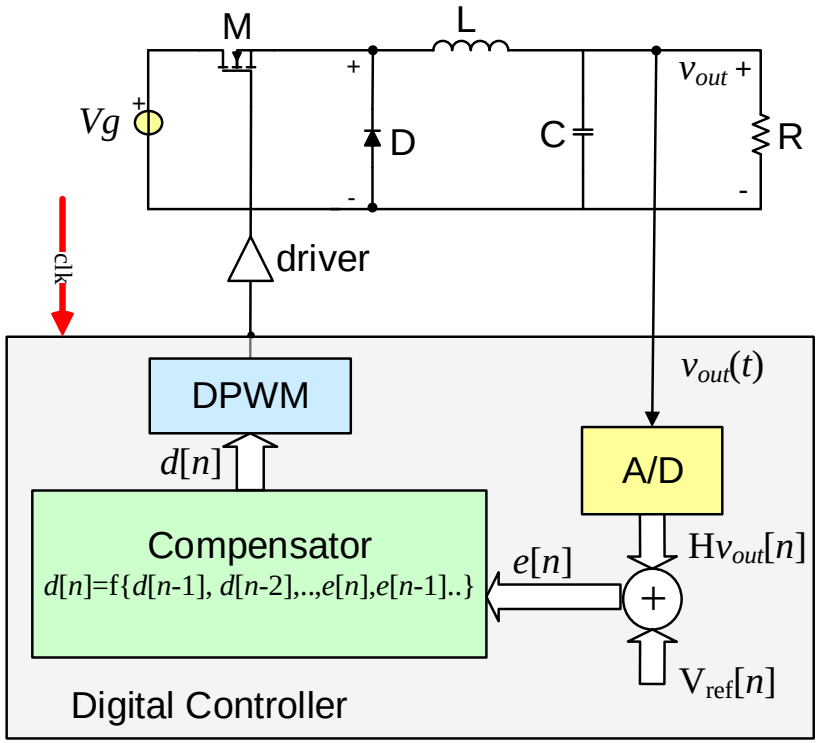
Steady-State Conditions for No Limit Cycling

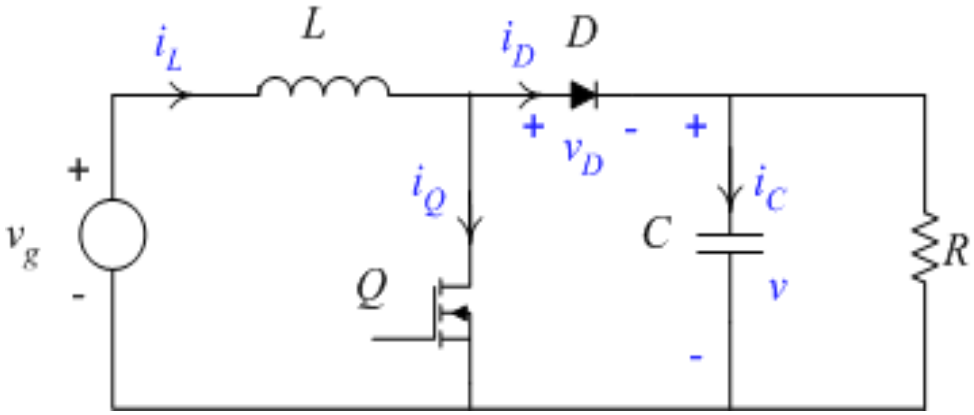


A necessary condition to avoid the limit cycle oscillation is that the change in the output voltage caused by one LSB change in the duty ratio has to be smaller than the quantization step of the ADC V_{q_ADC}:

$$V_{q\_ADC} > V_g \cdot \Delta M(D)$$

Steady-State Conditions for No Limit Cycling





Boost case:

$$V_{q\_ADC} > \frac{V_g}{1-(D+\Delta D_{LSB})} - \frac{V_g}{1-D}$$

$$\Delta D = \frac{1}{2^{Ndpwm}}$$

Buck case:

$$V_{q\_ADC} > V_{in}\ (D+\Delta D_{LSB}) - V_g\ D$$

These conditions need to be satisfied for the first case operating conditions in terms of the quantization steps

Steady-State Conditions for No Limit Cycling

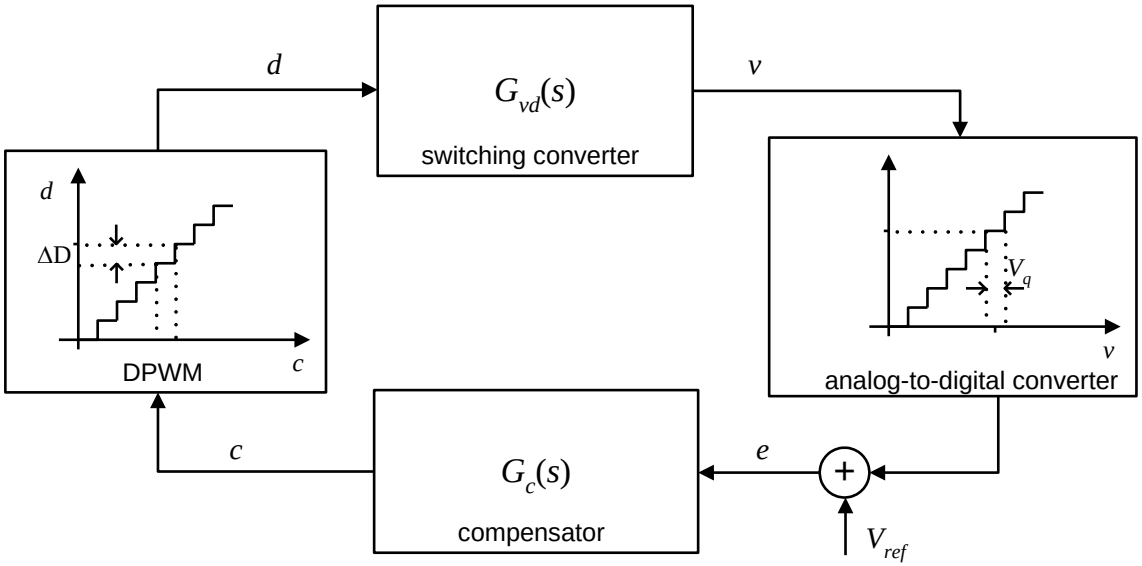
MINIMUM RESOLUTION OF DPWM FOR TYPICAL CONVERTERS

Type of converter/ Conversion ratio M(D)	Minimal resolution of DPWM	
Buck M(D)=D	$\text{int}\left[n_{a/d}+\log_2\left(\frac{V_{ref}}{V_{\max_{a/d}}\cdot D}\right)\right]$	$\text{int}\left[\log_2\left(\frac{V_{ref}}{D\cdot\Delta V_q}\right)\right]$
Boost M(D)=1/(1-D)	$\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{V_{\max_{a/d}}}\cdot 2^{n_{a/d}}+1\right)\right)\right]$	$\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{\Delta V_q}+1\right)\right)\right]$
Buck-boost, Cuk, sepic M(D)=D/(1-D)	$\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{DV_{\max_{a/d}}}\cdot 2^{n_{a/d}}+1\right)\right)\right]$	$\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{D\cdot\Delta V_q}+1\right)\right)\right]$
Flyback M(D)=nD/(1-D)	$\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{DV_{\max_{a/d}}}\cdot 2^{n_{a/d}}+1\right)\right)\right]$	$\text{int}\left[\log_2\left(\frac{1}{1-D}\left(\frac{V_{ref}}{D\cdot\Delta V_q}+1\right)\right)\right]$
Forward M(D)=nD	$\text{int}\left[n_{a/d}+\log_2\left(\frac{V_{ref}}{V_{\max_{a/d}}\cdot D}\right)\right]$	$\text{int}\left[\log_2\left(\frac{V_{ref}}{D\cdot\Delta V_q}\right)\right]$
Watkins-Johnson M(D)=(2D-1)/D	$\text{int}\left[\log_2\left(\frac{1}{D}\left(\frac{V_{\max_{a/d}}}{V_{ref}}\cdot\frac{2^{n_{a/d}}}{2D-1}-1\right)\right)\right]$	$\text{int}\left[\log_2\left(\frac{1}{D}\left(\frac{V_{ref}}{(2D-1)\cdot\Delta V_q}-1\right)\right)\right]$

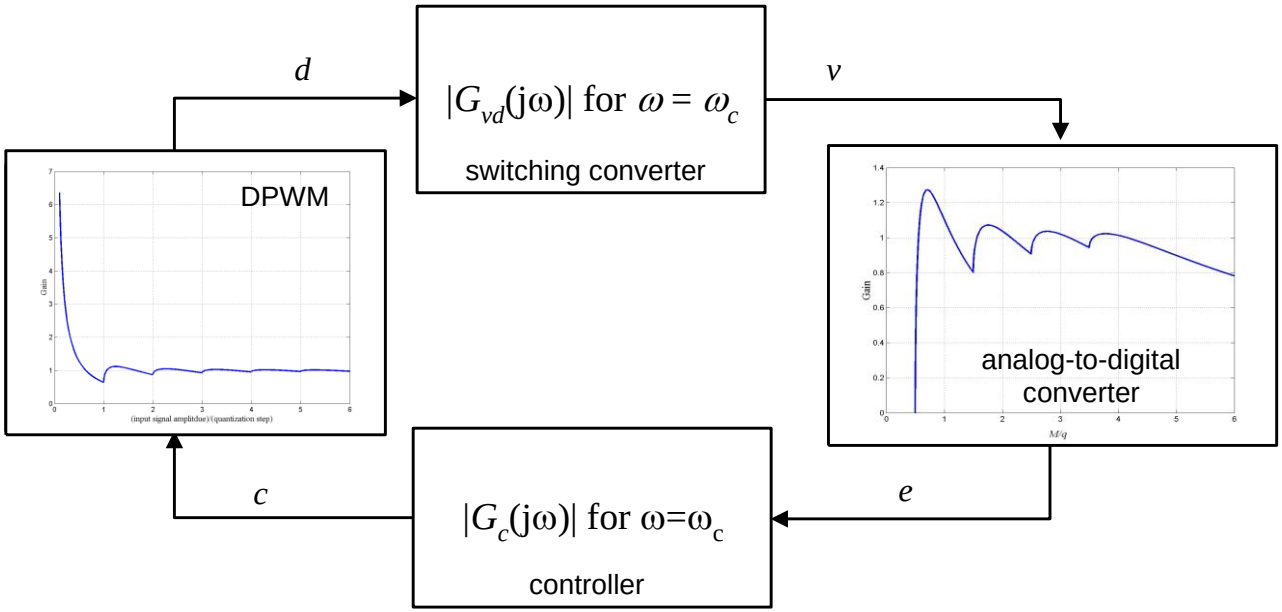
Dynamic Conditions for No Limit Cycling

- *Even when the conditions given in the table are satisfied, limit-cycle oscillations can still appear. Due to extra gain introduced with nonlinear quantization effects in the ADC and the DPWM.*

- *In order to explain this limit cycling mechanisms, an analysis based on the describing functions can be applied*



Dynamic Conditions for No Limit Cycling



Dynamic condition for no limit cycling

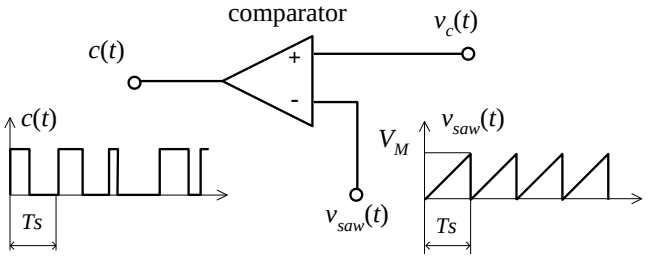
$$\frac{\Delta V_{q\_ADC}}{2} > \frac{2\left|G_{vd}\left(j\omega_{LC}\right)\right|}{\pi}\Delta V_{DPWM}$$

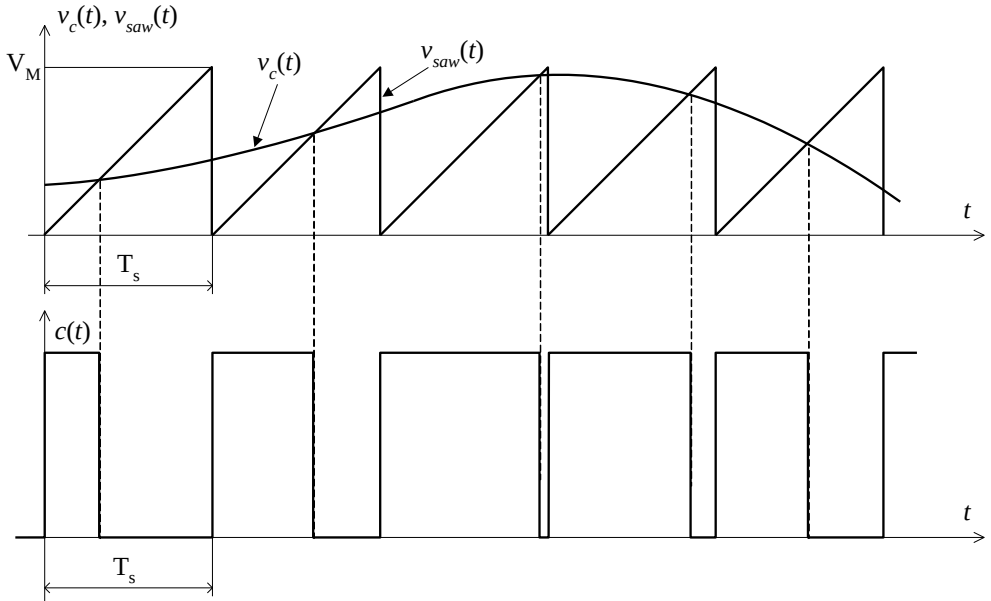
$$\Delta V_{q\_ADC} > \frac{4}{\pi}\left|G_{vd}\left(j\omega_{LC}\right)\right|\Delta V_{DPWM}$$

Design/Selection of Power & Area Efficient Basic Functional Blocks

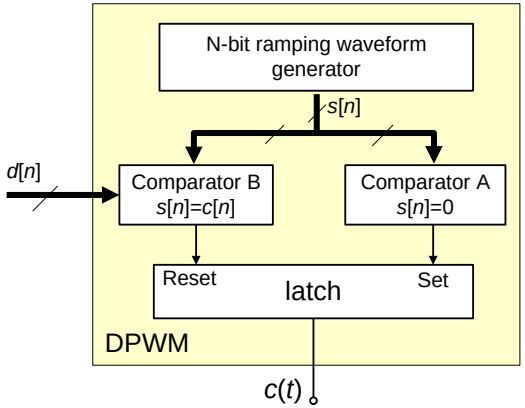
Digital Pulse-Width Modulator (DPWM) Architectures

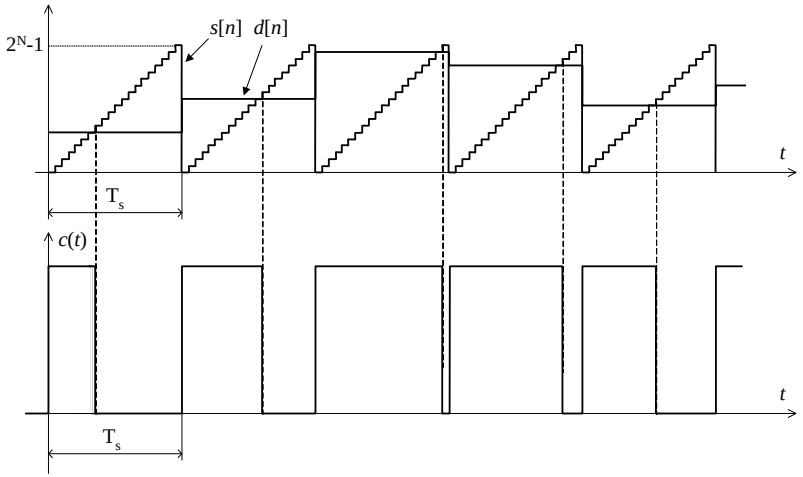
Analog pulse-width modulator and DPWM





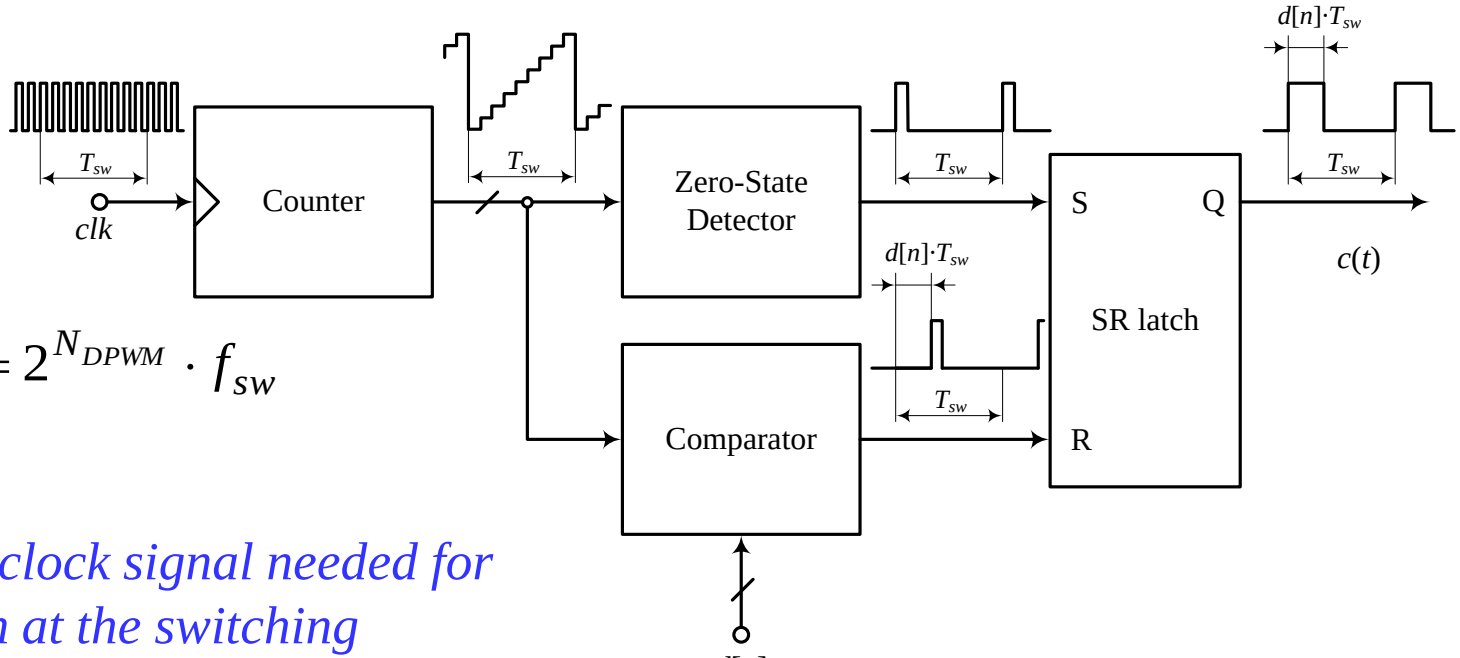
Analog PWM





Digital Pulse Width Modulator (DPWM)

DPWM: Traditional Counter-Based Architecture



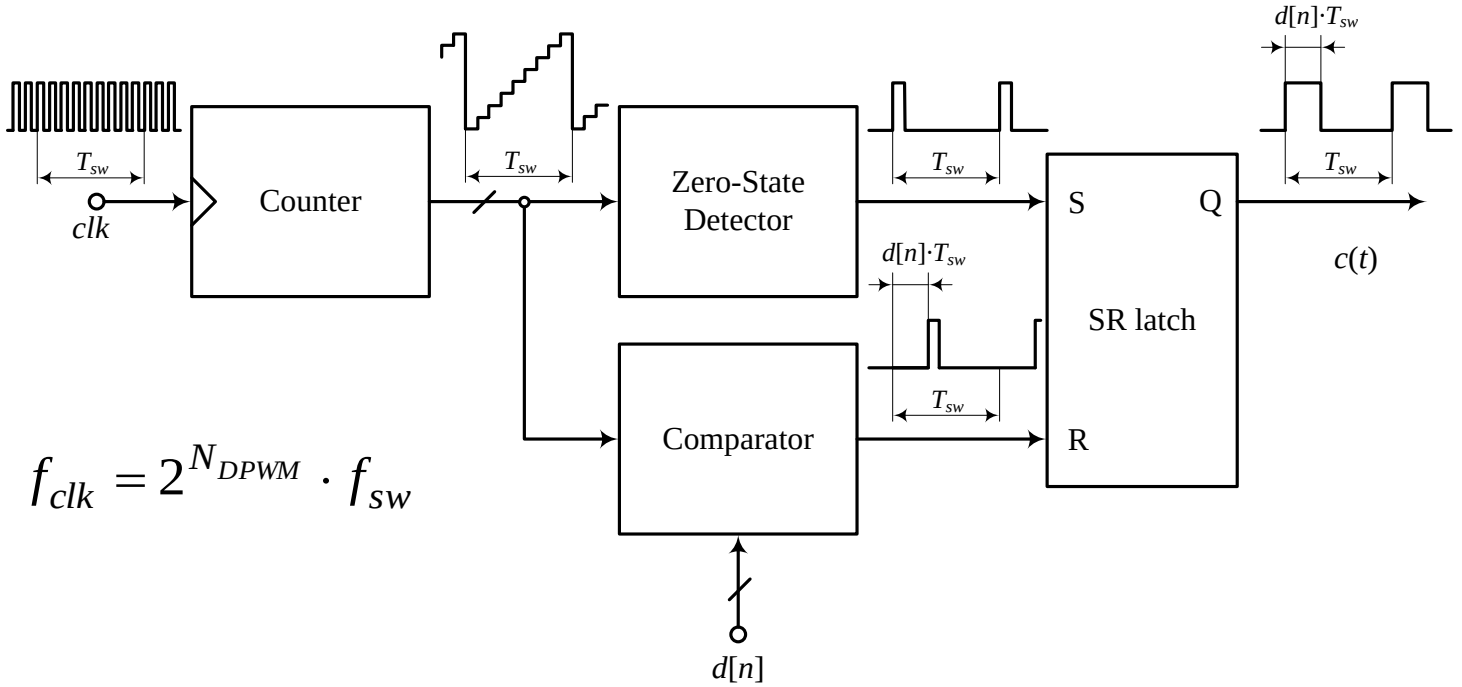
$$f_{clk} = 2^{N_{DPWM}} \cdot f_{sw}$$

A 4 GHz clock signal needed for operation at the switching frequency of 4 MHz with 10-bit resolution. For 12-bit, 16 GHz clock would be required.

$$P_{tot} = \sum_{i=1}^{N} \left(\alpha_i C_i V_{dd}^{\,2} f_{clk} + \alpha_i Q_{sc} V_{dd} f_{sw} + I_{leakage_i} V_{dd} \right)$$

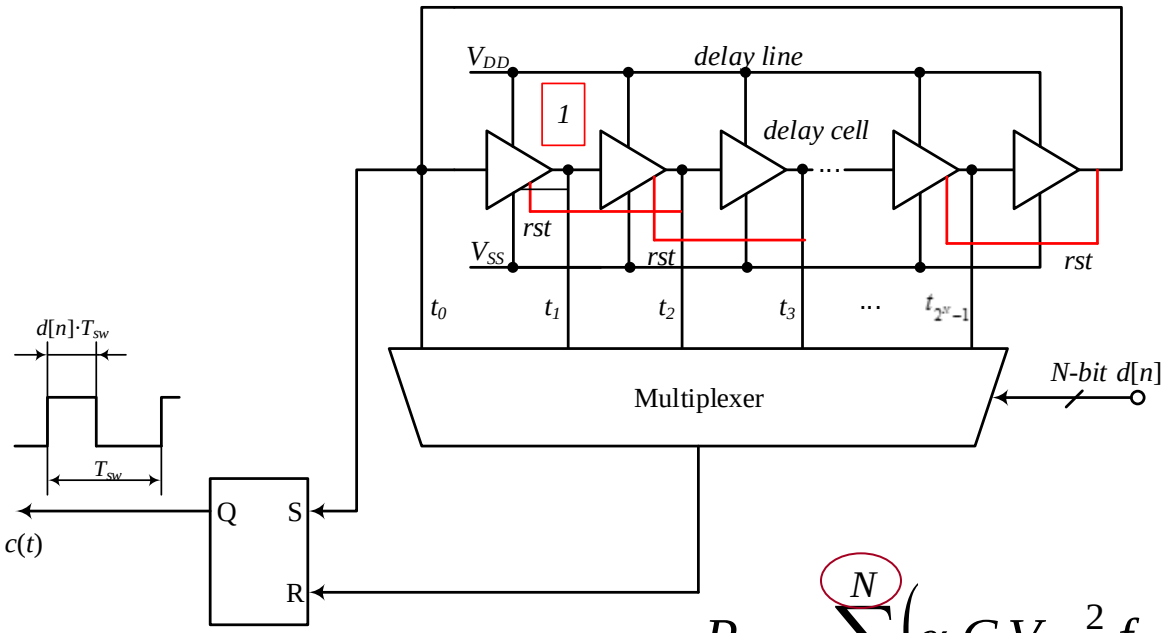
- *High power consumption and definitely challenging IC design*
- *Top of the line processors don't have the ability to produce high frequency high resolution DPWM signals*

DPWM: Traditional Counter-Based Architecture



Also the reason for that the resolution of DPWM in commercial products reduces as the switching frequency increases (for example 10 bit at 50 kHz and 8 bit at 200 kHz) => Tradeoff between resolution and frequency

DPWM: Ring Oscillator Based Architecture

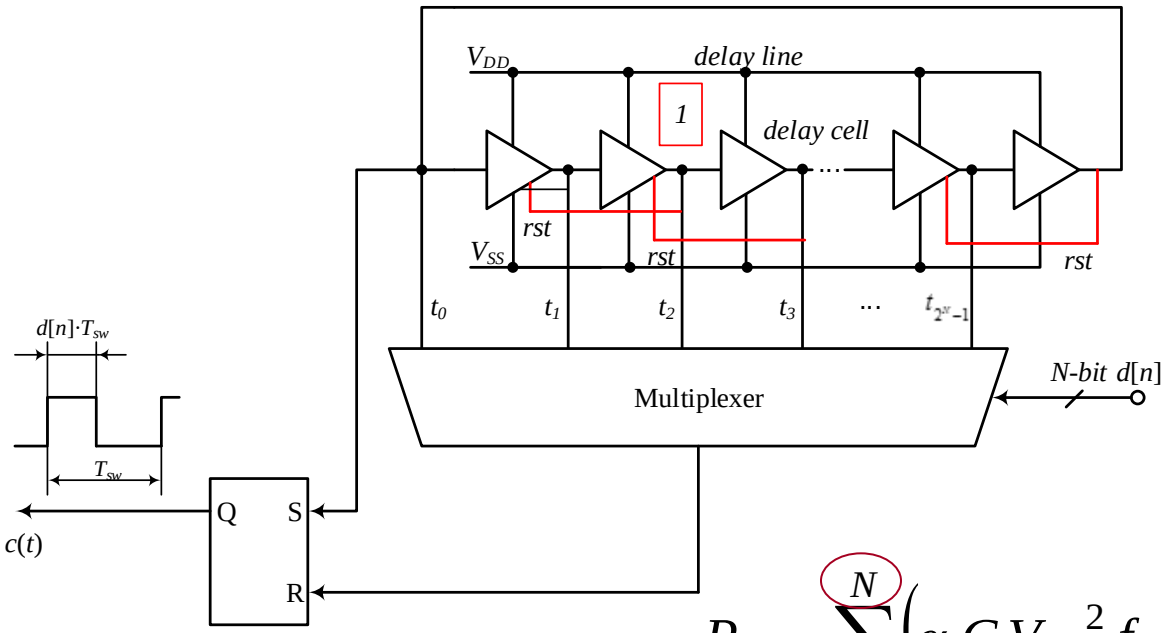


$$N_{delay\_el} = 2^{N_{DPWM}}$$

$$P_{tot} = \sum_{i=1}^{N} \left(\alpha_i C_i V_{dd}^{\,2} f_{clk} + \alpha_i I_{sc} V_{dd} + I_{leakage_i} V_{dd} \right)$$

- *Low power consumption*
- *Requires relatively large silicon area*
- *Nonlinearity (non-monotonic) problems could occur*

DPWM: Ring Oscillator Based Architecture



$$N_{delay\_el} = 2^{N_{DPWM}}$$

$$P_{tot} = \sum_{i=1}^{N} \left(\alpha_i C_i V_{dd}^{\,2} f_{clk} + \alpha_i I_{sc} V_{dd} + I_{leakage_i} V_{dd} \right)$$

- *Low power consumption*
- *Requires relatively large silicon area*
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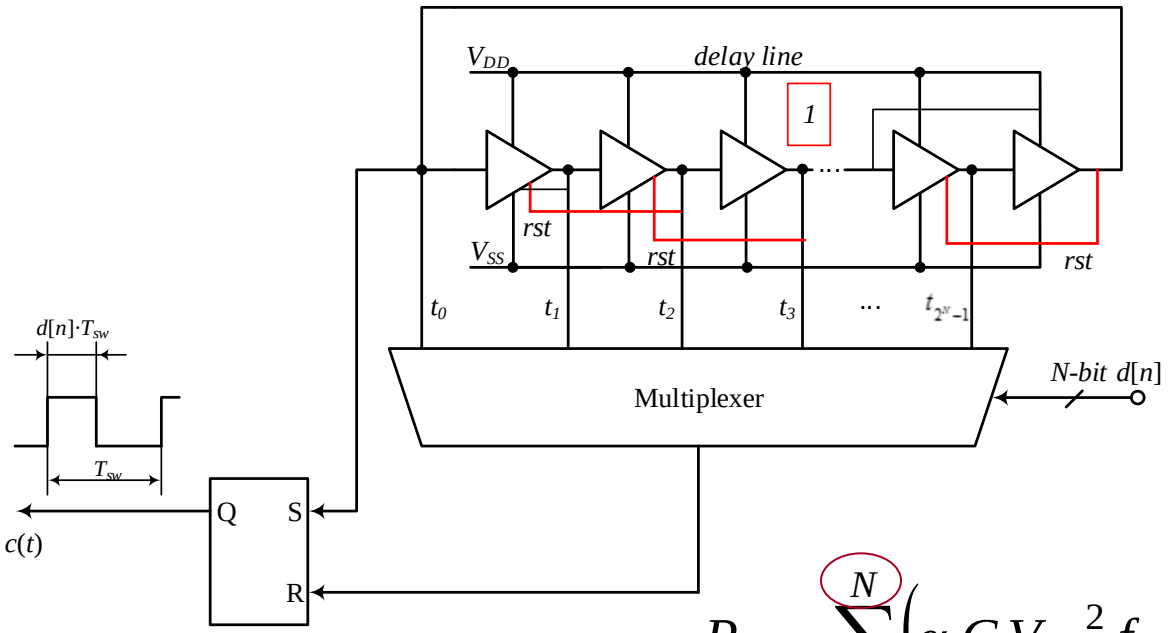
DPWM: Ring Oscillator Based Architecture

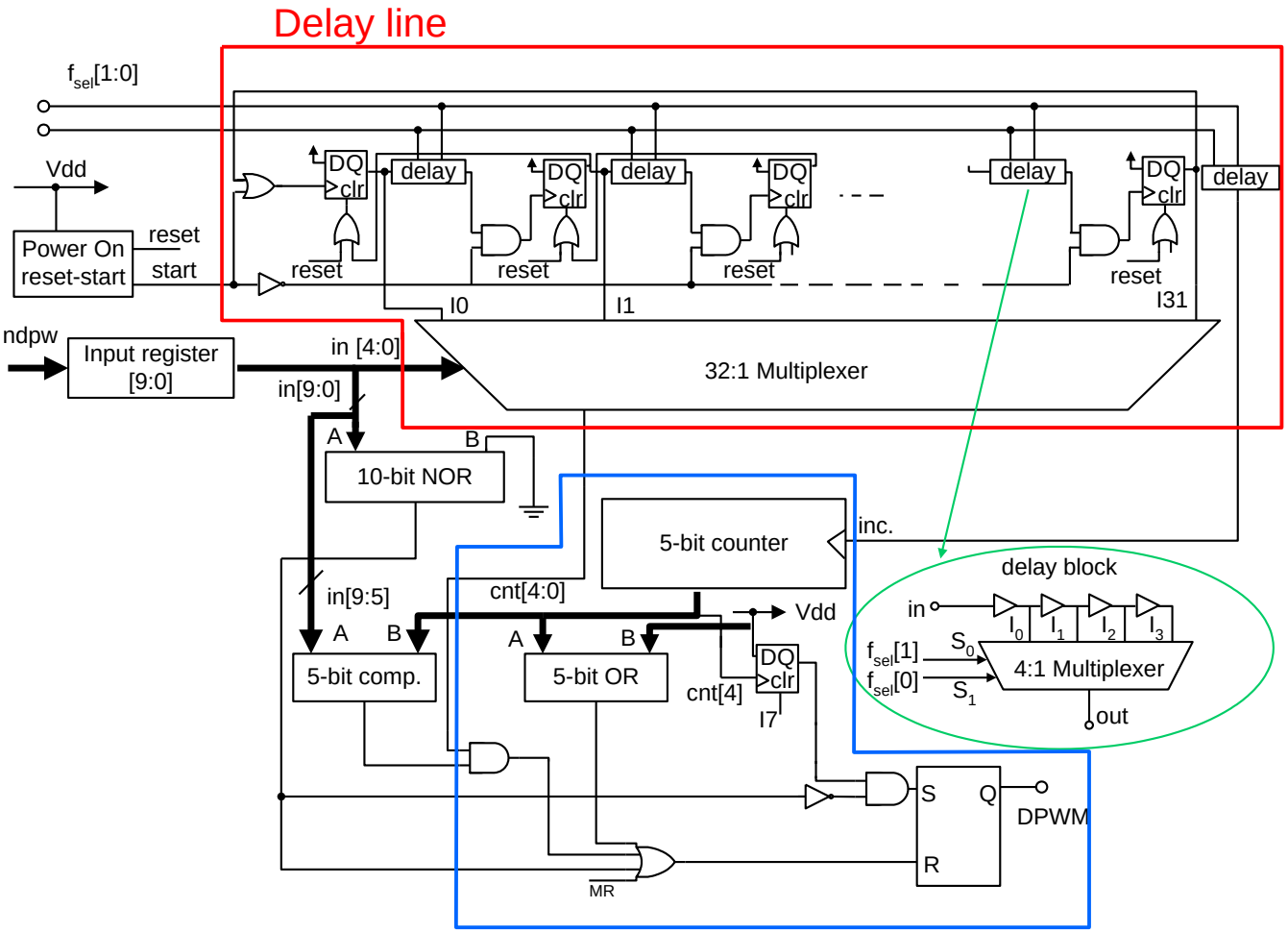


$$N_{delay\_el} = 2^{N_{DPWM}}$$

$$P_{tot} = \sum_{i=1}^{N} \left(\alpha_i C_i V_{dd}^{\,2} f_{clk} + \alpha_i I_{sc} V_{dd} + I_{leakage_i} V_{dd} \right)$$

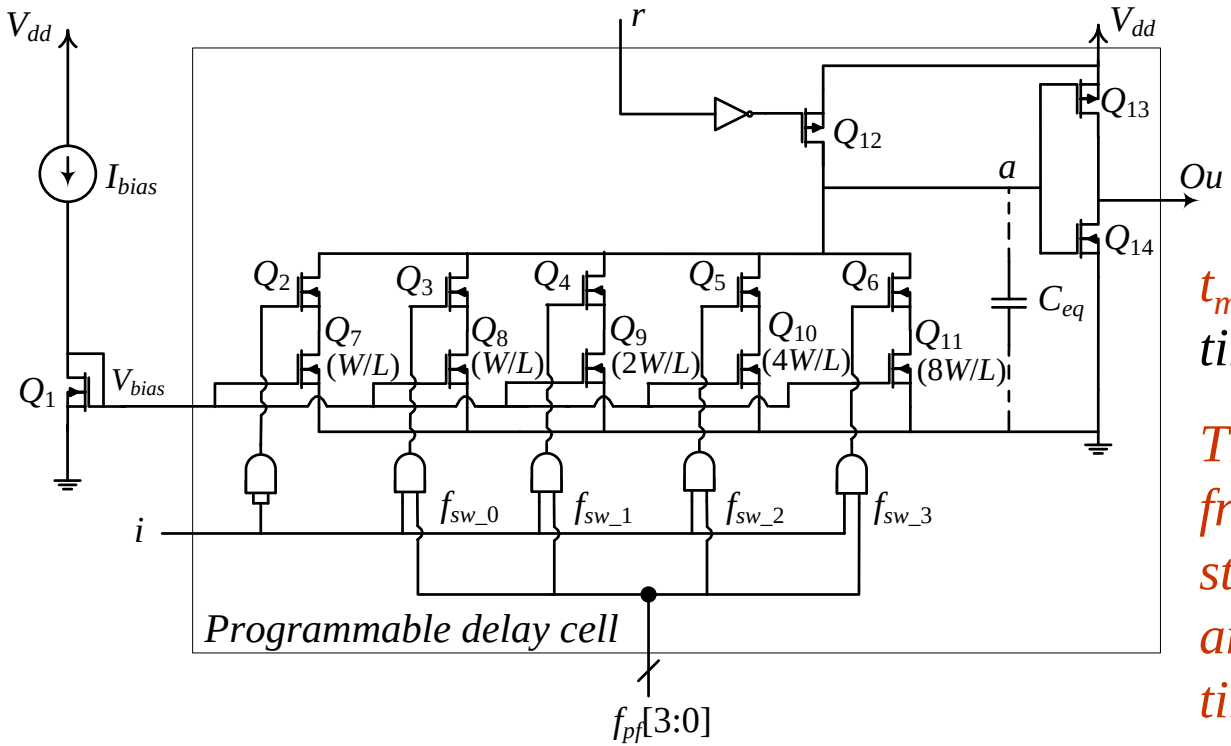
- *Low power consumption*
- *Requires relatively large silicon area*
- *Nonlinearity (non-monotonic) problems could occur*

DPWM: Hybrid Ring/Counter Based Architecture



❑ *Hybrid structure shares advantages (and drawbacks) of the previous two architectures. A compromise between power and area consumption.*

"Digital Like" Analog Component: Digitally Programmable Current-Starved Delay Cell



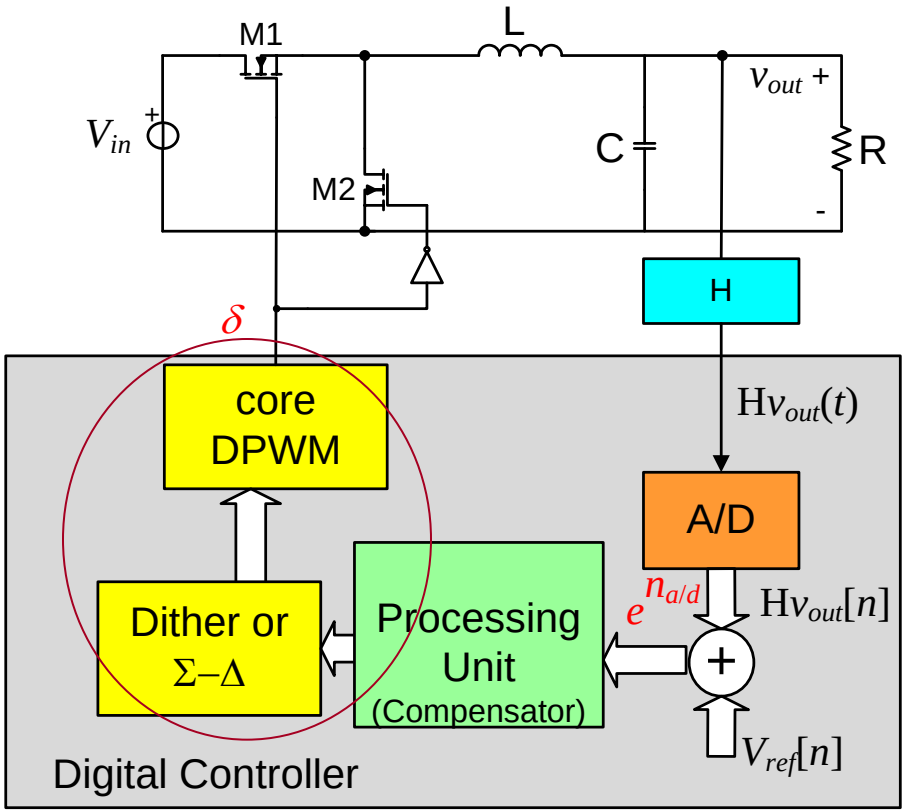
$$t_{delay} = f_{sw}[n]t_{\min}$$

t_{min} – *minimum propagation time*

The resolution/ maximum frequency of the DPWM are still limited. For 10 MHz and 10-bit the propagation time < 100 ps needed!

- *Allows regulation of switching frequency/resolution*
- *Reduces overall size and power consumption*
- *Can operate at low supply voltages used for digital logic, i.e. can be implemented in most recent technologies.*

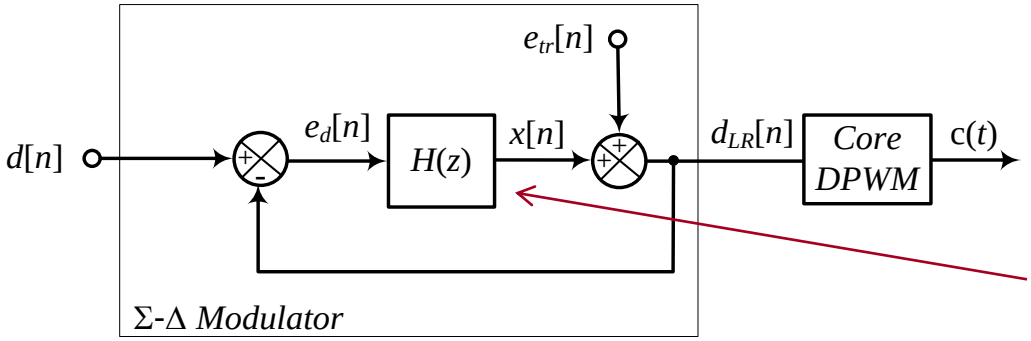
High-Frequency High-Resolution Dithering and Sigma-Delta Based DPWM



- The duty ratio of a core resolution (high-frequency) DPWM is varied over several switching cycles to achieve high effective resolution.

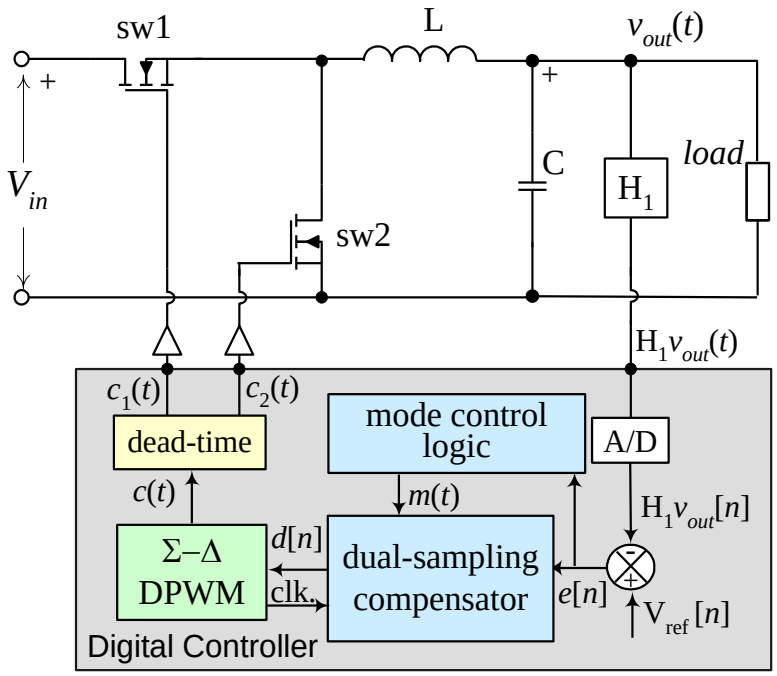
- For example, for a 2-bit DPWM producing 0%, 25%, 50 %, 75%, and 37.5% can be obtained by periodically changing output between 25 % and 50%.

High-Frequency High-Resolution 1st Order Σ–Δ Based DPWM



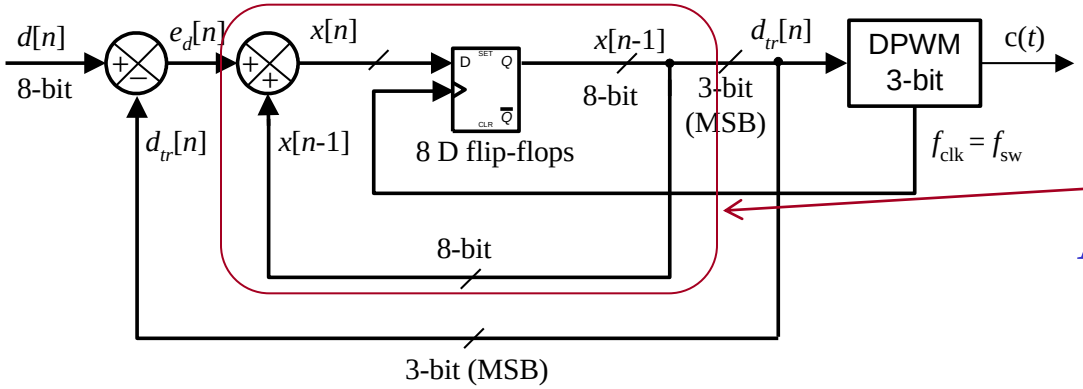
$$H(z)=\frac{X(z)}{E_d(z)}=\frac{z^{-1}}{1-z^{-1}}$$

A pole in zero, i.e. integrator 1/s



- Sigma-delta modulator changes the output of the core (3-bit) DPWM to result in average value equal to the high-resolution input d[n]
- The averaging is performed by the switching converter itself (LC filter)
- Can be implemented with very simple hardware

1st Order Σ–Δ DPWM – Tone Problems



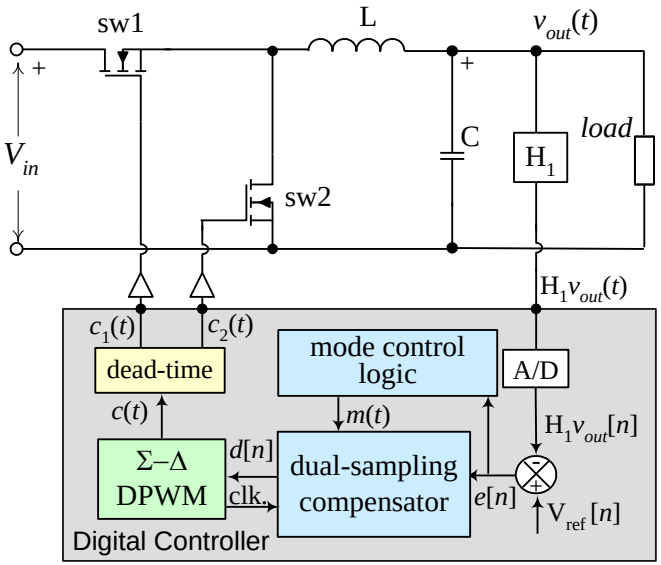
$$H(z)=\frac{X(z)}{E_d(z)}=\frac{z^{-1}}{1-z^{-1}}$$

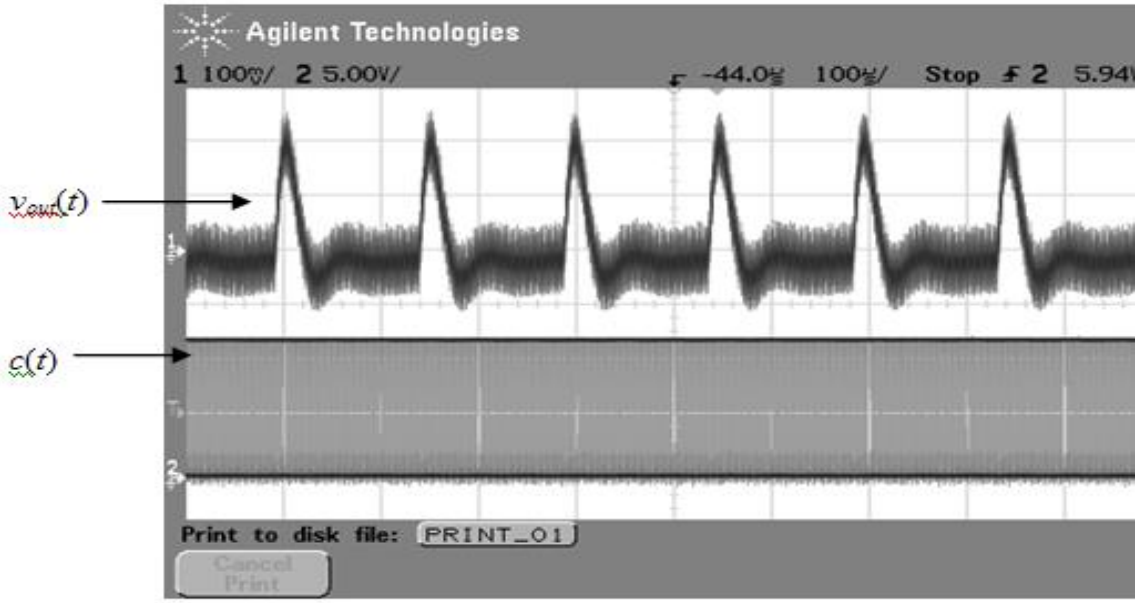
An s-pole in zero, i.e. integrator 1/s

Periodic output sequence for a constant input

n	d[n]	$e_d[n]$	x[n]	x[n-1]	$d_{tr}[n]$	Duty Ratio c(t)	Average Duty Ratio
1	0.2	0.2	0.2	0	0	0	0
2	0.2	0.0125	0.2125	0.2	0.1875	0.1875	0.0937
3	0.2	0.0125	0.225	0.2125	0.1875	0.1875	0.0125
4	0.2	0.0125	0.2375	0.225	0.1875	0.1875	0.1406
5	0.2	0.0125	0.25	0.2375	0.1875	0.1875	0.15
6	0.2	-0.05	0.2	0.25	0.25	0.25	0.1666
7	0.2	0.0125	0.2125	0.2	0.1875	0.1875	0.1696
8	0.2	0.0125	0.225	0.2125	0.1875	0.1875	0.1719
9	0.2	0.0125	0.2375	0.225	0.1875	0.1875	0.1736
10	0.2	0.0125	0.25	0.2375	0.1875	0.1875	0.175
11	0.2	-0.05	0.2	0.25	0.25	0.25	0.1818
12	0.2	0.0125	0.2125	0.2	0.1875	0.1875	0.1822

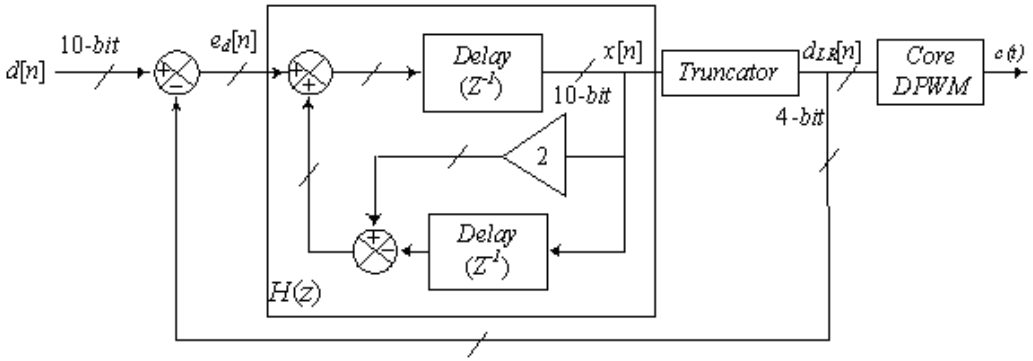
1st Order Σ–Δ Based DPWM – Tone Problems





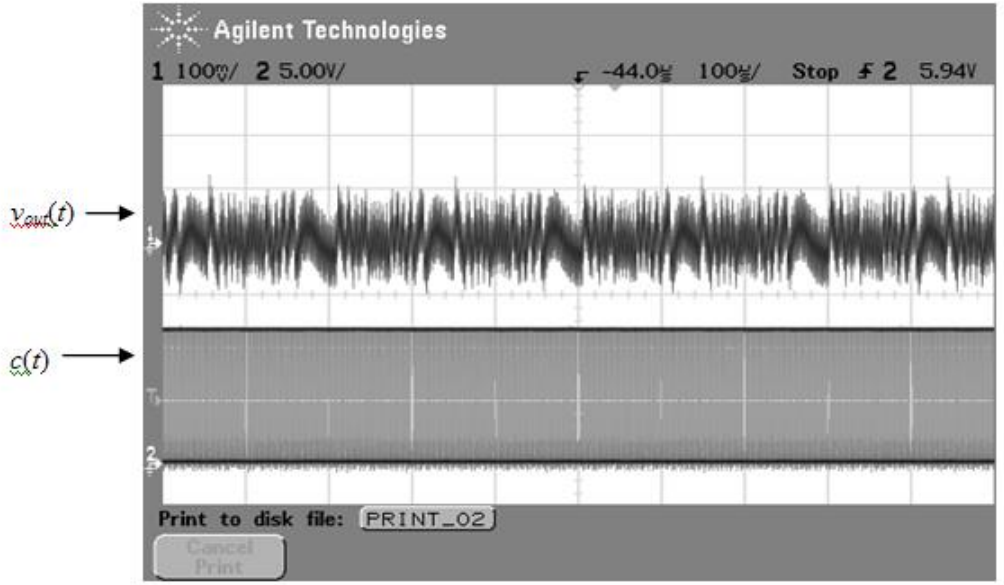
- *For some inputs the low frequency periodic sequences (tones) can coincide with the corner frequency of the LC filter causing large output voltage variations*

2nd order Σ–Δ Based DPWM



- *By changing the output duty ratio more aggressively creates tones at higher frequencies.*

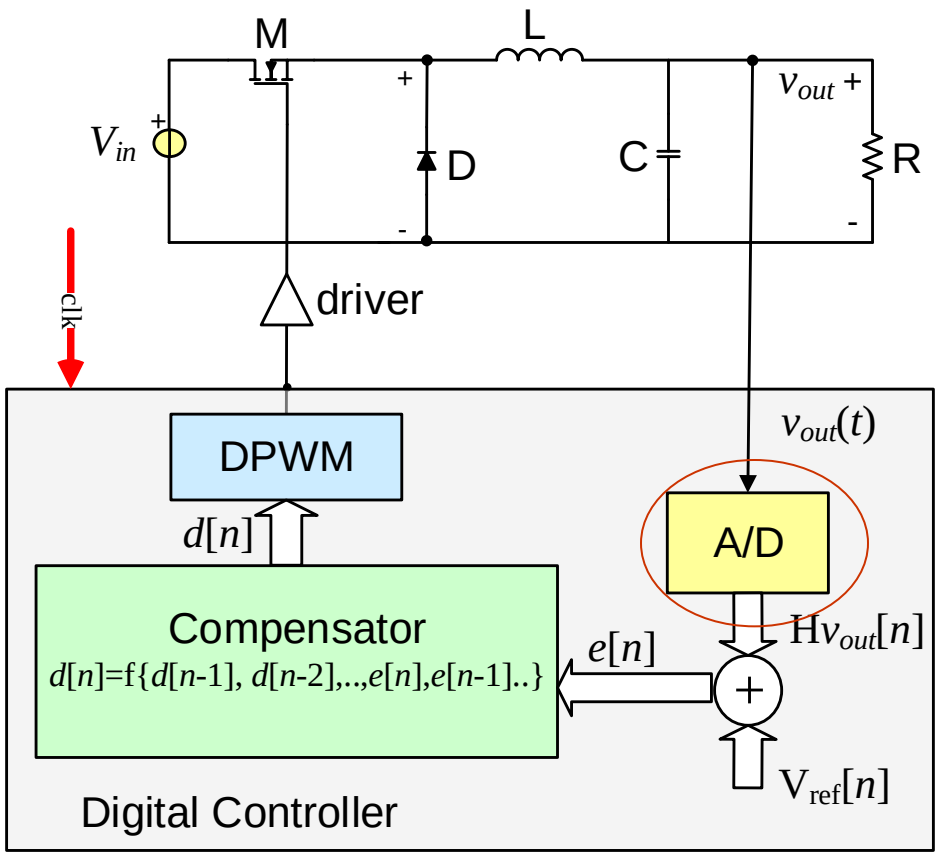
- *Elimination of tone related problems with a minor increase of hardware complexity.*



Design/Selection of Power & Area Efficient Basic Functional Blocks

Analog-to-Digital Converter (ADC) Architectures

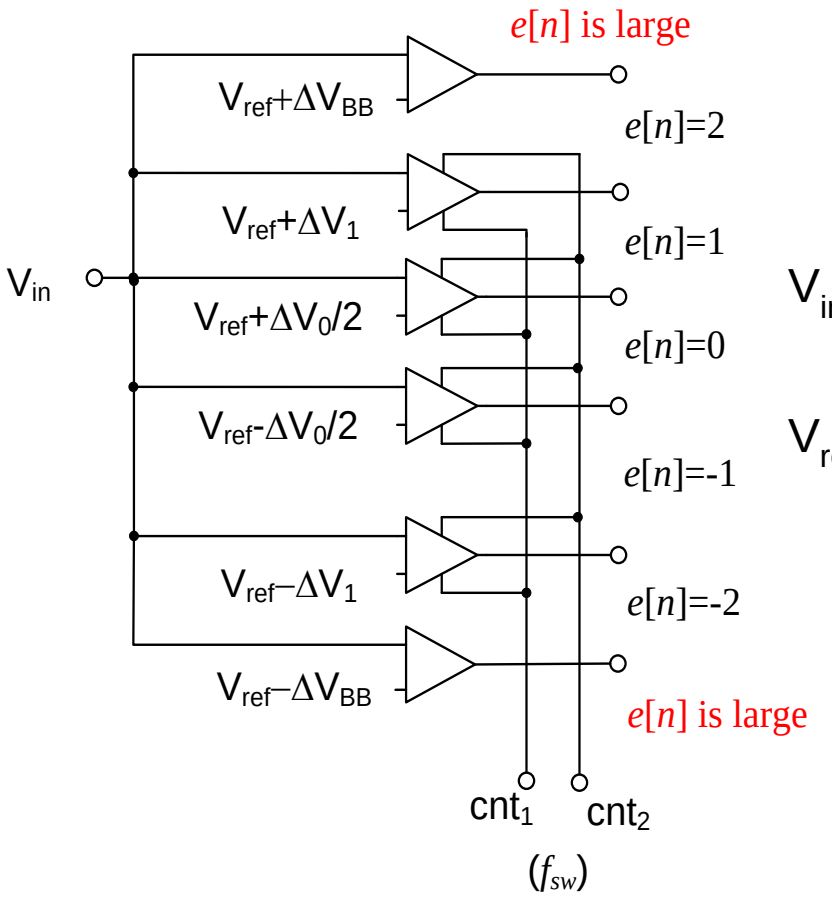
ADC Requirements

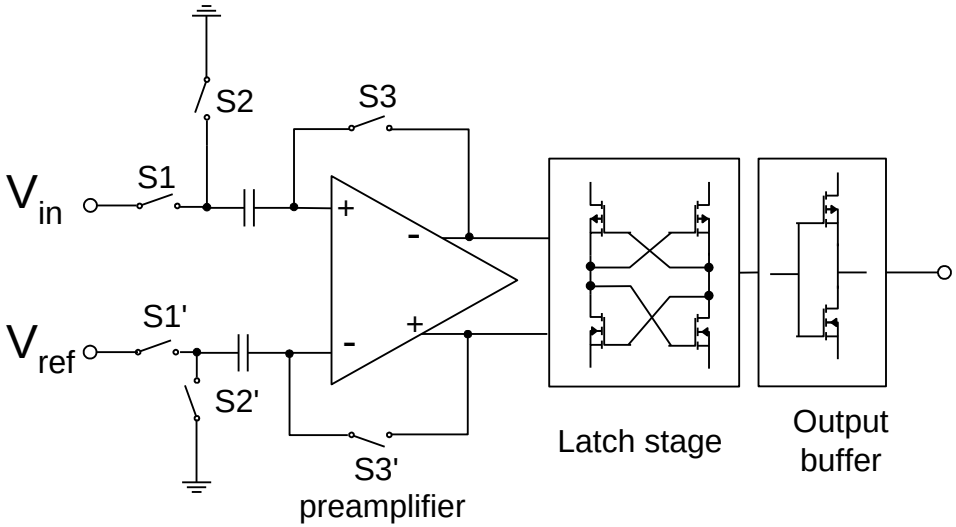


- The ADC does not need to measure the voltage over a large range, just around reference voltage
- Resolution of the ADC needs to be just sufficient to satisfy voltage regulation requirement V_{Q_ADC} just a little bit smaller than the maximum allowable v_{out} variation
- *Important for limit cycling, not to push the resolution of the ADC too much since it can cause the LCO or require very high resolution for the DPWM*

$$V_{q\_ADC} > V_g \cdot \Delta M(D)$$

Windowed Flash ADC





A comparator with offset calibration and latch stage

- Lower power consumption than the full-range flash ADC, still could be larger than a complete analog controller
- Can even be implemented in discrete manner, no need for a full range ADC

Design Guidelines (Steps) for Selecting Resolution of the ADC and DPWM

- Determine resolution of the ADC based on the voltage regulation, i.e. allowable variation of the output voltage in steady state => just marginally smaller than the voltage regulation requirement
- In this case lower ADC resolution of the ADC is better (smaller requirements for DPWM)
- Based on $V_{q\_ADC} > V_g \cdot \Delta M(D)$

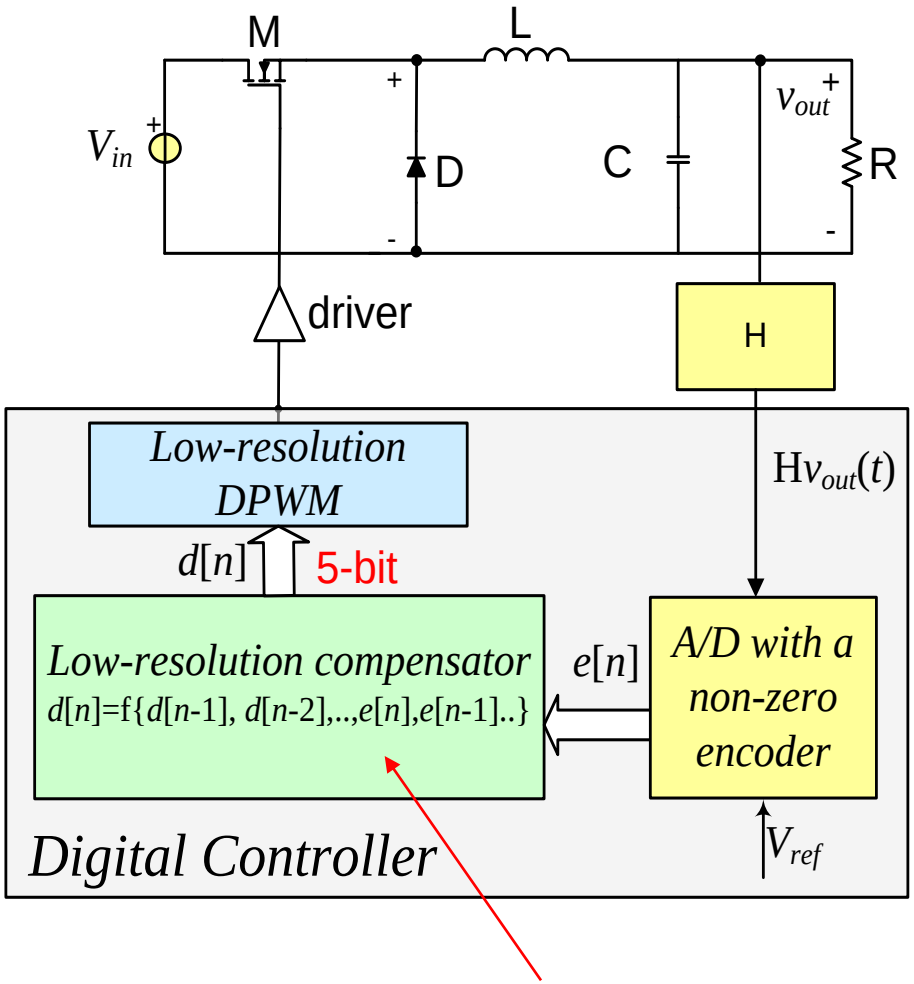
select the resolution of the DPWM

More Stringent Requirements

- *What do we do if the regulation requirement is so tight that the resolution of the DPWM and the ADC are so high that we cannot realistically make it (cannot find/build components)*

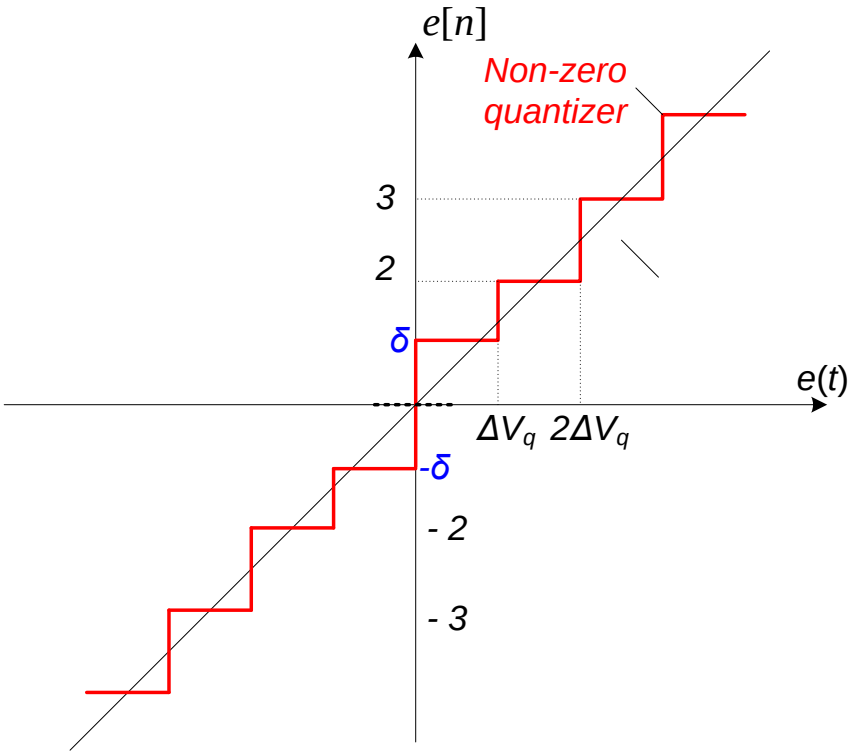
Non-Zero Error Coding Method for Improving Voltage Regulation of Low-Resolution Digital Controllers

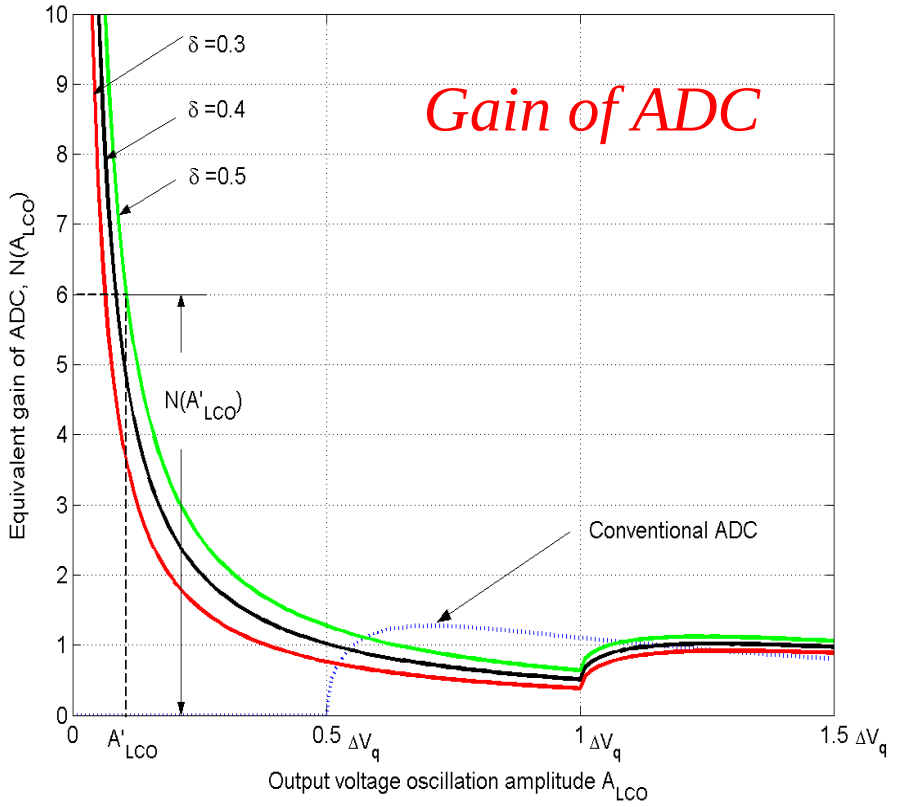
Causing *d*[*n*] Oscillations



If we eliminate the zero error bin, the compensator will always be excited and => oscillations will always happen

Controlling the Oscillations: Gain Characteristic of the Non-Zero ADC





- *δ is a variable that we define in our controller, for example (can be set between 0 and 2)*

Controlling the Amplitude and Frequency of the Oscillations

$$-1 = 1\angle 180^\circ = N(A_{LCO})T(j\omega_{LCO})$$

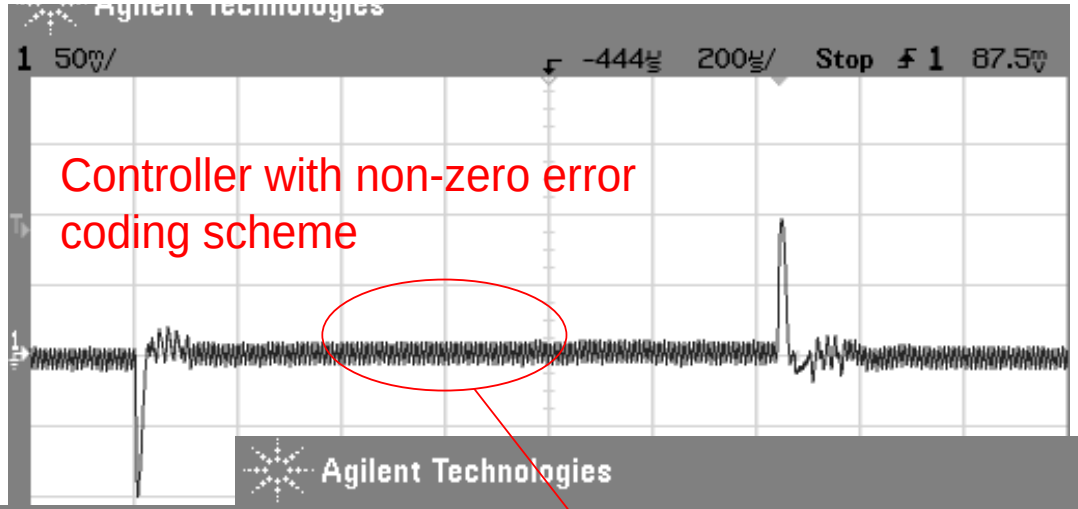
Gain of ADC at the point of oscillations

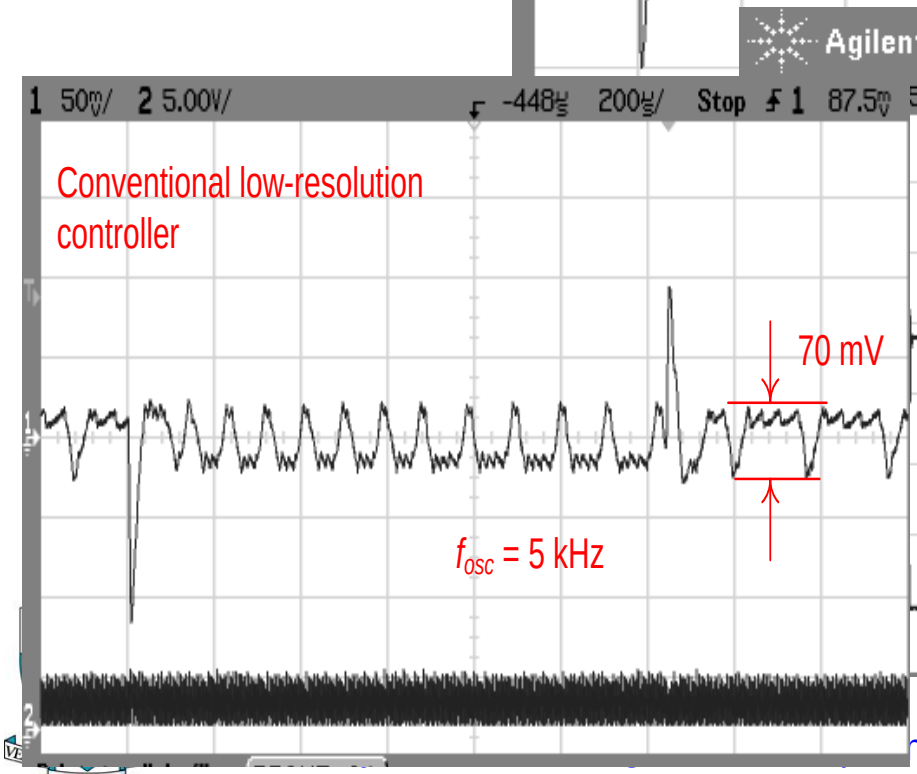
Loop gain

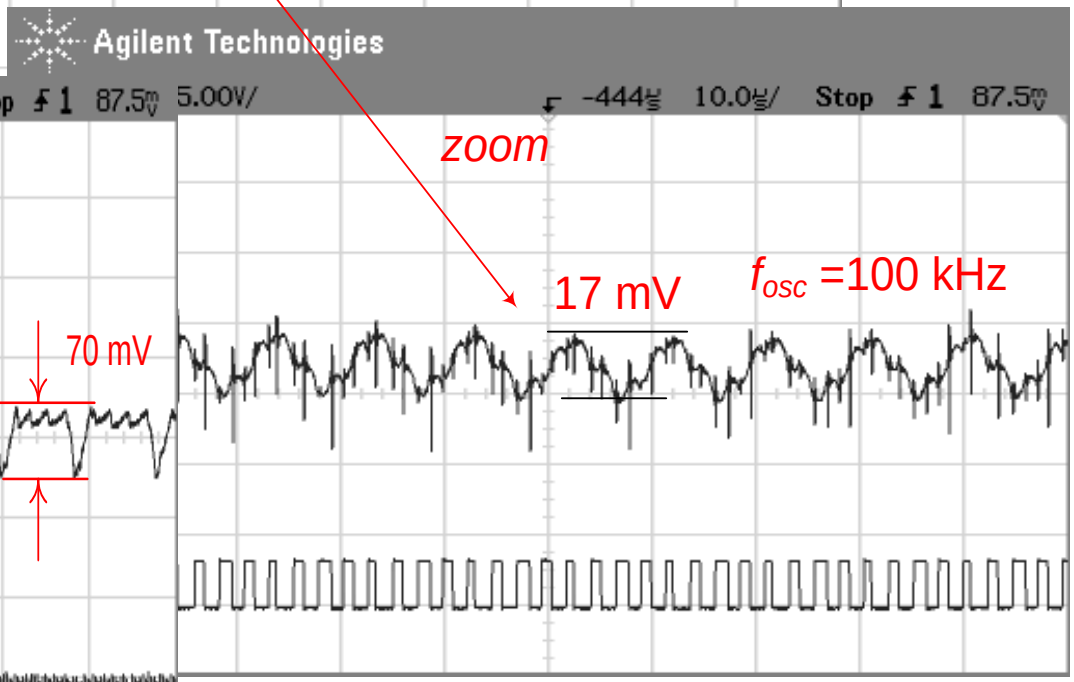
- *Adjust the compensator such that the phase shift of the loop gain is 180° at the desired oscillations frequency (larger than the crossover frequency of the power stage)*

- *Select the value δ such that the gain of the ADC, i.e. amplitude of oscillations, automatically adjusts to a pre-defined limited amplitude*

Experimental Results







Conclusions

- *Hardware-efficient low-power implementation of a high-frequency digital controller for SMPS is possible*
- *The same architecture can be implemented using FPGA systems or any other hardware and higher power levels*
- *Some of these architectures are today used in several commercial products (TI and Exar, can be used as a good foundation for building integrated solutions)*

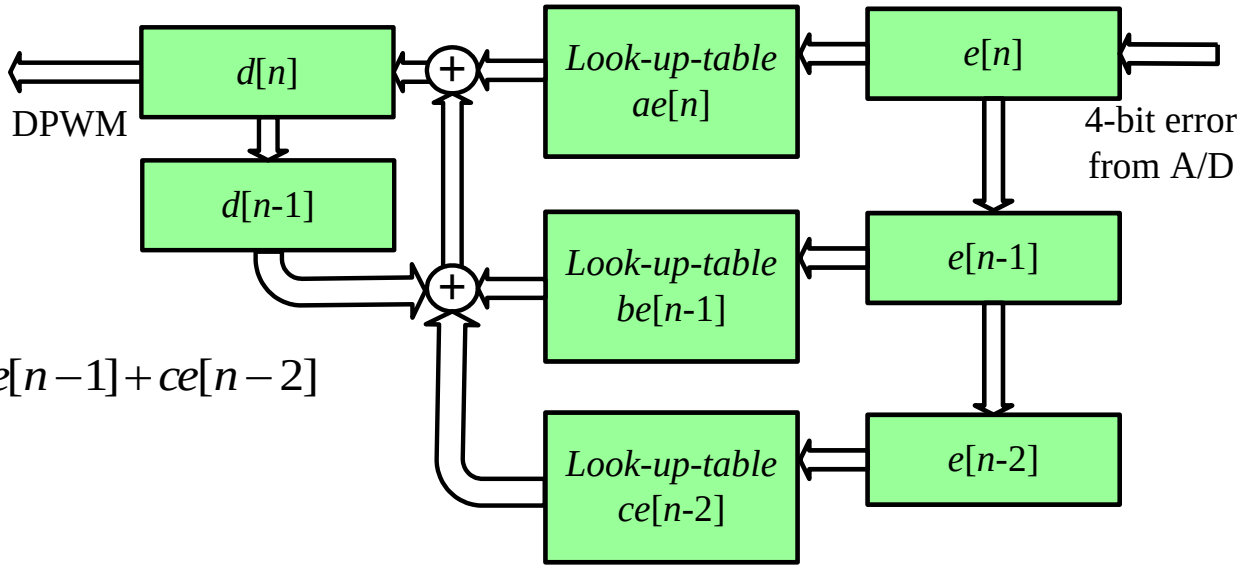
Design/Selection of Power & Area Efficient Basic Functional Blocks

Compensator

Look-up Table Based PID compensator

Discrete-time control law:

$$d[n] = \alpha_1 d[n-1] + \alpha_2 d[n-2] + \ldots + \beta_0 e[n] + \beta_1 e[n-1] + \ldots$$



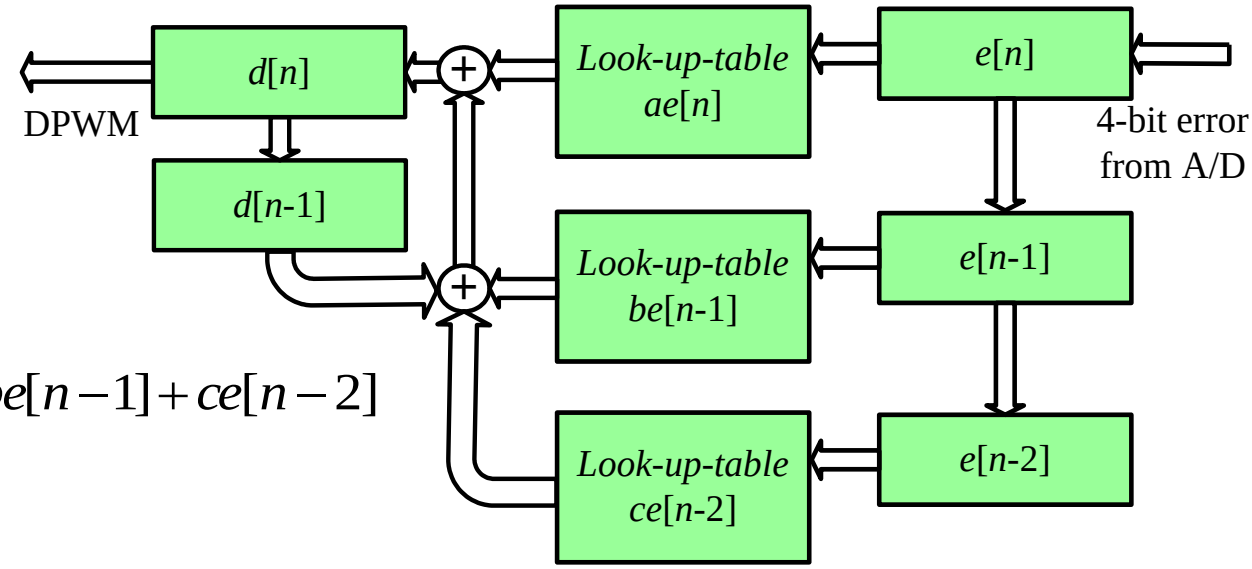
$$d[n] = d[n-1] + ae[n] + be[n-1] + ce[n-2]$$

- Zero steady-state error,
- No multipliers, which can be hard to implement at high frequencies, almost no resources spent on d[n-1]
- Inherent soft start-up

Look-up Table Based PID compensator

Discrete-time control law:

$$d[n] = \alpha_1 d[n-1] + \alpha_2 d[n-2] + \ldots + \beta_0 e[n] + \beta_1 e[n-1] + \ldots$$



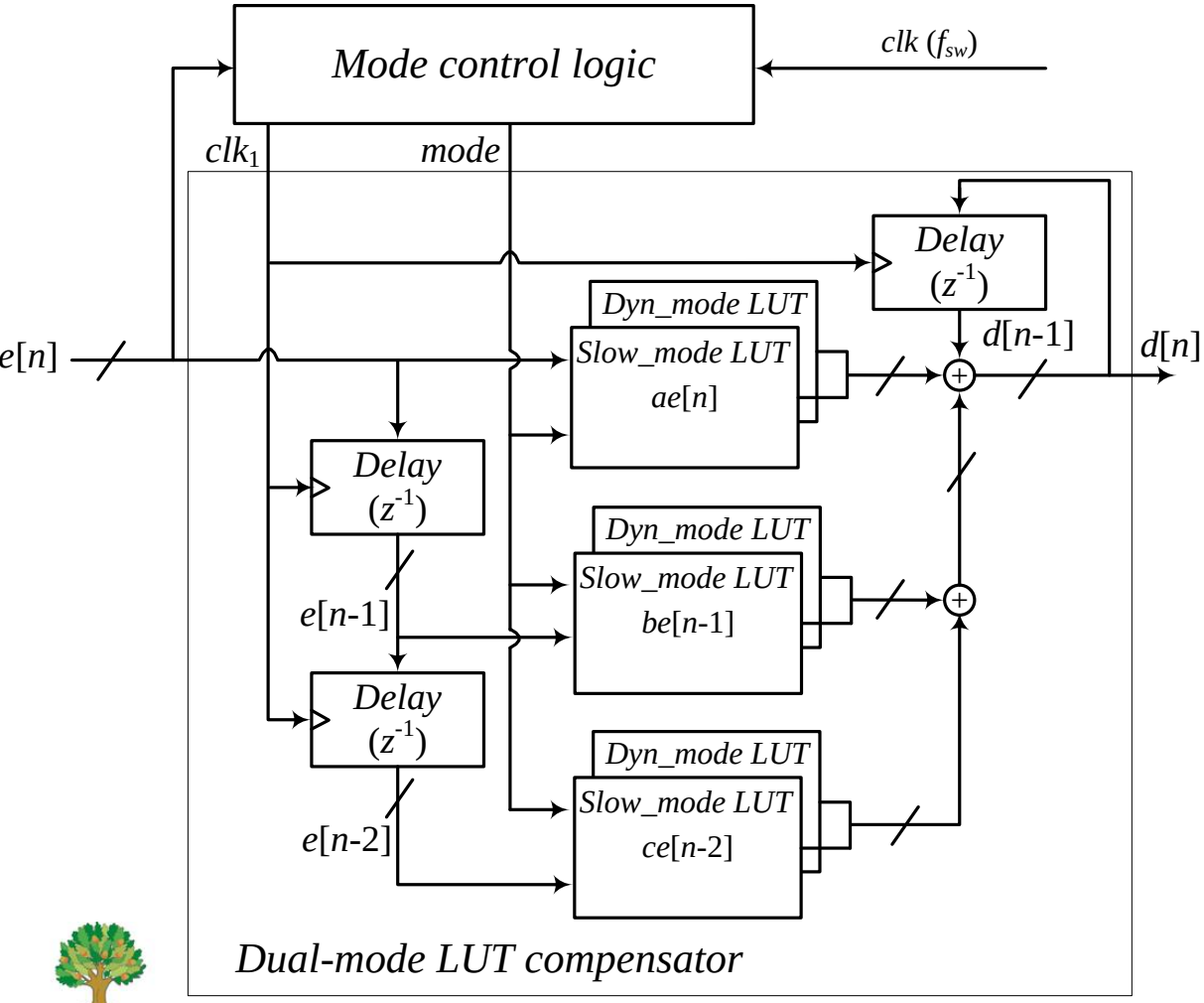
$$d[n] = d[n-1] + ae[n] + be[n-1] + ce[n-2]$$

- A tradeoff between the speed stability and power consumption of the compensator

$$P_{tot} = \sum_{i=1}^{N} \left(\alpha_i C_i V_{dd}^{\ 2} f_{clk} + \alpha_i Q_{sc} V_{dd} f_{sw} + I_{leakage_i} V_{dd} \right)$$

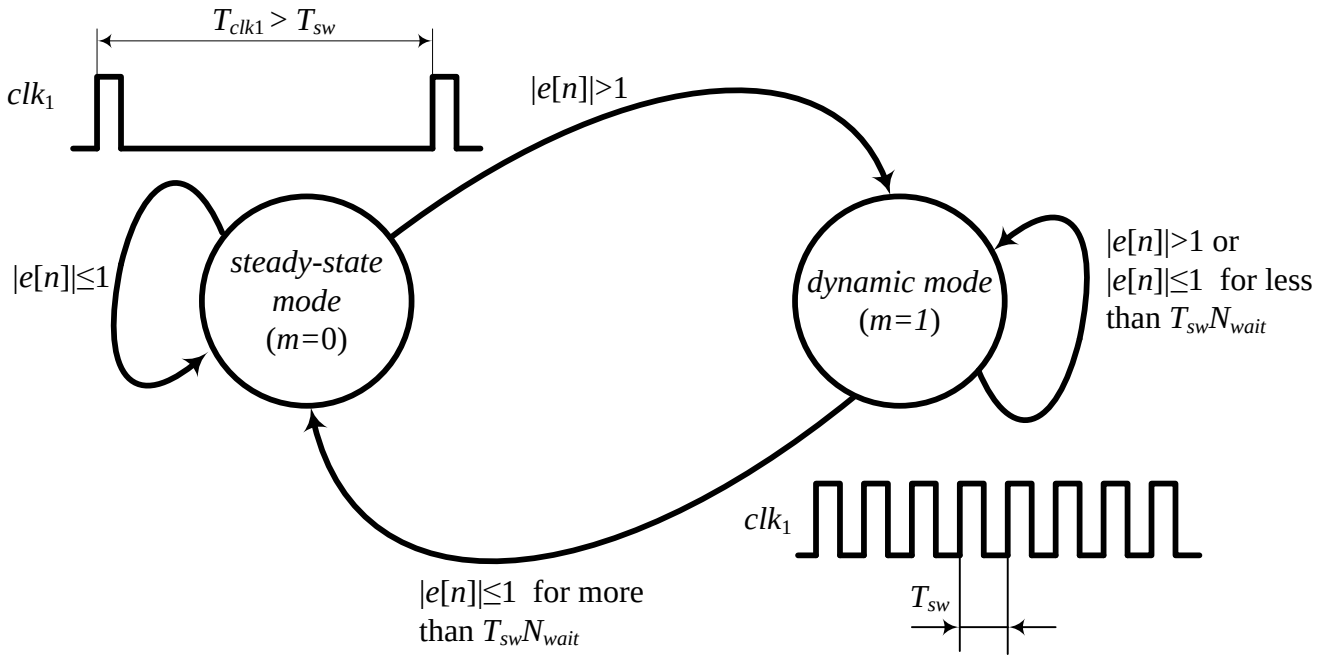
Faster compensator implies a larger probability of logic state changes and, likely, lower stability margin.

Dual mode look-up table based PID compensator



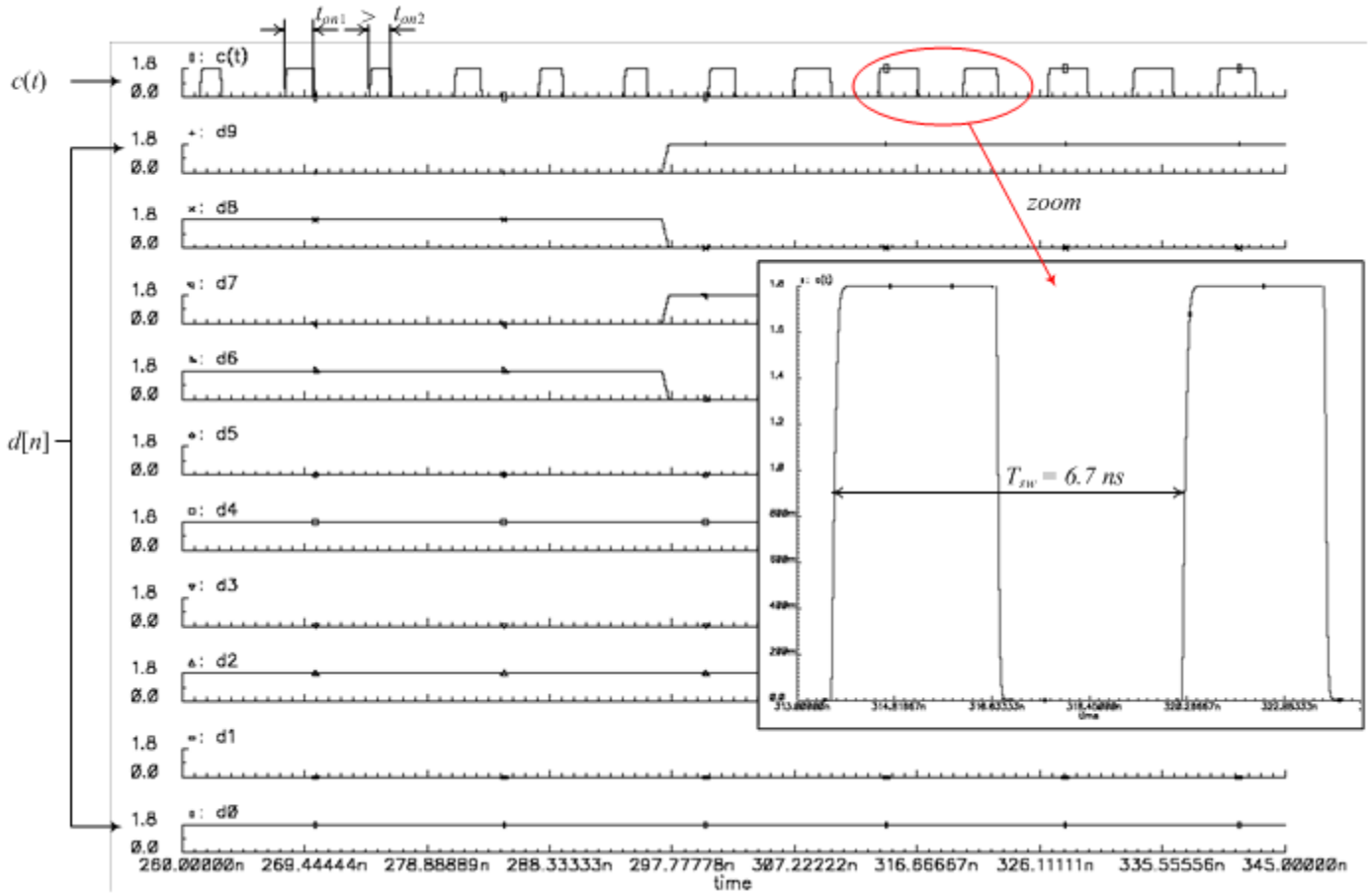
- *In steady state the compensator operates with only 3 error values - 1, 0, and 1 and reacts slowly, i.e. α reduced*
- *During transients a fast compensator starts working*

Dual mode look-up table based PID compensator



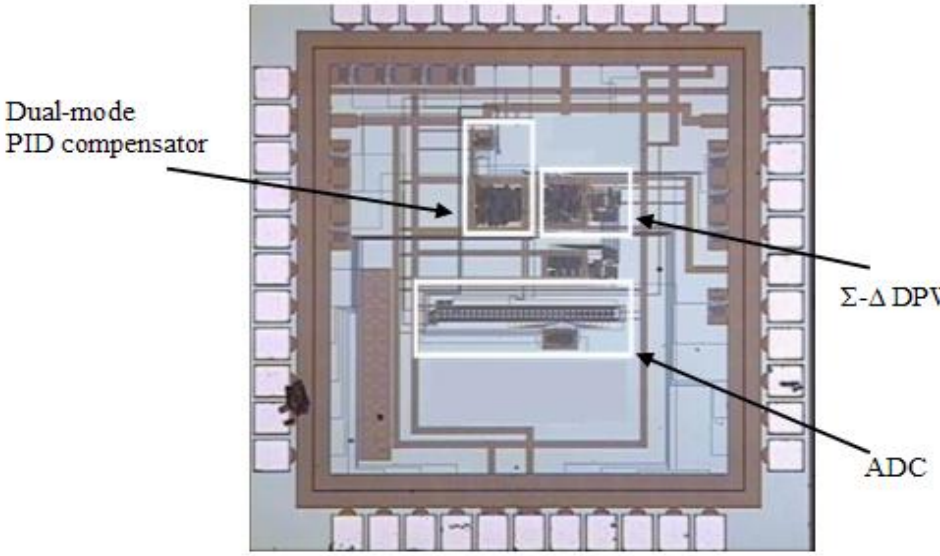
Operation of mode switching logic

Ultra-High Frequency 2nd Order Σ–Δ Based DPWM

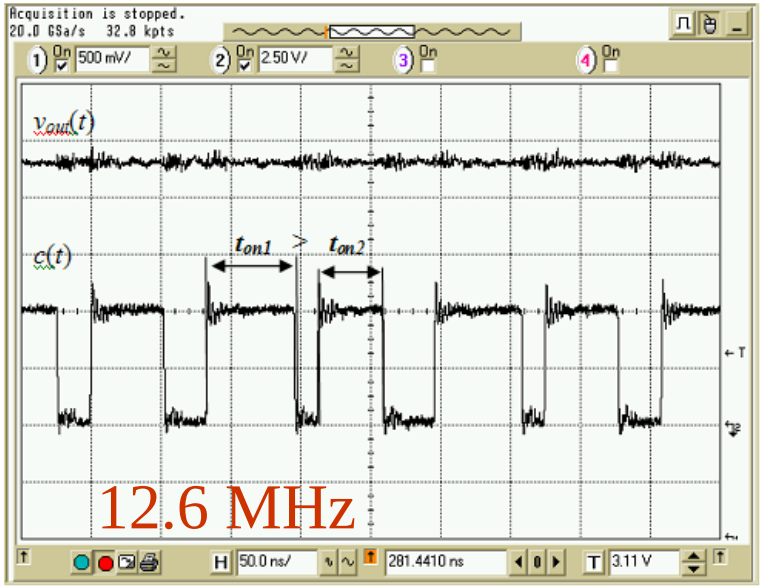


150 MHz *post-layout simulation results*

IC Implementation and Experimental Results



DPWM switching frequency	Programmable, 400 kHz to 18 (400) MHz
DPWM effective resolution	10-bit
Σ-Δ DPWM chip area	0.028 mm^2
Core DPWM current consumption	43 (8) μA/MHz
Σ-Δ Modulator current consumption	2 μA/MHz

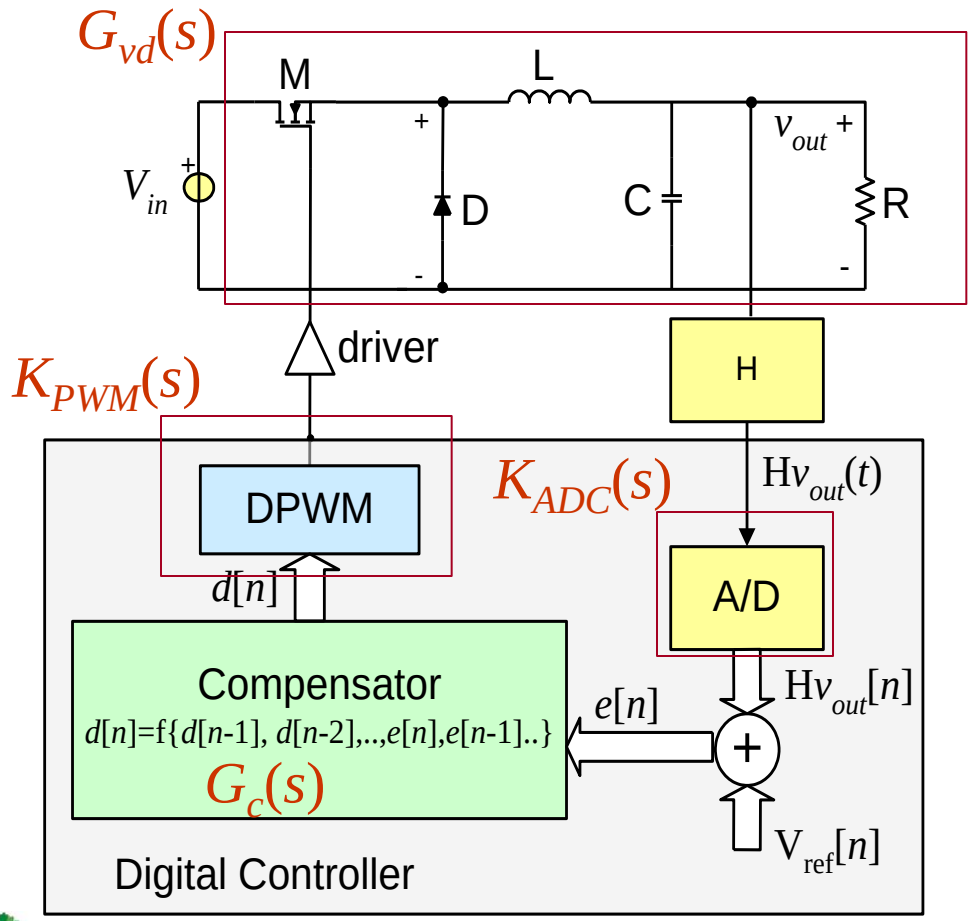


More Stringent Requirements

- *What do we do if the regulation requirement is so tight that the resolution of the DPWM and the ADC are so high that we cannot realistically make it (cannot find components)*

Modeling of Digitally Controlled SMPS and Compensator Design (Selection of Discrete Control Law)

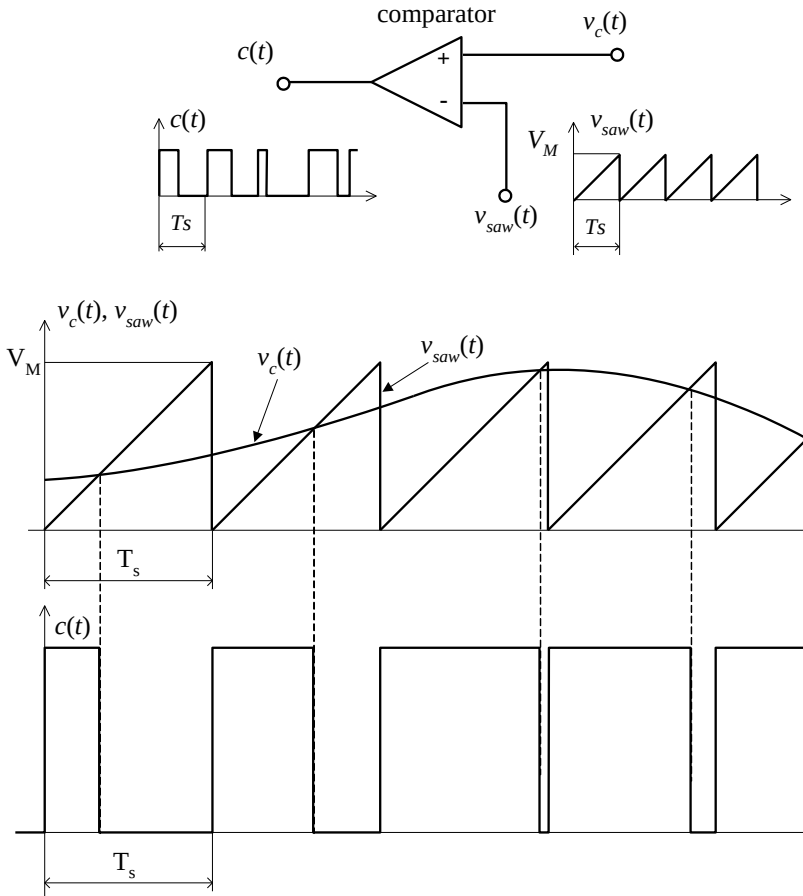
Goal of This Section



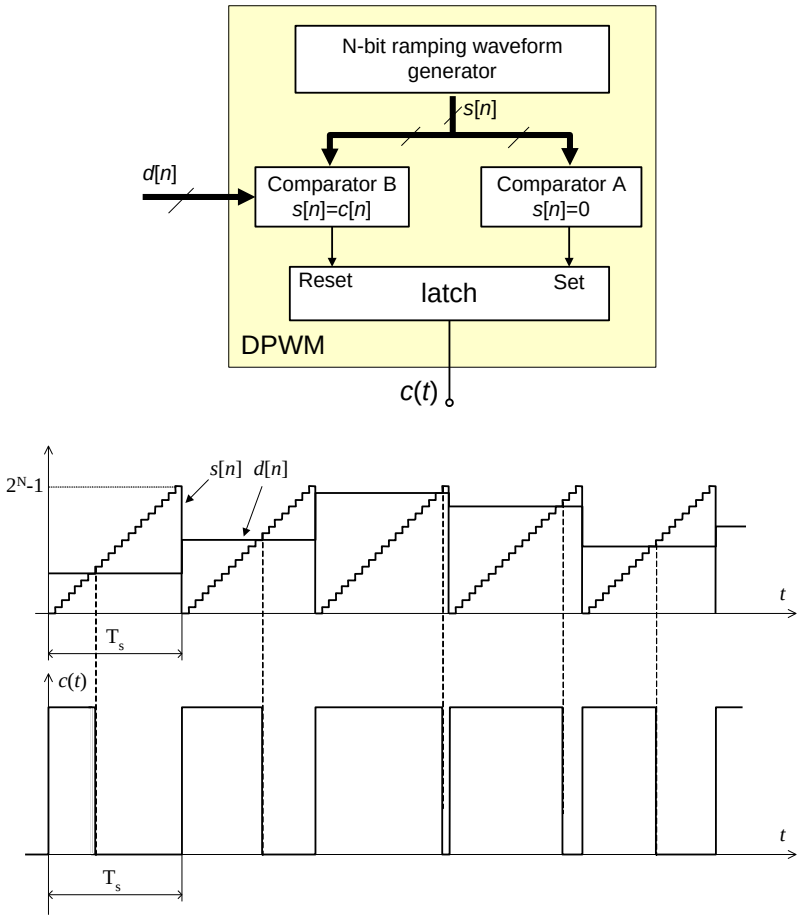
- To find a modified transfer function of this controller utilizing the large body of knowledge from analog modeling
- In other words, to modify the transfer functions such that the DPWM and ADC are included (we know their resolution and properties now)
- To select digital PID compensator control law, i.e. coefficients in difference equations

Modeling of the ADC and DPWM

Analog pulse-width modulator and DPWM

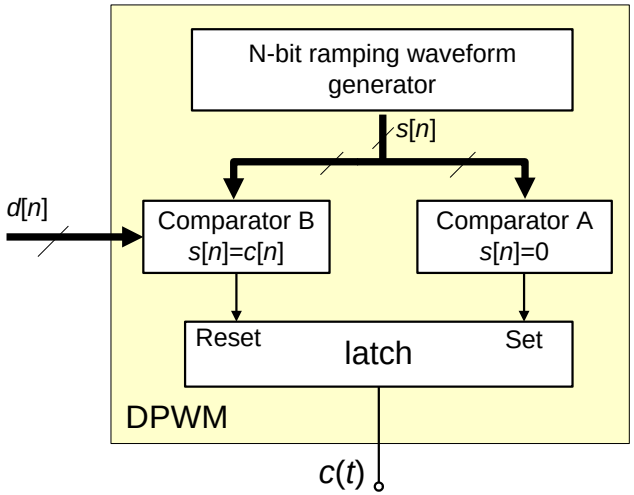


Analog PWM



Digital Pulse Width Modulator (DPWM)

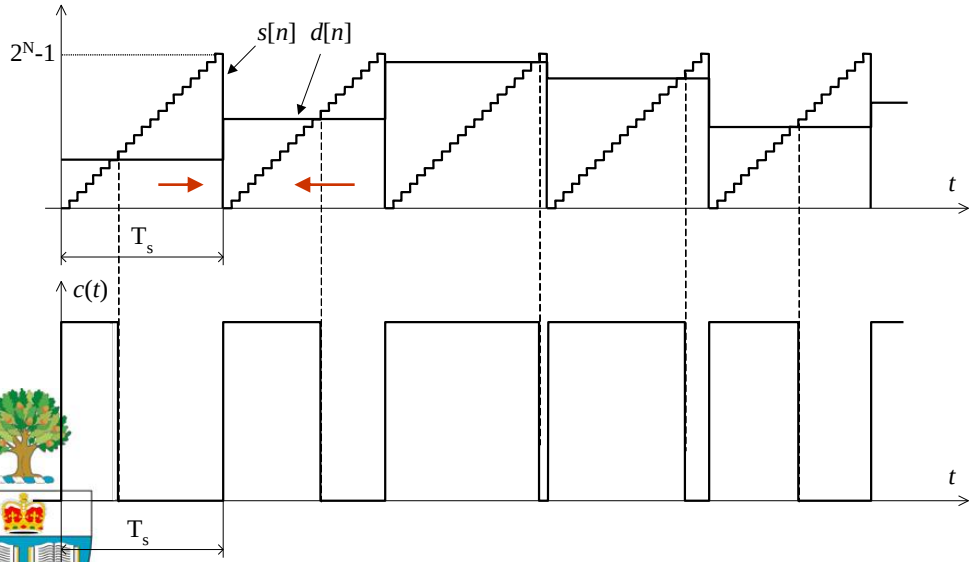
Modeling of DPWM



Phase Characteristic

$$T_d = DT_s$$

$$\angle G_{DPWM}(j\omega) = \angle e^{-j2\pi f_s DT_s} = -2\pi f_s DT_s$$



Modeling of DPWM

The DPWM's gain K_{DPWM} is the ratio of the change of the duty cycle D in the pulse-width modulated signal c(t) and the increment of the control variable d[n],

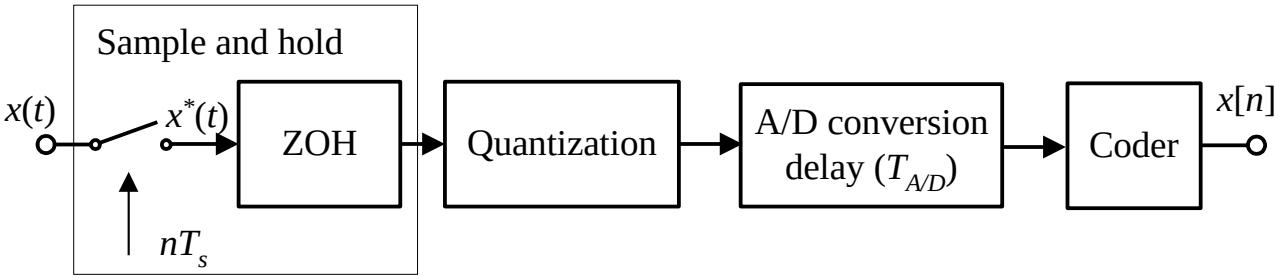
$$K_{DPWM} = \frac{dD}{dd} \approx \frac{\Delta D[n]}{\Delta d[n]}$$

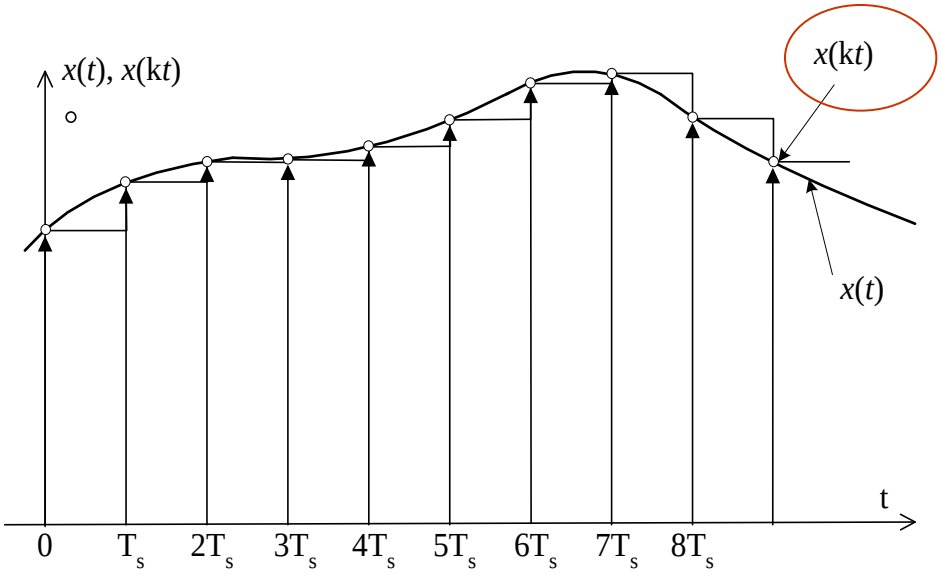
$$\Delta D[n] = \frac{1}{2^{N_{DPWM}}}$$

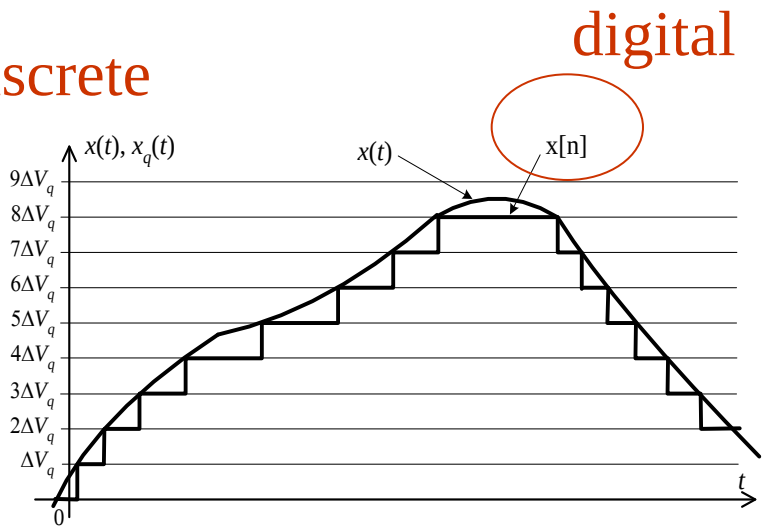
← *Duty ratio changes in discrete steps*

The minimal increment of the control variable depends on the selected representation of numbers. The numbers' representation defines the value of the least significant bit LSB_{DPWM} of the input control signal.

Modeling of A/D converter



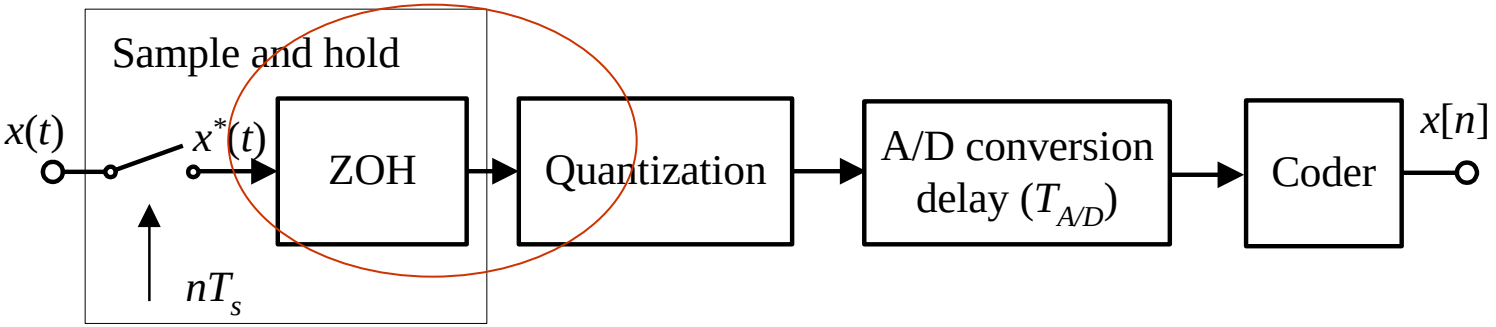


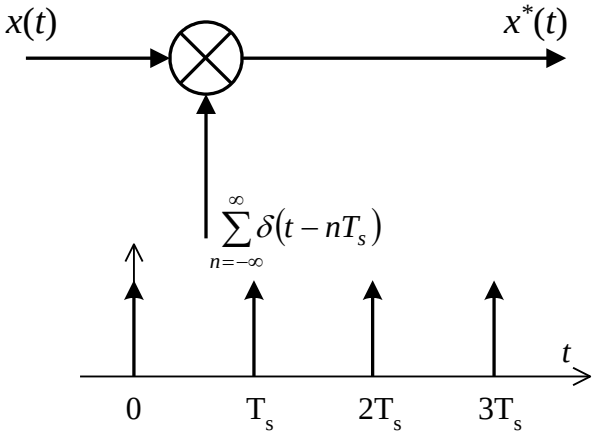


Amplitude discretization

Discretization in time: Sample and hold

A/D: Sample and Hold



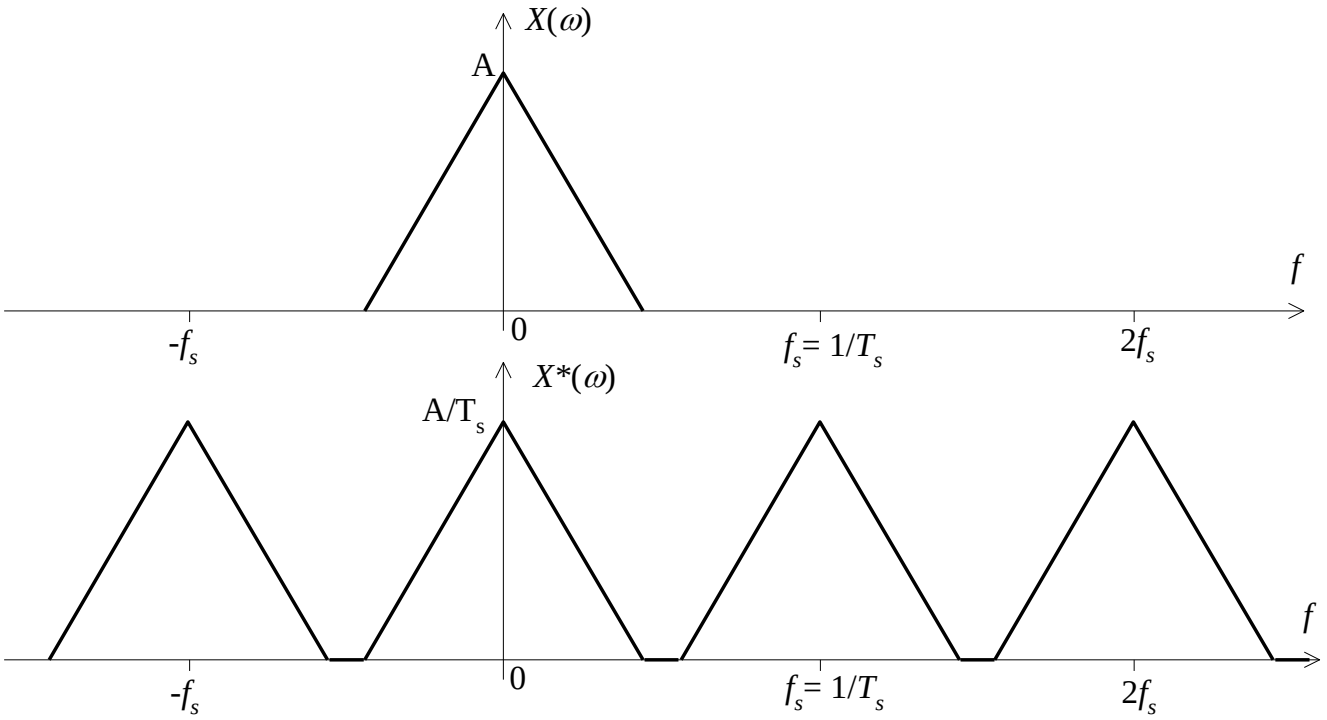


$$x^*(t) = \sum_{n=-\infty}^{\infty} x(t)\cdot\delta(t-nT_s)$$

$$X^*(s) = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} X(s-jn\omega_s)$$

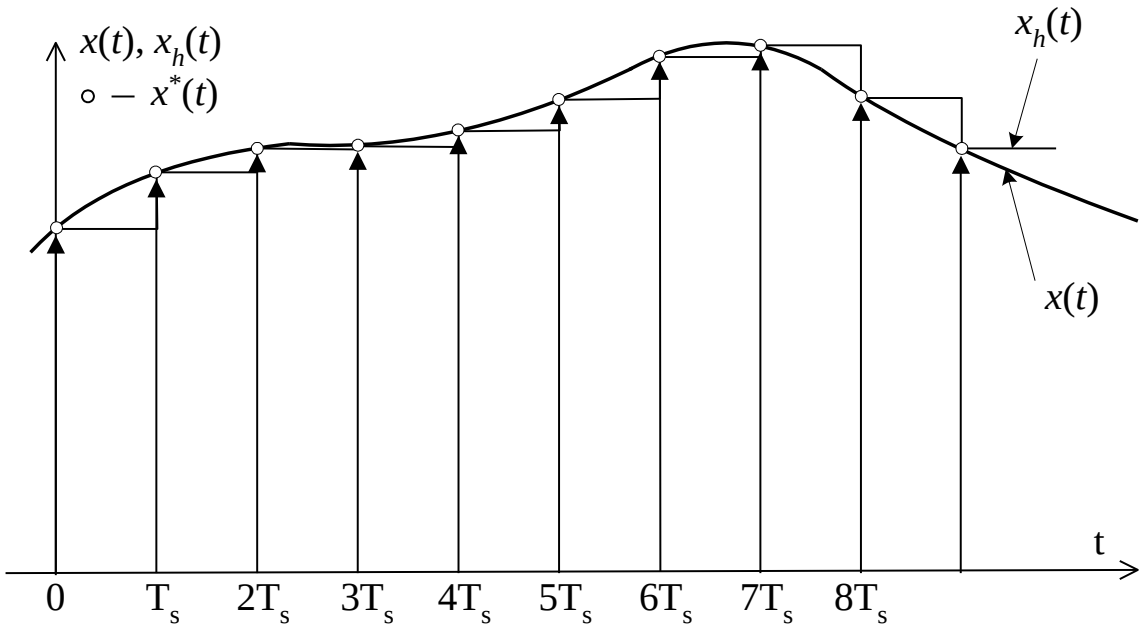
Sampling of a continuous-time signal

A/D (S &H): sampled signal spectrum



Spectrums of a continues time signal (top) and its sampled equivalent (bottom)

A/D modeling: Zero order hold (ZOH)



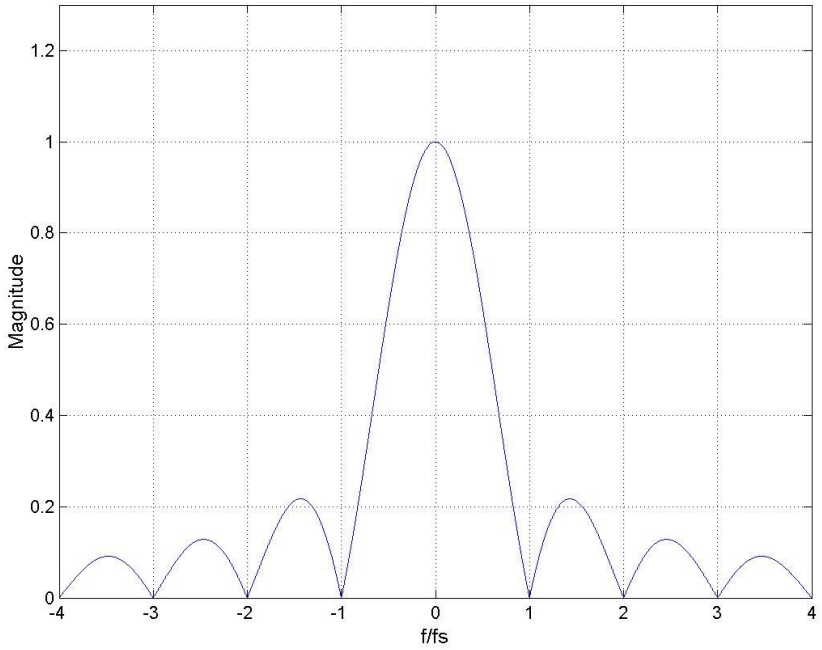
$$u(t) = h(t) - h(t - T_s)$$

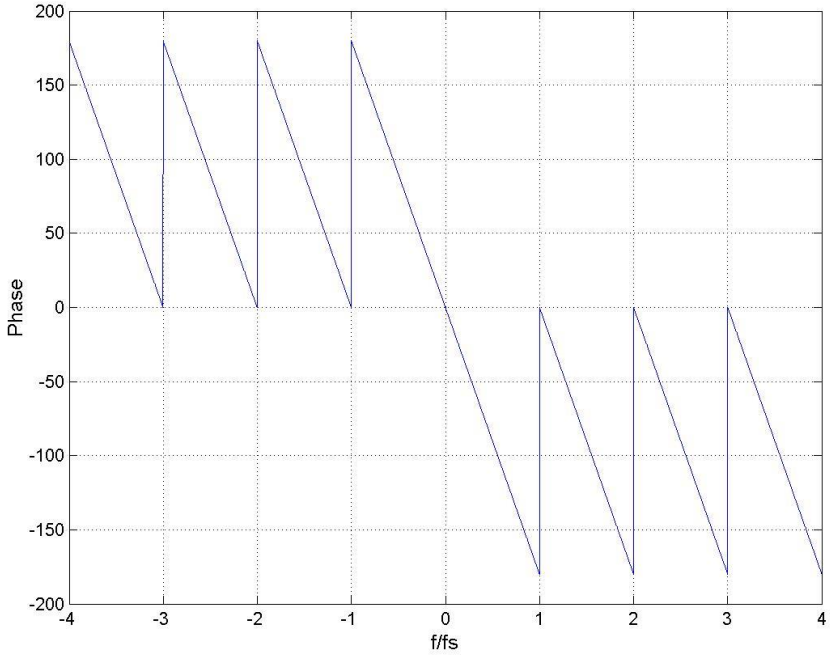
$$\Im\{u_h(t)\} = U_h(j\omega) = \frac{1 - e^{-j\omega T_s}}{j\omega}$$

Transfer function of the zero-order hold circuit:

$$U_h(j\omega) = \frac{1 - e^{-j\omega T_s}}{j\omega} = e^{-j\omega\frac{T_s}{2}} \cdot \left\{ \frac{e^{j\omega\frac{T_s}{2}} - e^{-j\omega\frac{T_s}{2}}}{2j} \right\} \frac{2T_s}{\omega T_s} = T_s \cdot \frac{\sin\left(\frac{\omega T_s}{2}\right)}{\frac{\omega T_s}{2}} \cdot e^{-j\frac{\omega T_s}{2}}$$

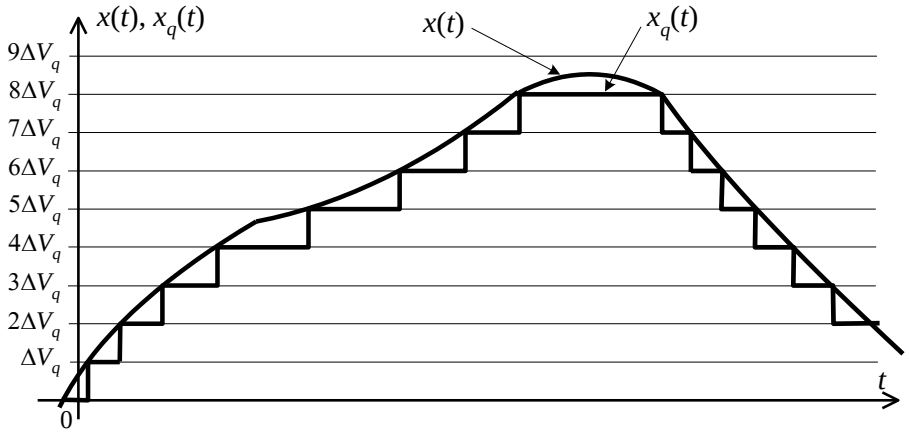
A/D modeling: Zero-Order Hold (ZOH)





Magnitude and phase characteristics for the sampling period Ts = 1

A/D modeling: Quantization and Coding



Continuous signal x(t) and its quantized value xq(t) for the case where the quantization step is ΔVq.

The voltage difference between two successive quantization levels, V_n and V_{n-1}, is the quantization step

$$\Delta V_{q,n} = V_n - V_{n-1}$$

around the n-th quantization level.

Low-frequency gain:

$$K_{A/D} = \frac{LSB_{A/D}}{\Delta V_{A/D}}$$

A/D modeling: DC Gain

For example, if the integer binary arithmetic is used, $LSB_{A/D} = 1$, and the gain of the analog to digital converter is

$$K_{A/D} = \frac{1}{\Delta V_{A/D}}$$

A/D Modeling: Processing Delay

Each of the conversion steps discussed so far introduces a certain delay. The total delay, known as the conversion time $t_{A/D}$ of the analog-to-digital converter, introduces a phase shift:

$$\angle G_{A/D}(j\omega) = \angle e^{-j2\pi\frac{f}{f_s}t_{A/D}} = -2\pi\frac{f}{f_s}t_{A/D}$$

Complete Model of the A/D converter

Using the results from the previous analysis the spectrum of an analog signal x(t), after the analog-to-digital conversion becomes:

$$X_{A/D}(j\omega) = \frac{1}{T_s}\sum_{k=-\infty}^{\infty} X\left(j(\omega - k\omega_s)\right)\cdot T_s \cdot \frac{\sin\left(\frac{\omega T_s}{2}\right)}{\frac{\omega T_s}{2}} \cdot e^{-j\frac{\omega T_s}{2}} \cdot K_{A/D} \cdot e^{-j\omega \cdot t_{A/D}}$$

For the input signal frequencies lower than the sampling frequency the expression can be simplified to include only the image of the original signal spectrum around zero (the "base band")

Model of A/D converter

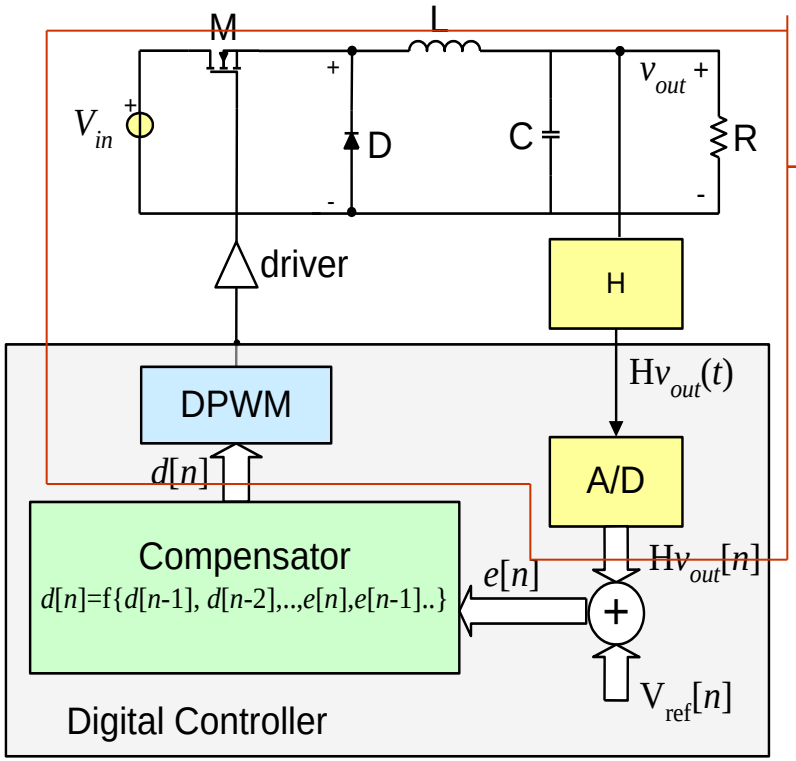
Hence, the transfer function of the analog to digital converter $G_{A/D}(j\omega)$ inside the base band is

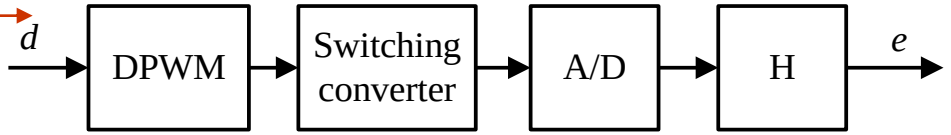
$$G_{A/D}(j\omega) = \frac{X_{A/D}(j\omega)}{X(j\omega)} = K_{A/D} \cdot \frac{\sin\left(\frac{\omega T_s}{2}\right)}{\frac{\omega T_s}{2}} \cdot e^{-j\frac{\omega T_s}{2}} \cdot e^{-j\omega \cdot t_{A/D}}$$

For $f << f_{sampling}$

$$G_{A/D}(j\omega) = \frac{X_{A/D}(j\omega)}{X(j\omega)} = K_{A/D} \cdot e^{-j\frac{\omega T_s}{2}} \cdot e^{-j\omega \cdot t_{A/D}}$$

Practical Model of Digitally Controlled SMPS





Controlled object (plant) of a digitally controlled switching regulator

$$G_{ed}(j\omega) = \frac{e(j\omega)}{d(j\omega)}$$

$$G_{ed}(j\omega) = K_{DPWM} \cdot e^{-j\omega DT_s} \cdot K_{A/D} \cdot e^{-j\omega T_{A/D}} \cdot G_{vd}(j\omega) \cdot H(j\omega)$$

Analog model of digitally controlled SMP

Selection of Compensator Coefficients

Discrete-time PID compensator

- *Discrete-time PID difference equation*

$$d[n] = d[n-1] + K_c\left(e[n] + a_1 e[n-1] + a_2 e[n-2]\right)$$

From previously described design…

- *We would like to find coefficients for the equivalent representation in the s domain*

Digitalization

Euler's Method

$$\dot{x}(t) = \frac{dx(t)}{dt} = \lim_{t\to 0}\frac{\Delta x}{\Delta t} \cong \frac{1}{T_s}\left(x(k+1) - x(k)\right)$$

$$\downarrow$$

$$L\left\{\frac{dx(t)}{dt}\right\} = sX(s)$$

This method can be used to obtain equivalent difference equation from a transformed form of a control law (s-domain)

$$d[n] = d[n-1] + K_c\left(e[n] + a_1 e[n-1] + a_2 e[n-2]\right)$$

$$\downarrow$$

$$G_{ct}(s) = \frac{\omega_k}{s}\left(1 + \frac{1}{Q_{cmp}}\frac{s}{\omega_z} + \left(\frac{s}{\omega_z}\right)^2\right)$$

Discrete-Time Z-Transform

- *The z-transform is a discrete-time, sampled-data dual of the Laplace transform, which contains duals of all the well known characteristics*

Z-Transform: $V_c(z) = \sum_{n=-\infty}^{\infty} v_c[n] z^{-n}$

The Laplace Transform: $V_c(s) = \int_{-\infty}^{\infty} v_c(t) e^{-st} dt$

Note that for $\underline{z = e^{sT}}$ *the z-transform has the form of a sampled version of the Laplace*

$$V_c(e^{sT}) = \sum_{n=-\infty}^{\infty} v_c(nT) e^{-snT}$$

Discrete-time PID compensator

- *Discrete-time PID difference equation*

$$d[n] = d[n-1] + K_c\left(e[n] + a_1 e[n-1] + a_2 e[n-2]\right)$$

Discrete-time and continuous time equivalent PID transfer functions

$$G_c(z) = \frac{d_c}{e} = K_c \frac{1 + a_1 z^{-1} + a_2 z^{-2}}{1 - z^{-1}}$$

$$G_{ct}(s) = \frac{\omega_k}{s}\left(1 + \frac{1}{Q_{cmp}}\frac{s}{\omega_z} + \left(\frac{s}{\omega_z}\right)^2\right)$$

- *The discrete-time pole at 1 corresponds to the continuous-time pole at zero. As a result, the compensator has infinite dc gain, i.e. the steady-state error e is zero*
- *The compensator has two zeros to provide the necessary phase lead*

Discrete-time PID compensator design based on analog template

$$G_c(z) = K_c \frac{1 + a_1 z^{-1} + a_2 z^{-2}}{1 - z^{-1}} \quad \Longleftrightarrow \quad G_{ct}(s) = \frac{\omega_k}{s}\left(1 + \frac{1}{Q_{cmp}}\frac{s}{\omega_z} + \left(\frac{s}{\omega_z}\right)^2\right)$$

- *Given Gct(s), i.e. by knowing how we would like our compensator in s-domain, Gc(z) can be obtained using one of a number of possible continuous-to-discrete time mapping techniques*
- *For example, we can apply the pole-zero matching technique:*

$$z = e^{s\,T}$$

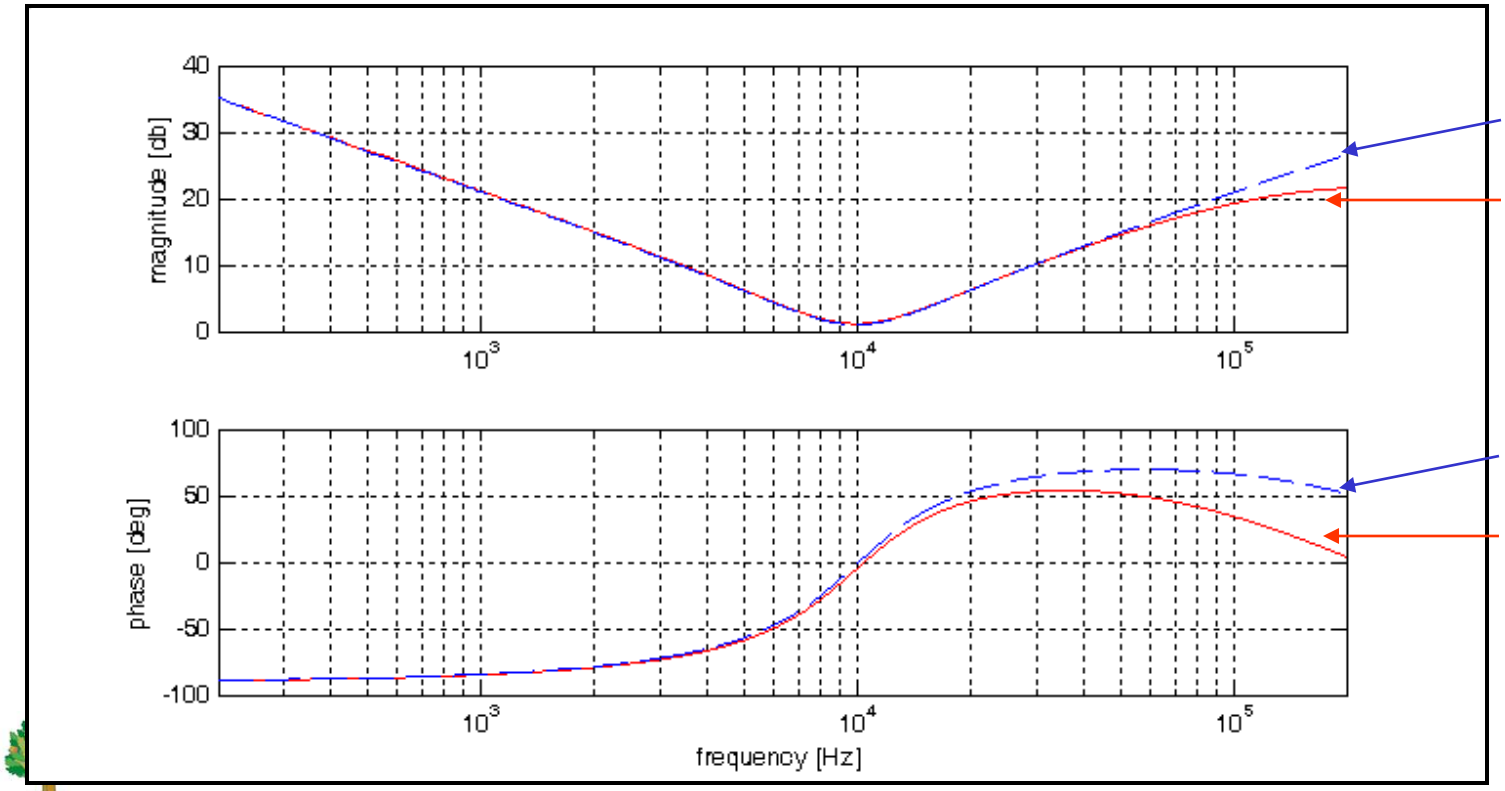
- *T is the sampling period (equal to the switching period $T_s = 1/f_s$ in our example)*
- *Equations:*

$$r = e^{-\pi f_z/(Q_{cmp} f_s)} \qquad a_1 = -2r\cos\left(2\pi \frac{f_z}{f_s}\sqrt{1 - \frac{1}{4Q_{cmp}^2}}\right) \qquad a_2 = r^2$$

K_c is selected so that the magnitude $||G_c||$ matches the magnitude $||G_{ct}||$ at a selected frequency (the cross-over frequency, for example)

Example

$$G_{ct}(s) = \frac{\omega_k}{s}\left(1 + \frac{1}{Q_{cmp}}\frac{s}{\omega_z} + \left(\frac{s}{\omega_z}\right)^2\right) \longrightarrow G_c(z) = K_c \frac{1 + a_1 z^{-1} + a_2 z^{-2}}{1 - z^{-1}}$$



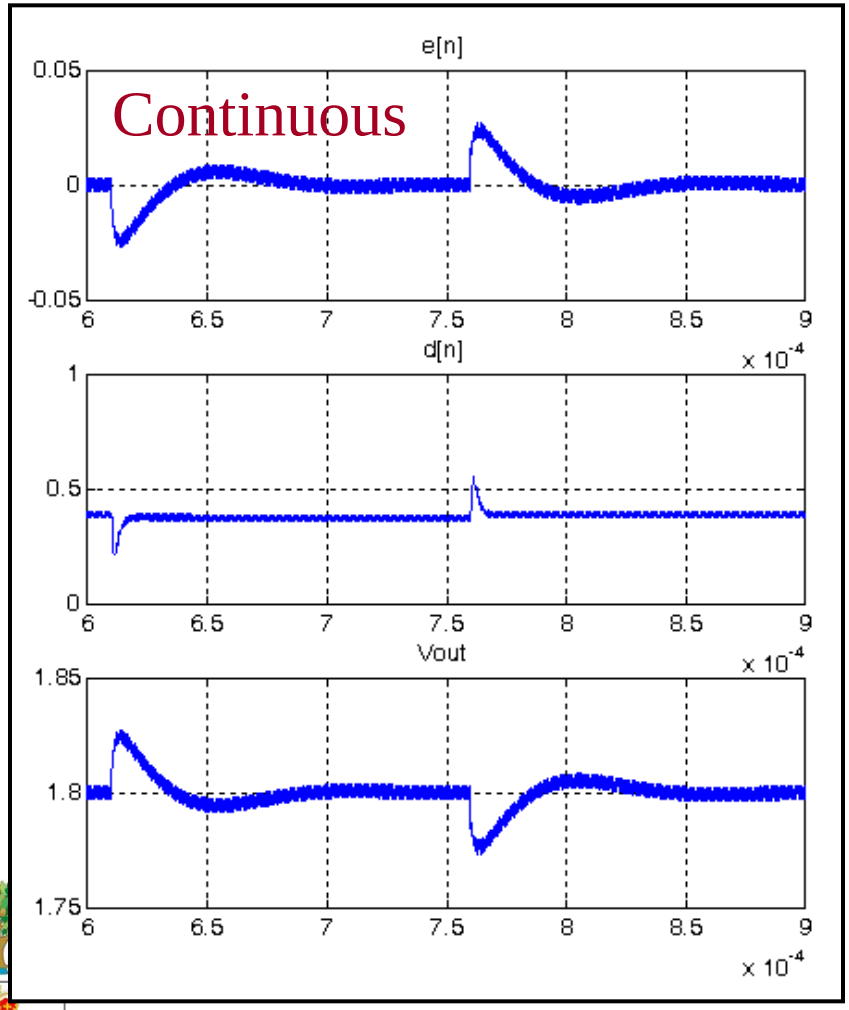
$G_c(j\omega)$ (cont)

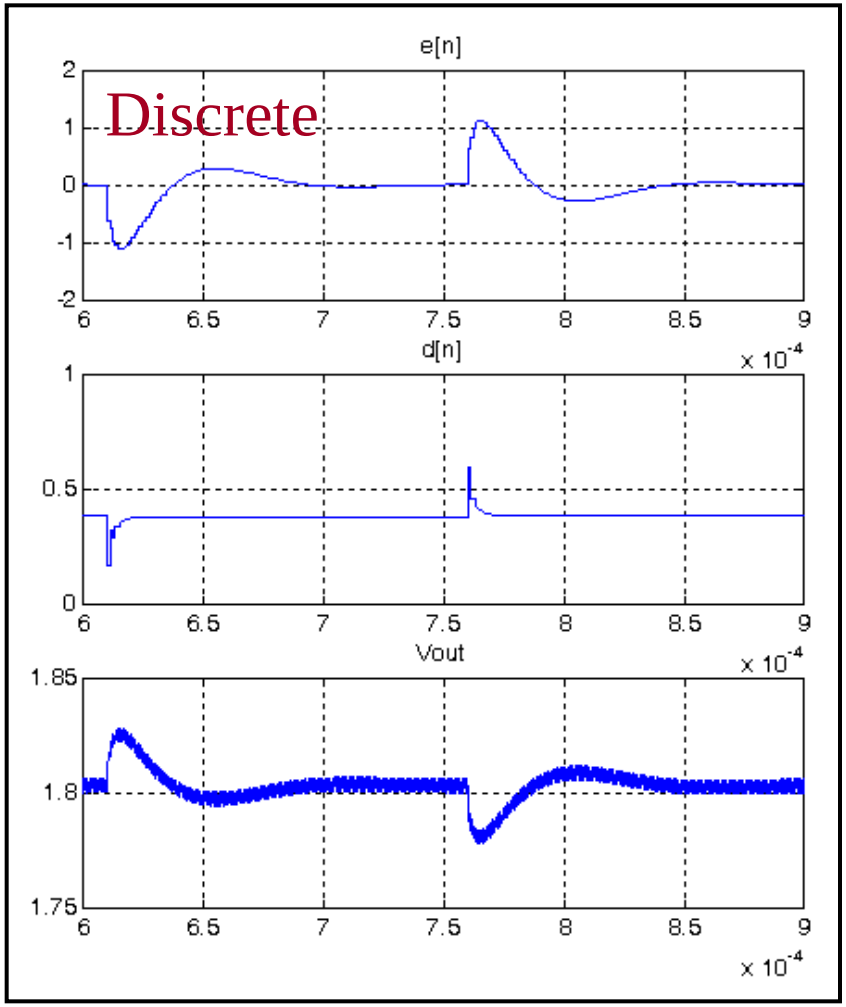
$G_{ct}(j\omega)$ (discrete)

$G_c(j\omega)$ (cont)

$G_{ct}(j\omega)$ (discrete)

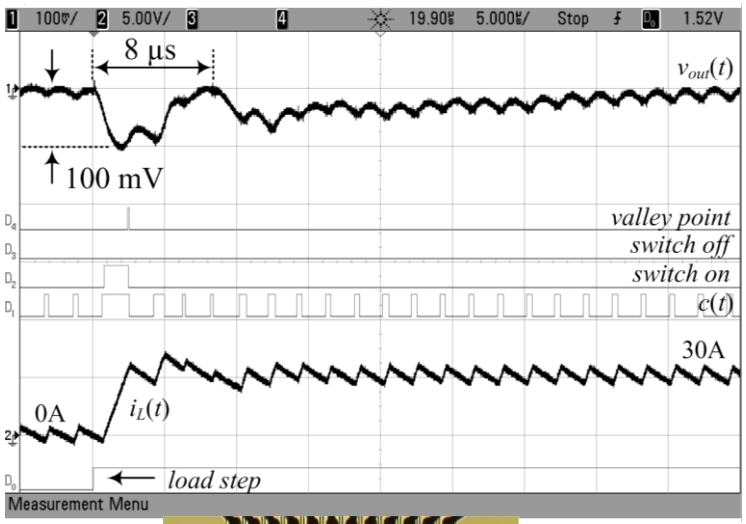
Load transient responses 50% → 100%

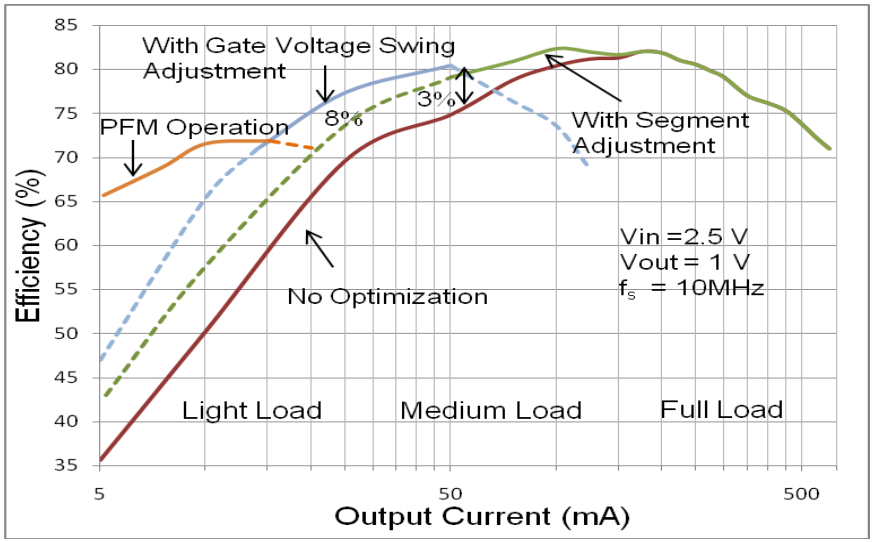


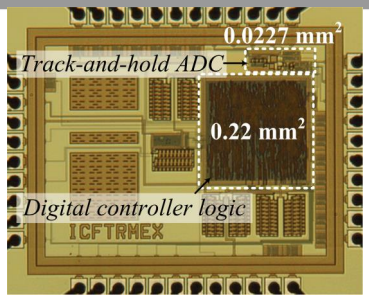


➢Near identical response!

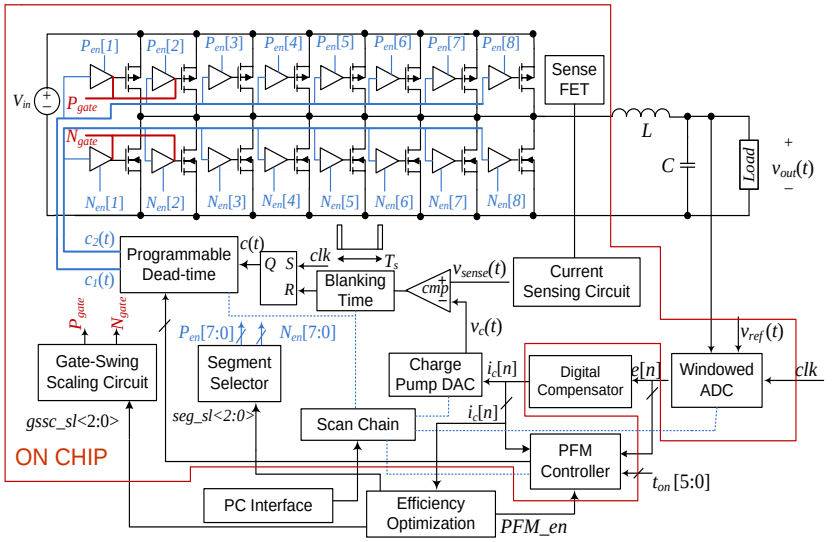
Day 2: Preview (Advanced Controllers)



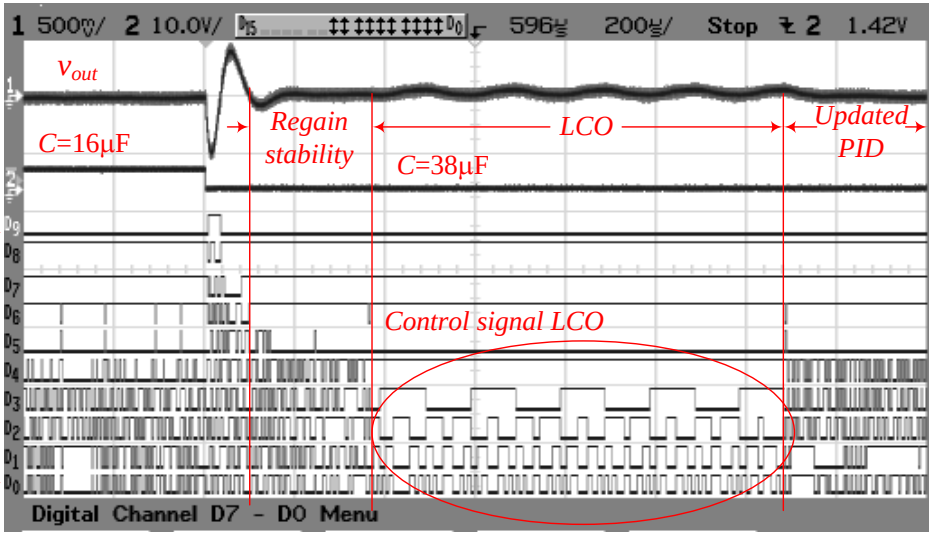


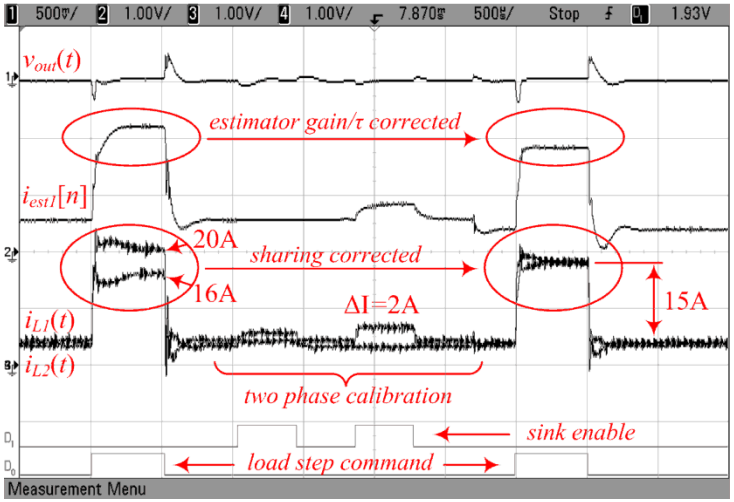


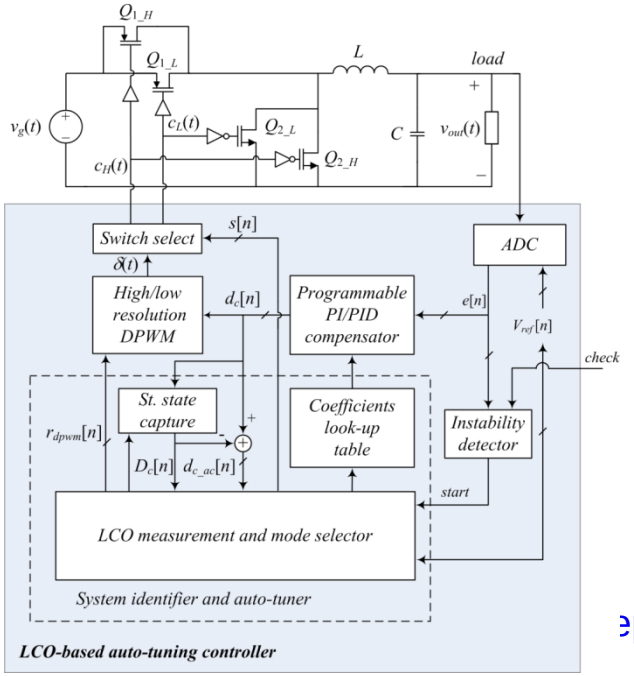
Digital controllers with the fastest possible transient response and virtually flat efficiency curve

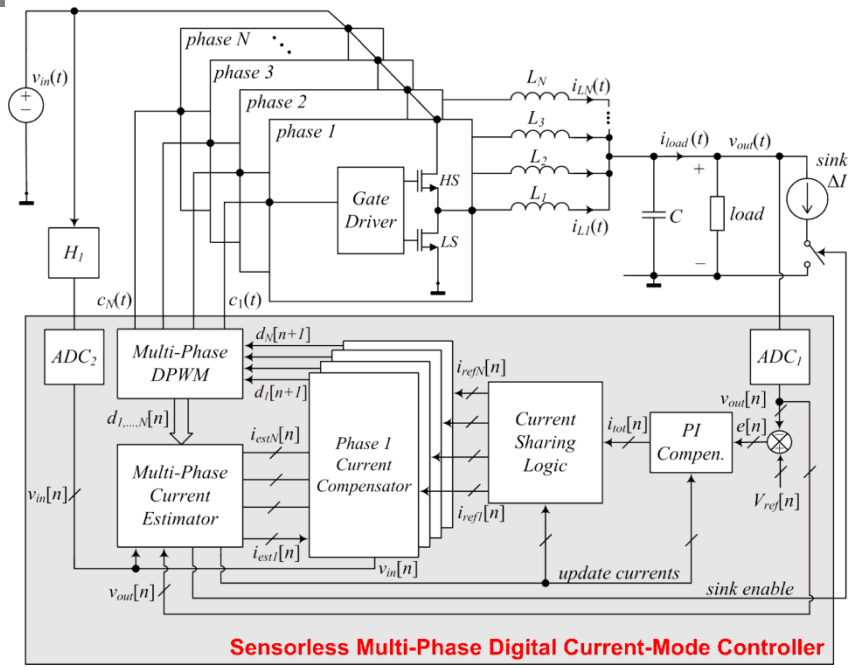


Day 2: Preview (Advanced Controllers)



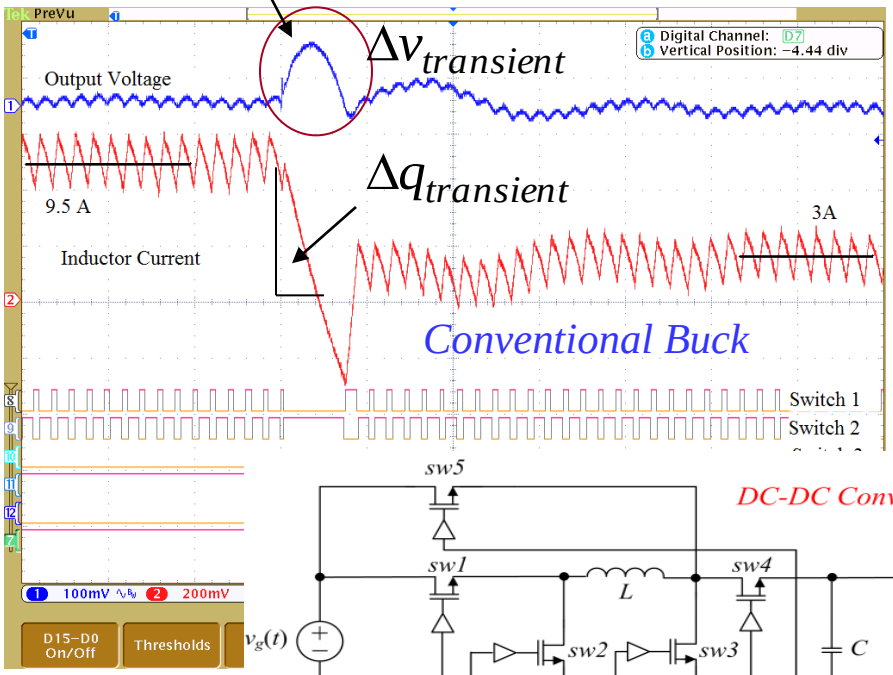


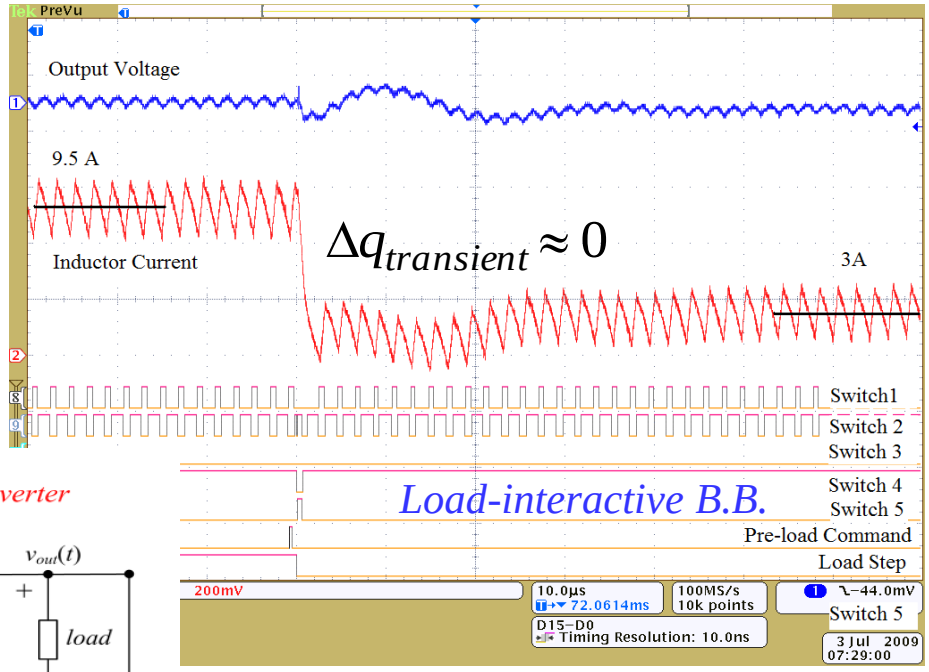


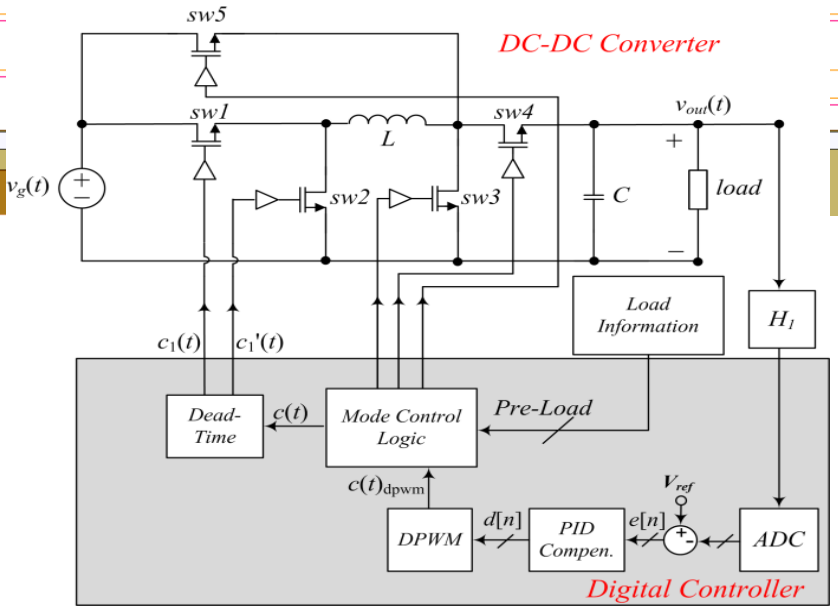


epartment

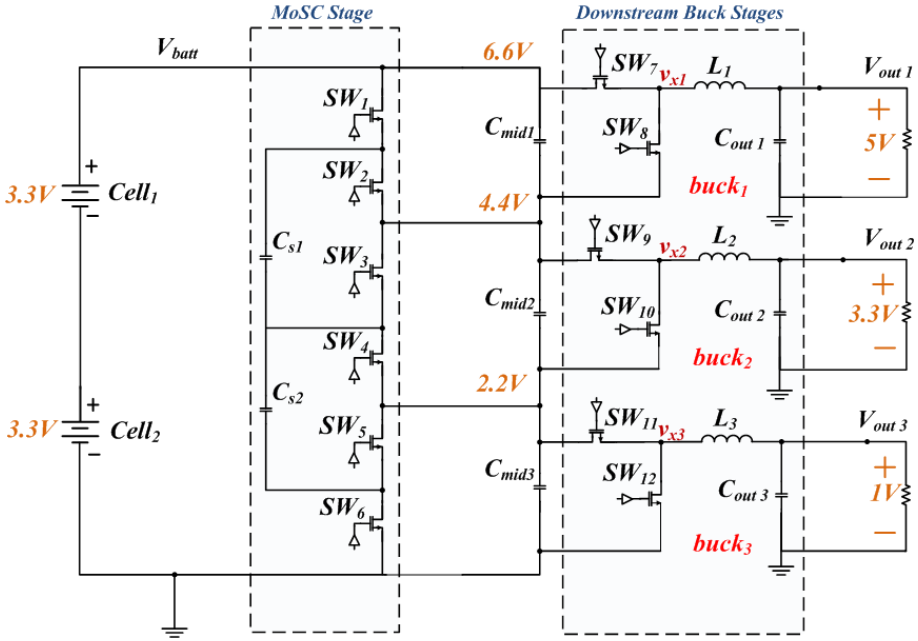
Day 2: Preview (Emerging Topologies)

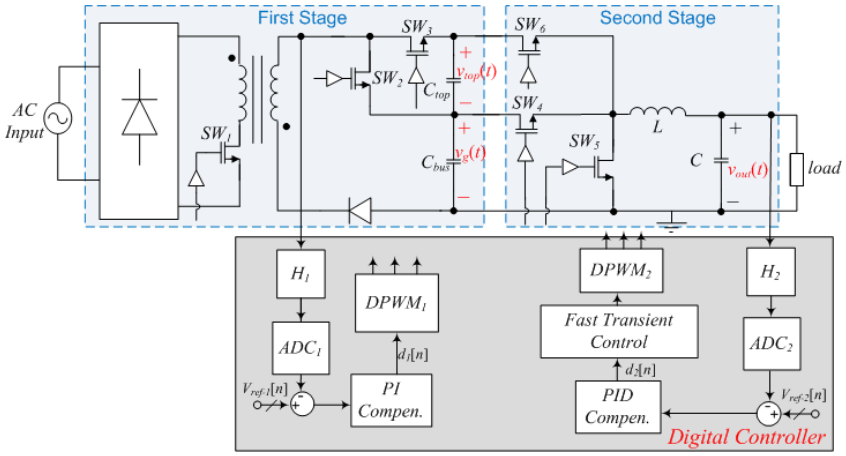






Day 2: Preview (Emerging Topologies)

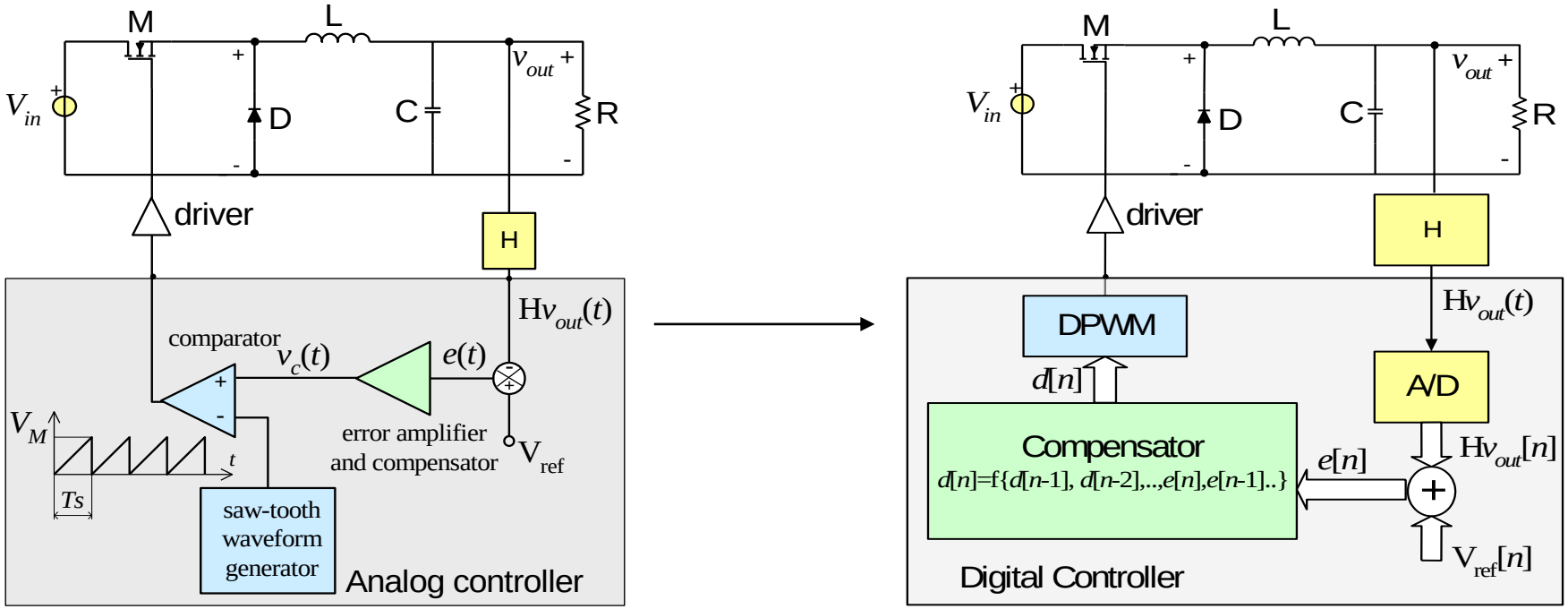




Part III

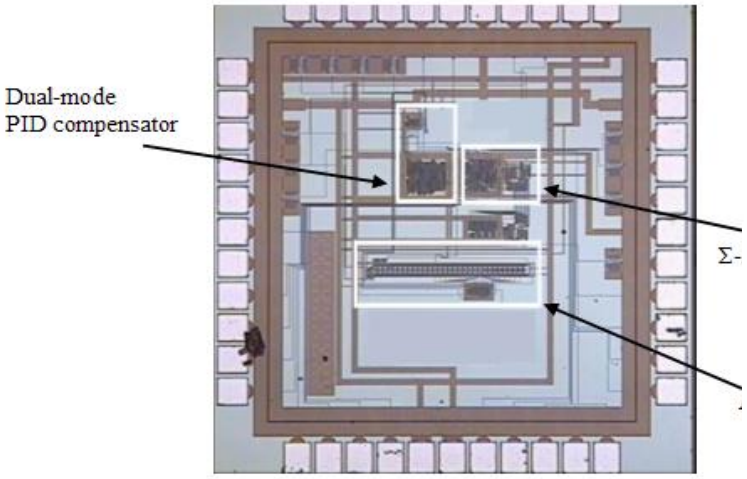
Advanced Controllers for Dc-Dc and Rectifiers with Power Factor Correction (Reaching the Physical Limits of Conventional Topologies)

Digital (Mixed-Signal) Control as Enabling Technology

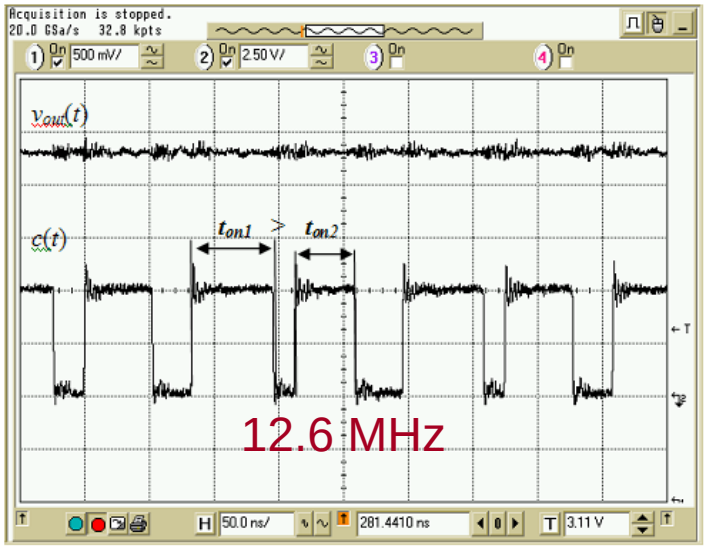


- *In the past high-frequency digital controllers were not available*
- *Digital high-frequency IC control solutions are available today*
- *Replacing analog with digital without using advantages of the digital is not sufficient*
- *Digital controllers that improve performance of SMPS (advanced controllers) will be presented here*

Progress of Digital Control: Ultra High-Frequency Digital Controller IC (Beyond 100 MHz)



DPWM switching frequency	Programmable, 400 kHz to 150 MHz
DPWM effective resolution	10-bit
Silicon area	0.14 mm^2



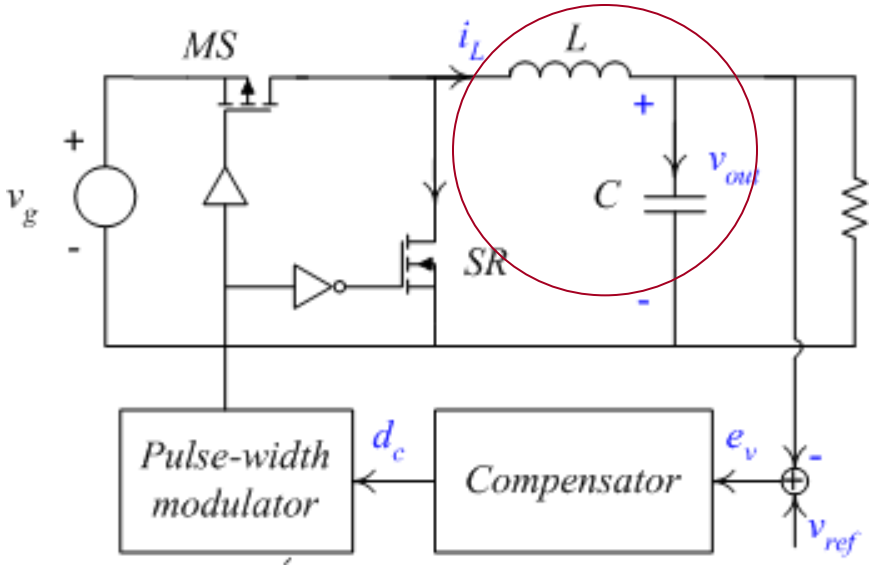
Area, speed and power as good as analog or even better

Digital controllers today can operate at higher switching frequencies than what the switching components can support (necessary condition).

[2] Z. Lukić, N. Rahman, and A. Prodić, "Multi-Bit Sigma-Delta PWM Digital Controller IC for Dc-Dc Converters Operating at Switching Frequencies Beyond 10 MHz," IEEE Trans. on Power Electronics, Sep. 2007, Vol.22, Iss. 5

Digital Control and Physical Limitations

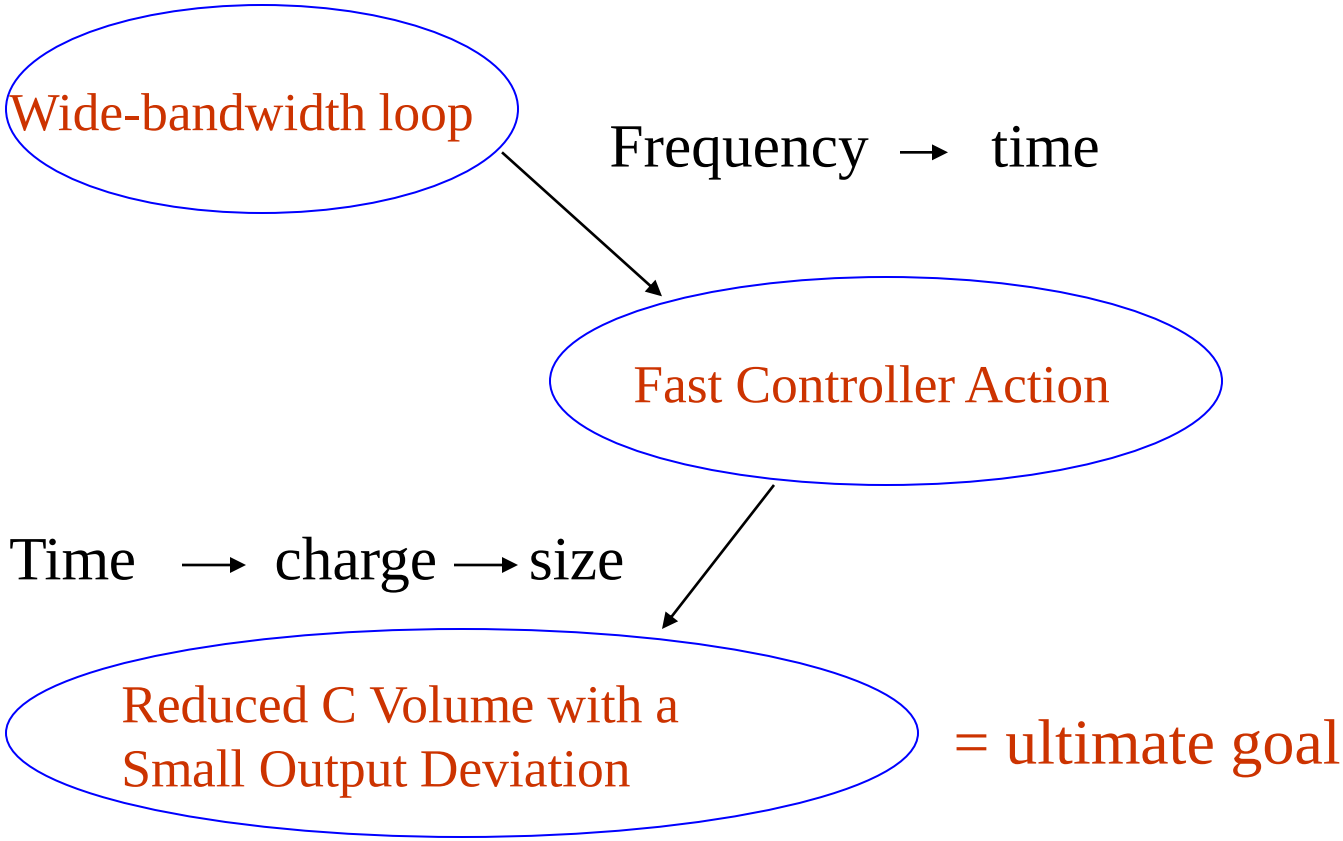
- Operation at high switching frequencies ✔
- Fast dynamic response of the controller ⬅focus



Load current

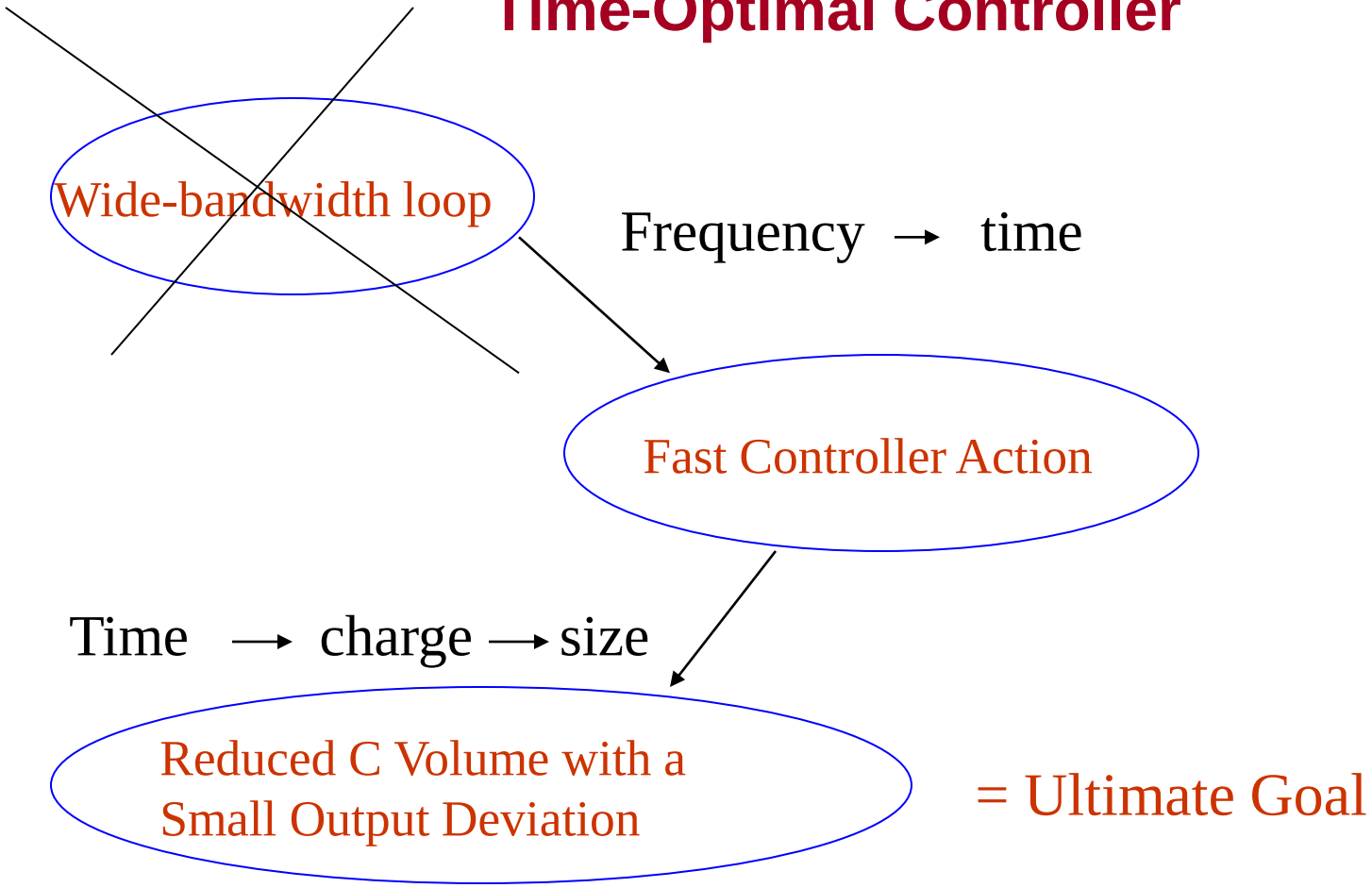
The size of the output capacitor strongly depends on the speed of the controller response

Conventional Controller Design



Design approach limitations: The modeling method includes bandwidth limitations (affects the speed of the controller)

Time-Optimal Controller



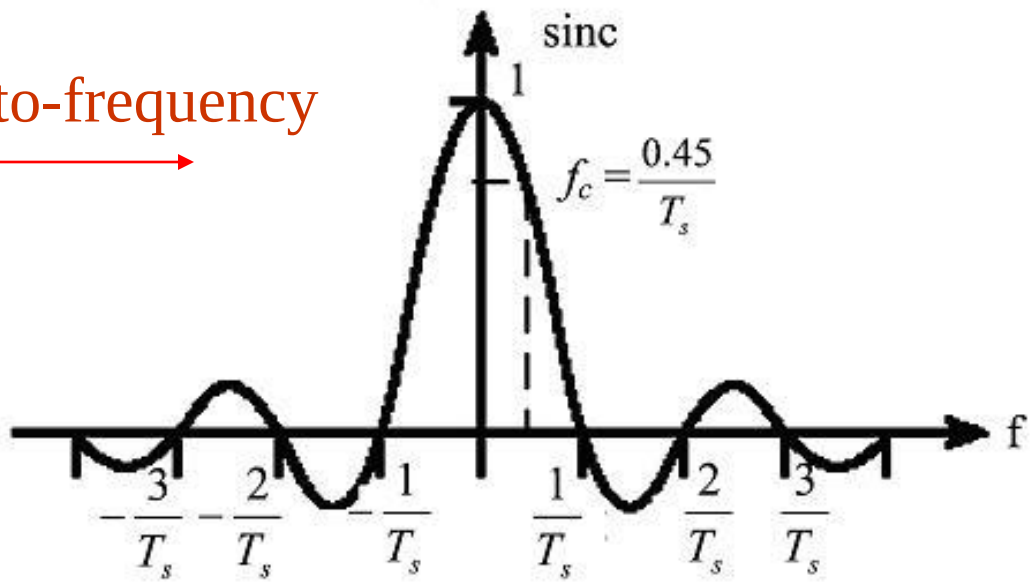
*The idea is **to use computational features** that digital control offers to improve dynamic performance, i.e. reduce the output capacitor size.*

Limitations of Frequency Design Based Controllers

$$\langle i_L(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt$$

$$\langle v(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{T_s} v(t)dt$$

Time-to-frequency



Mathematical tool used to approximately describe filtering effect of the power stage reactive components, works relatively good for output voltage, far from perfect for current and switches waveforms.

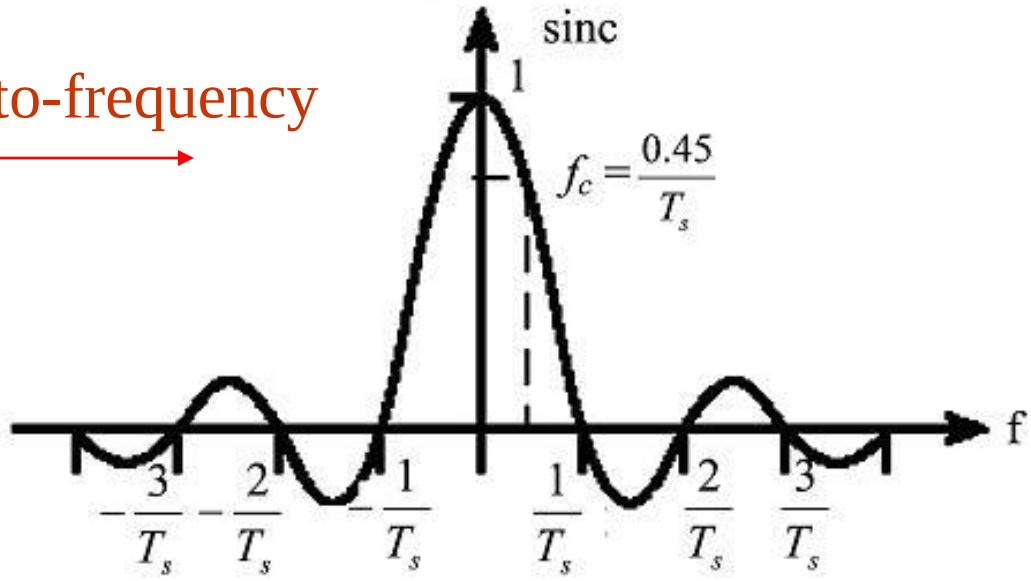
Limitations of Frequency Design Based Controllers

- *Valid for frequencies much smaller than the switching frequency, approximately up to $f_{sw}/10$. Still very efficient in ripple elimination.*

$$\langle i_L(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt$$

$$\langle v(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{T_s} v(t)dt$$

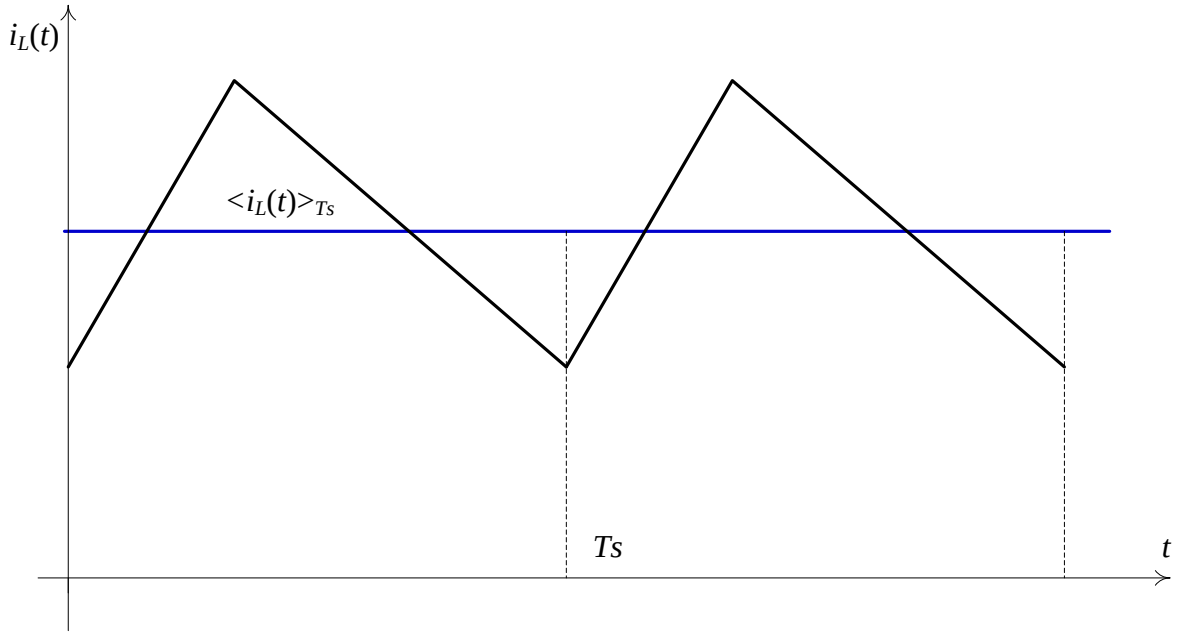
Time-to-frequency



- *The analysis is applicable for small variations around a steady state operating point*

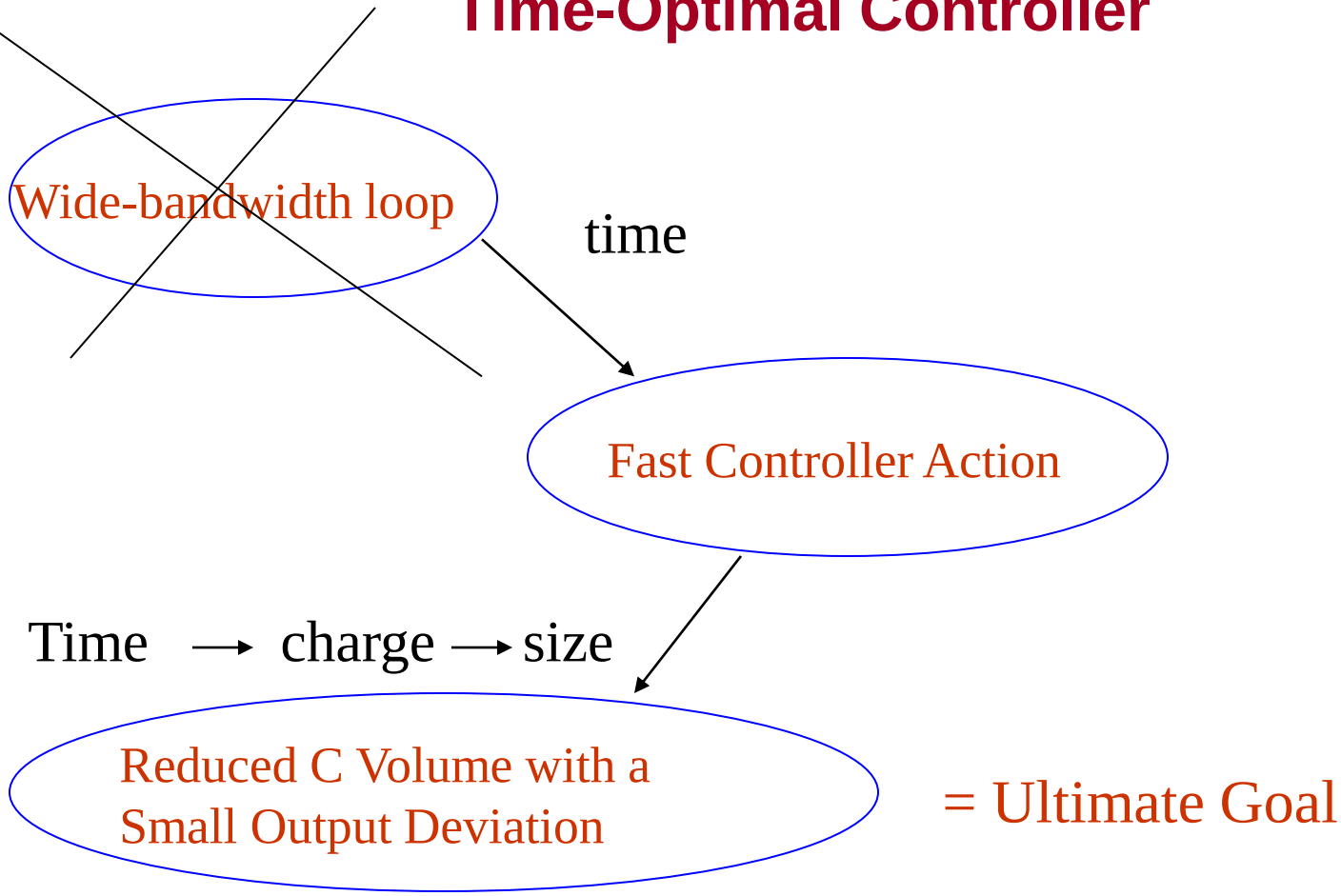
- *Also means that the controller by its nature has limited speed and the validity of modeling approach for large changes is questionable*

Limitations of Frequency Design Based Controllers



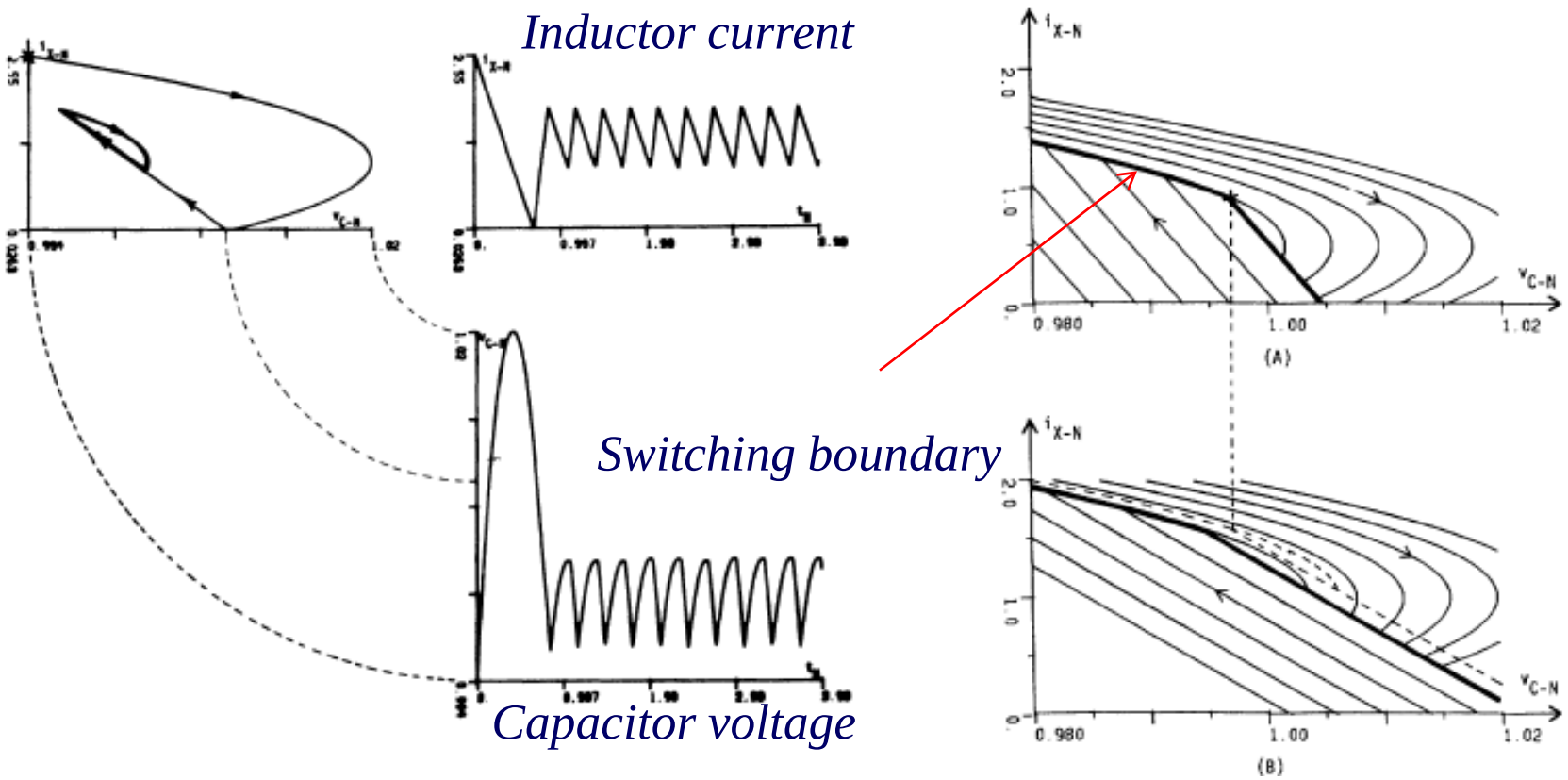
By averaging the current ripple, which in modern SMPS cannot be considered negligible is eliminated (for some converters and full loads we throw away about 40% of current from calculations)

Time-Optimal Controller



*The idea is **to use computational features** that digital control offers to improve dynamic performance, i.e. reduce the output capacitor size.*

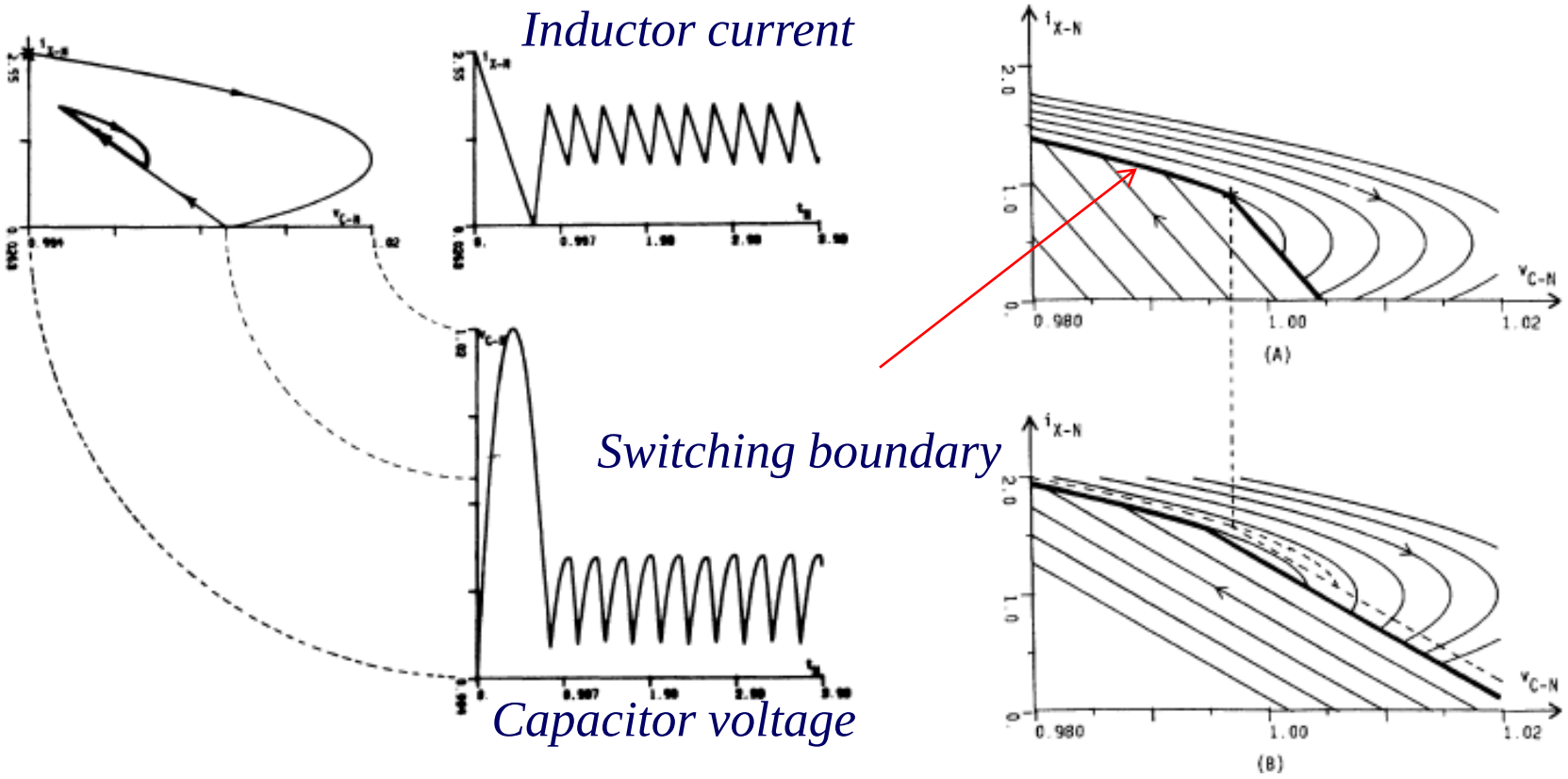
Time-Optimal Control, i.e. Geometric Control[1]



Simultaneous analysis of instantaneous waveforms (rather than average) in state-plane is performed to determine time-optimal switching sequence

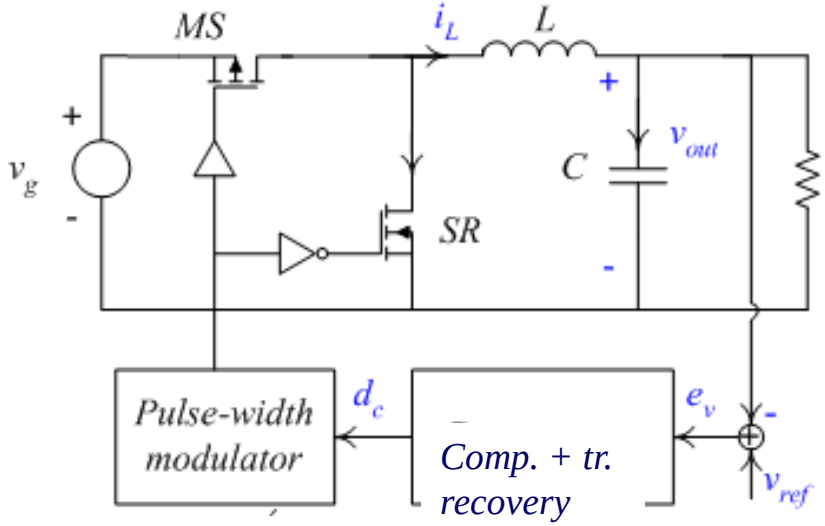
[1] W. Burns, T. Wilson "A State-Trajectory Control Law for DC-to-DC Converters", IEEE Transactions on Aerospace and Electronic Systems, January, 1978.

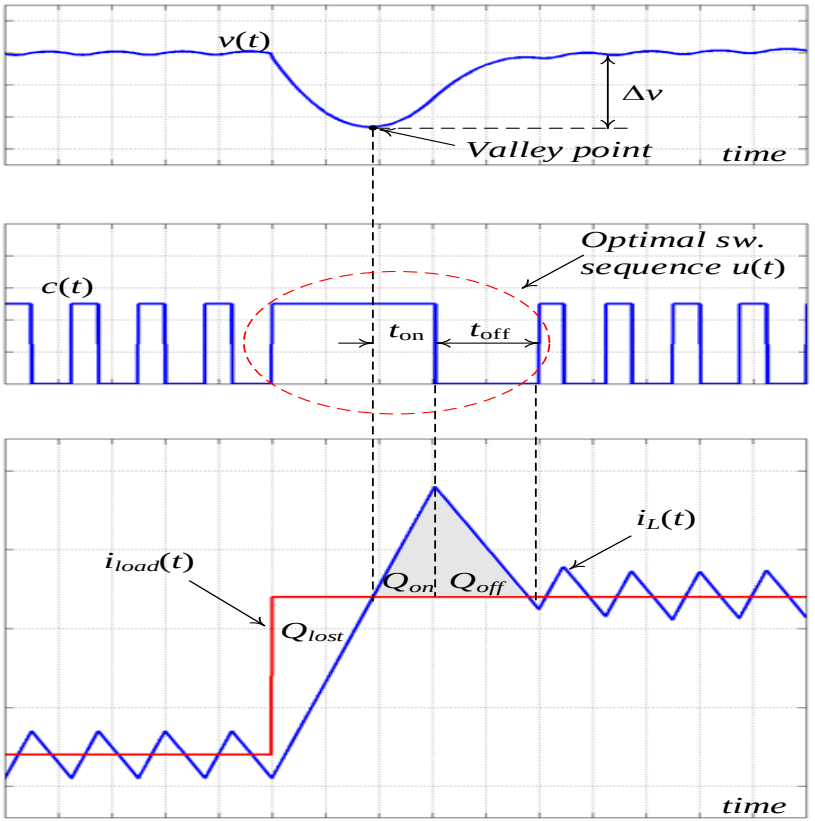
Time-Optimal Control, i.e. Geometric Control[1]



The method has been known for almost 40 years, however due to large computational complexity, has not been adopted in high-frequency applications. Calculation of the curves (trajectories) is very demanding.

Charge Based (Mixed-Signal) Time-Optimal Response





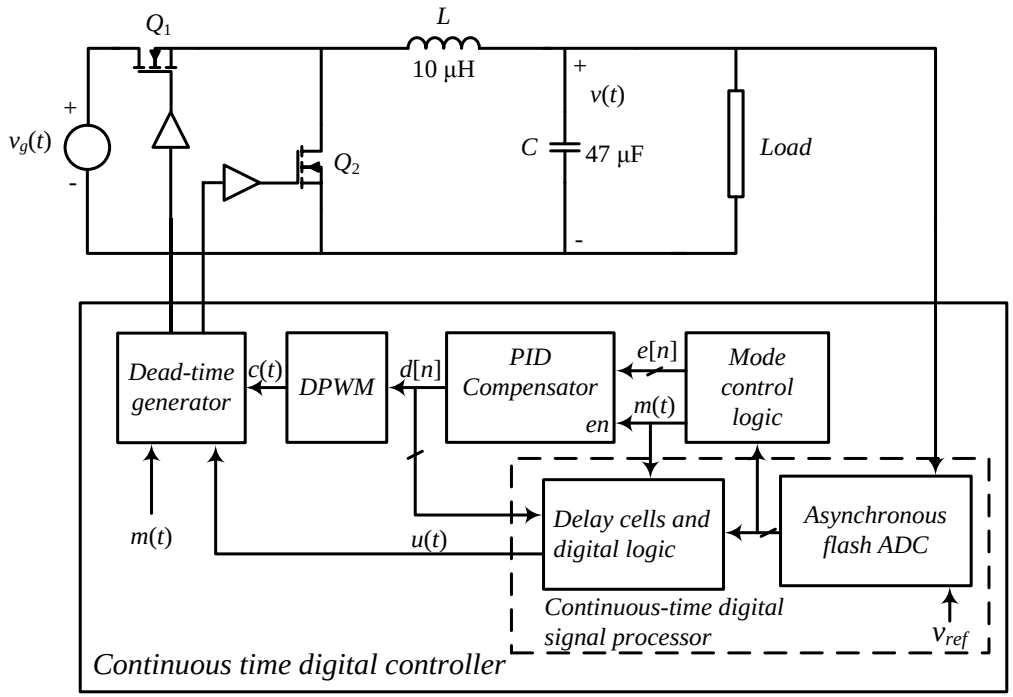
$$Q_{lost} = Qon + Qoff$$

$$Q = C\Delta V$$

Simpler computational logic, based on charge replacement and calculations of t_{on} and t_{off} times. Transient suppression logic active during transients only.

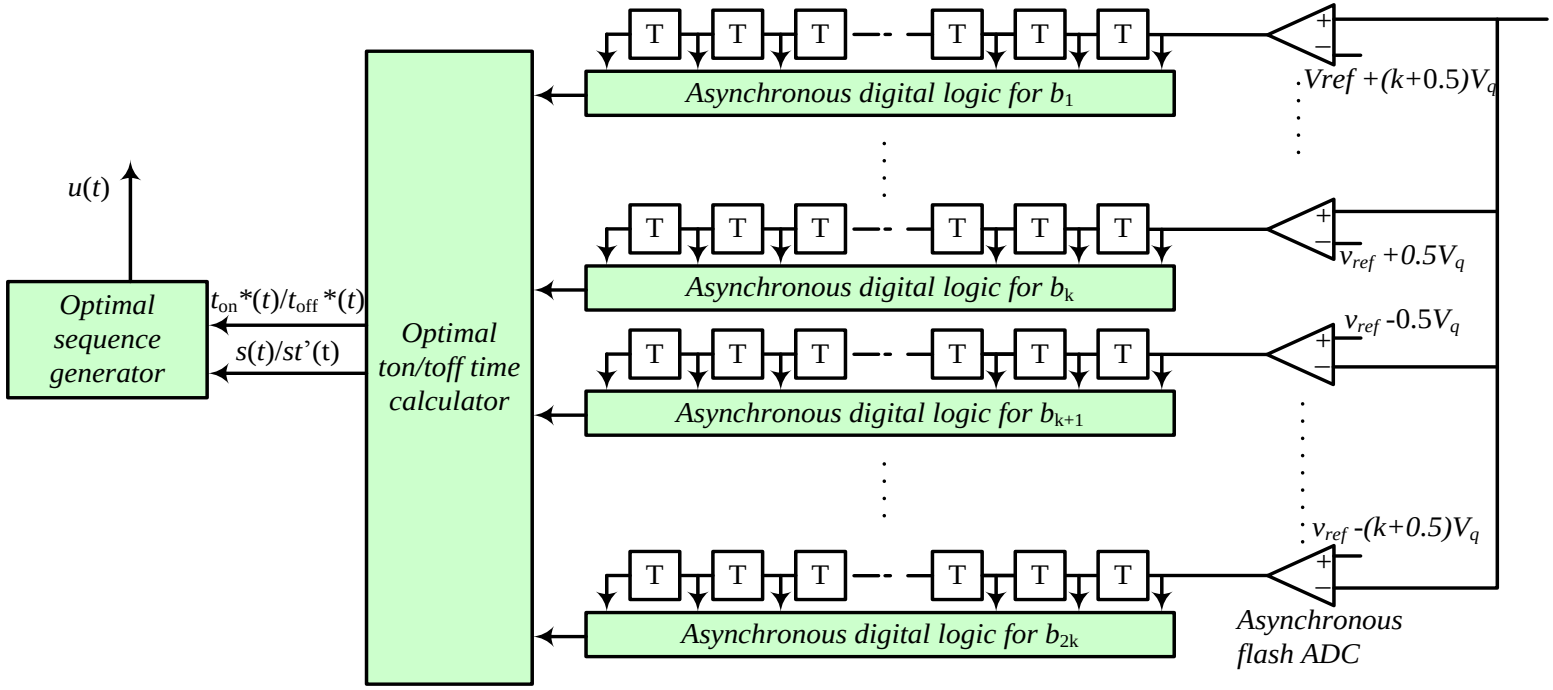
[1] F. Guang, E. Meyer, Y.-F. Liu, "A New Digital Control Algorithm to Achieve Optimal Dynamic Performance in DC-to-DC Converters," Power Electronics, IEEE Transactions on , vol.22, no.4, pp.1489-1498, July 2007.

Continues-time Digital Controller Reaching the Physical Limitations of a Given Power Stage



- *In steady state the controller operates as a conventional voltage-mode PWM system*
- *CT-DSP reacts during transients*

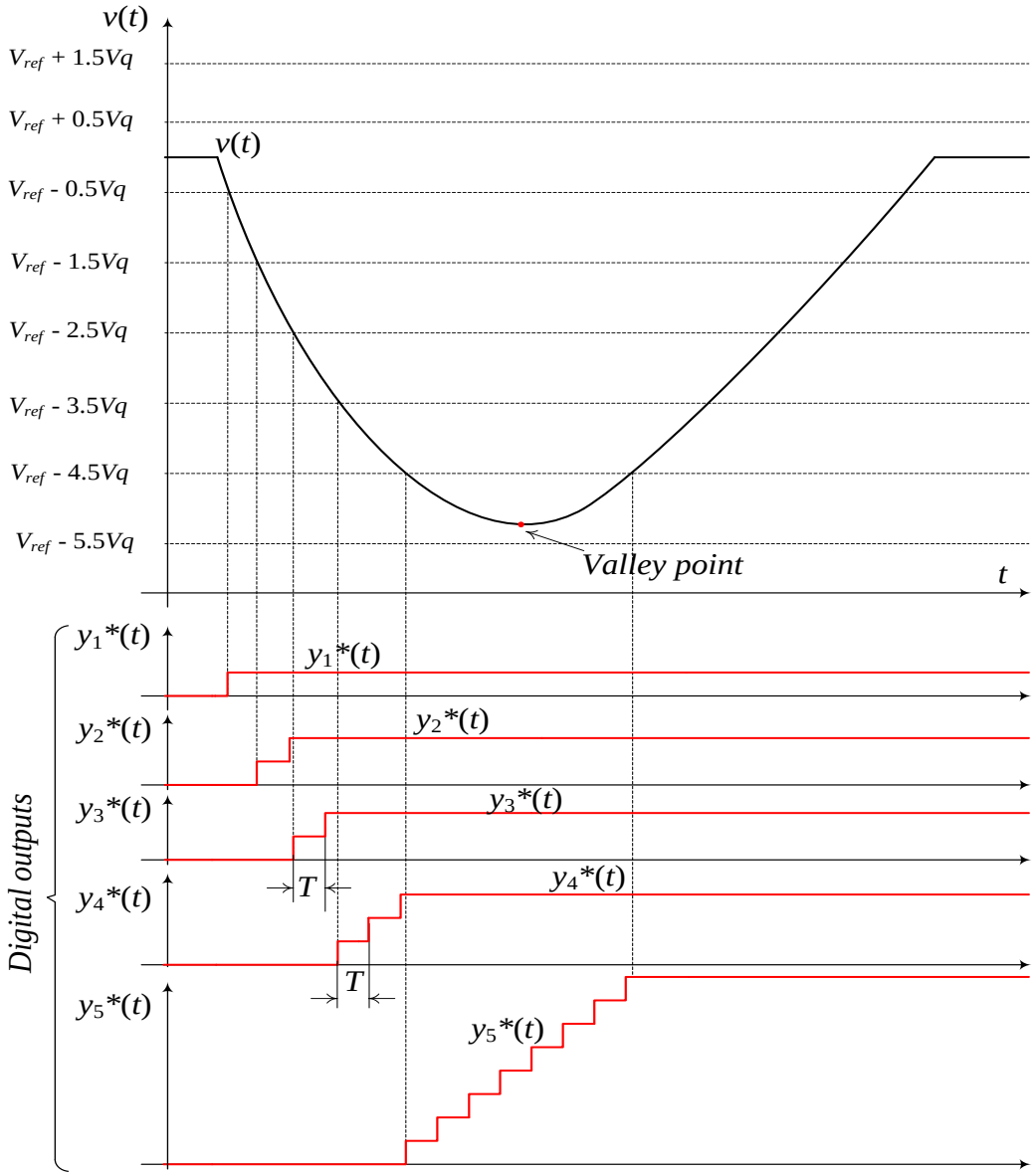
Mixed-signal Architecture Example: Continuous-Time Digital Controller



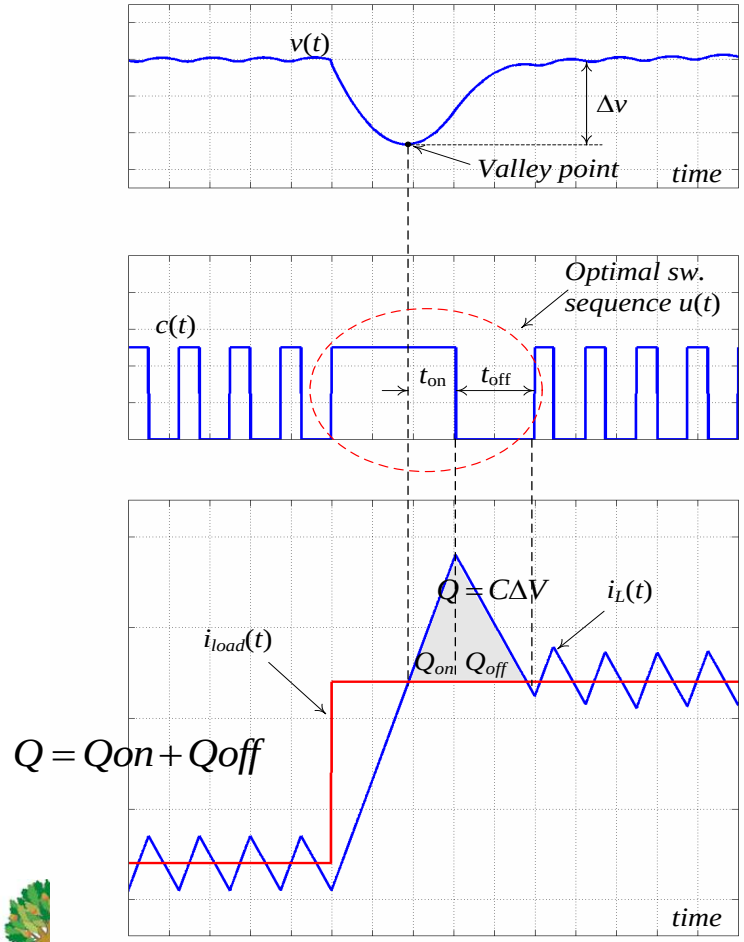
- *Continuous-time digital processor (CT-DSP) used as a combined windowed ADC and optimal sequence calculator.*
- *Takes voltage "snapshot" during transients and calculates the sequence accordingly.*

Capturing a Snapshot

- Valley point and its amplitude are captured (to calculate Q)
- Valley point is also used to get the time reference for calculation of t_{on} and t_{off} times (previous slide)
- Post processing used to improve accuracy, i.e. minimize discretization effects (both in time and amplitude)

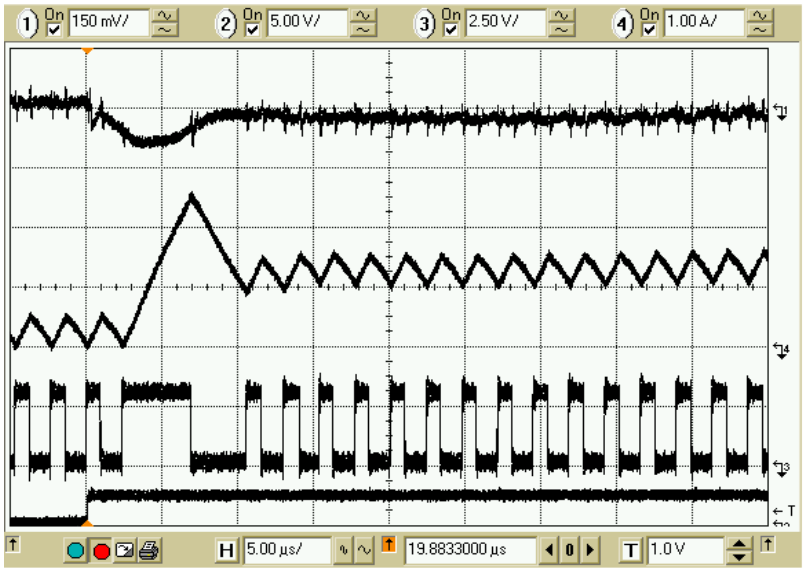


CT-DSP Algorithm and Experimental System Performance



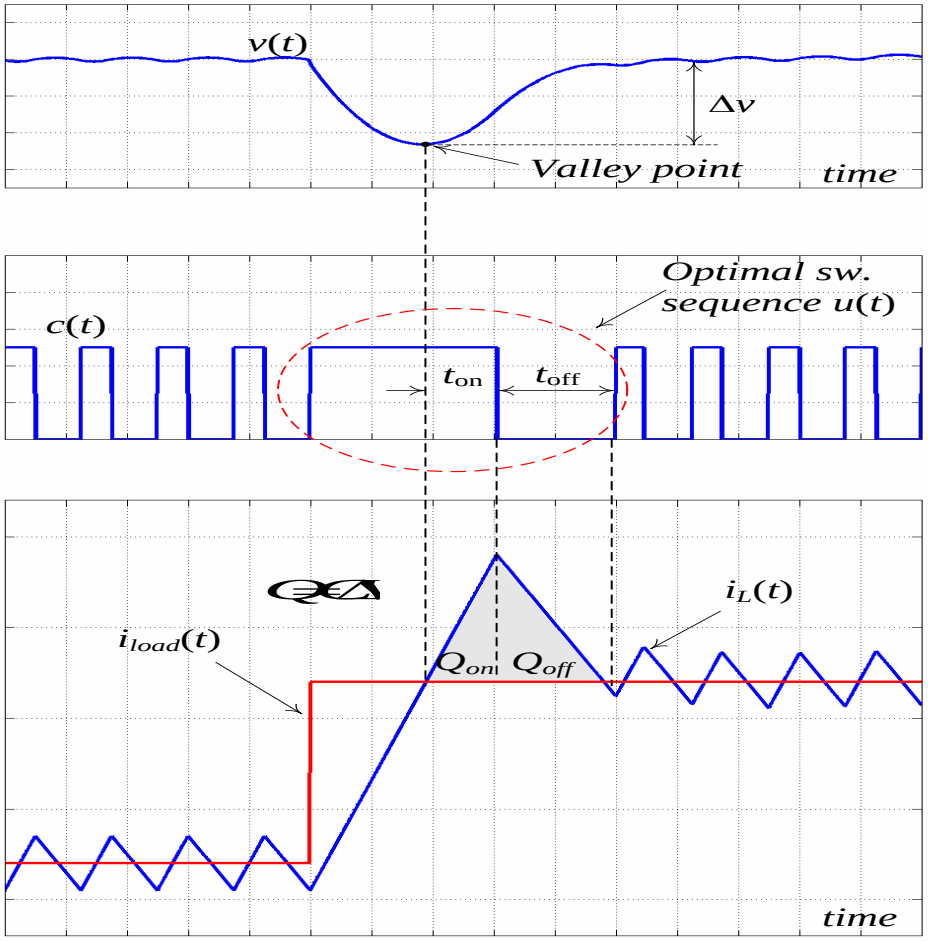
Optimal response theoretical waveforms

Optimal response experimental waveforms



Transient response of an experimental 2 A, 400 kHz system for a 10 % to 60 % load change.

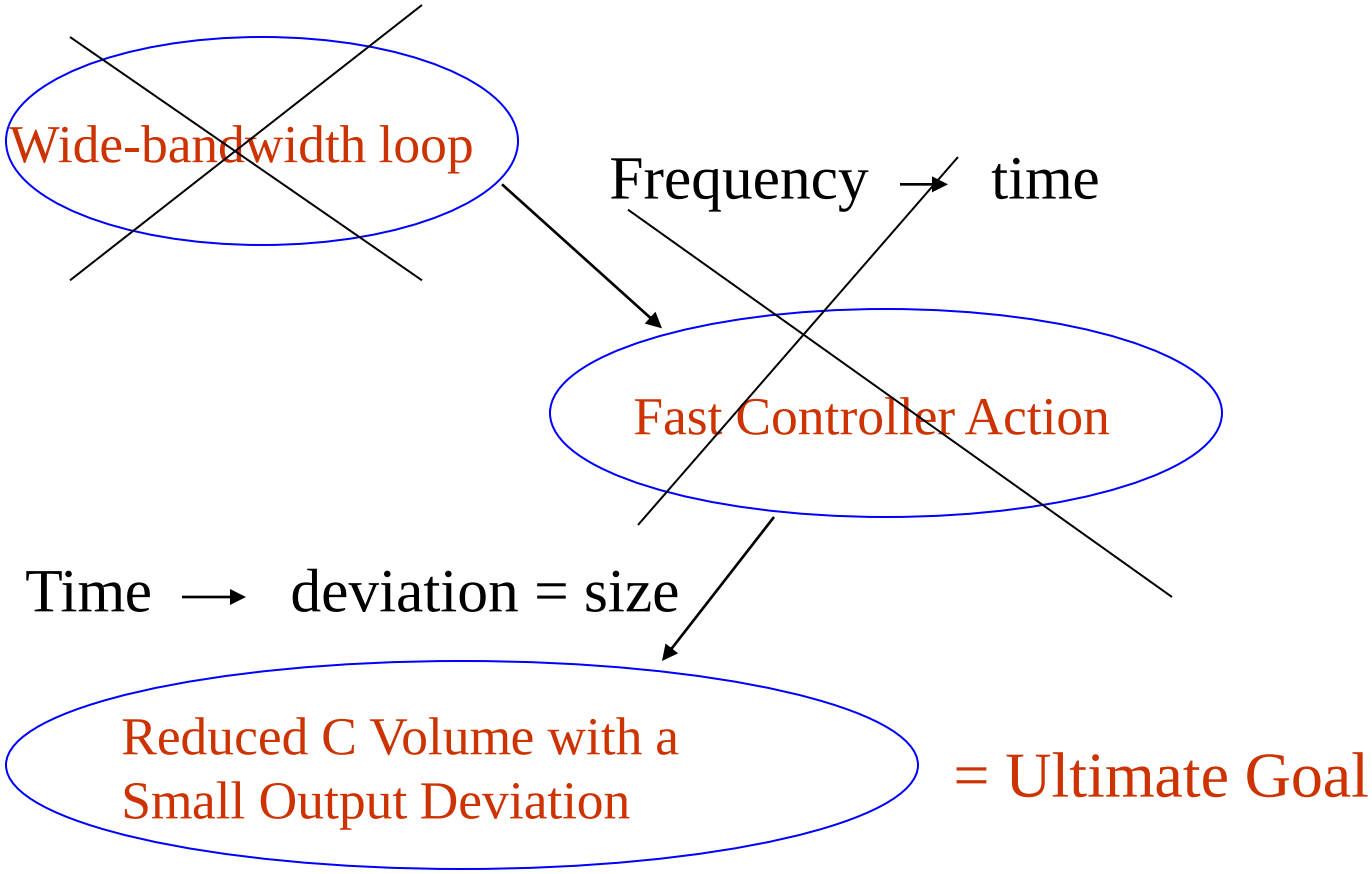
Drawbacks of Time-Optimal Control Methods



- Large peak inductor current, i.e. inductor might need to be over designed
- In some cases, need to know LC values or to have a very high resolution ADC[1]
- Relatively complex calculations and sensitivity to delay

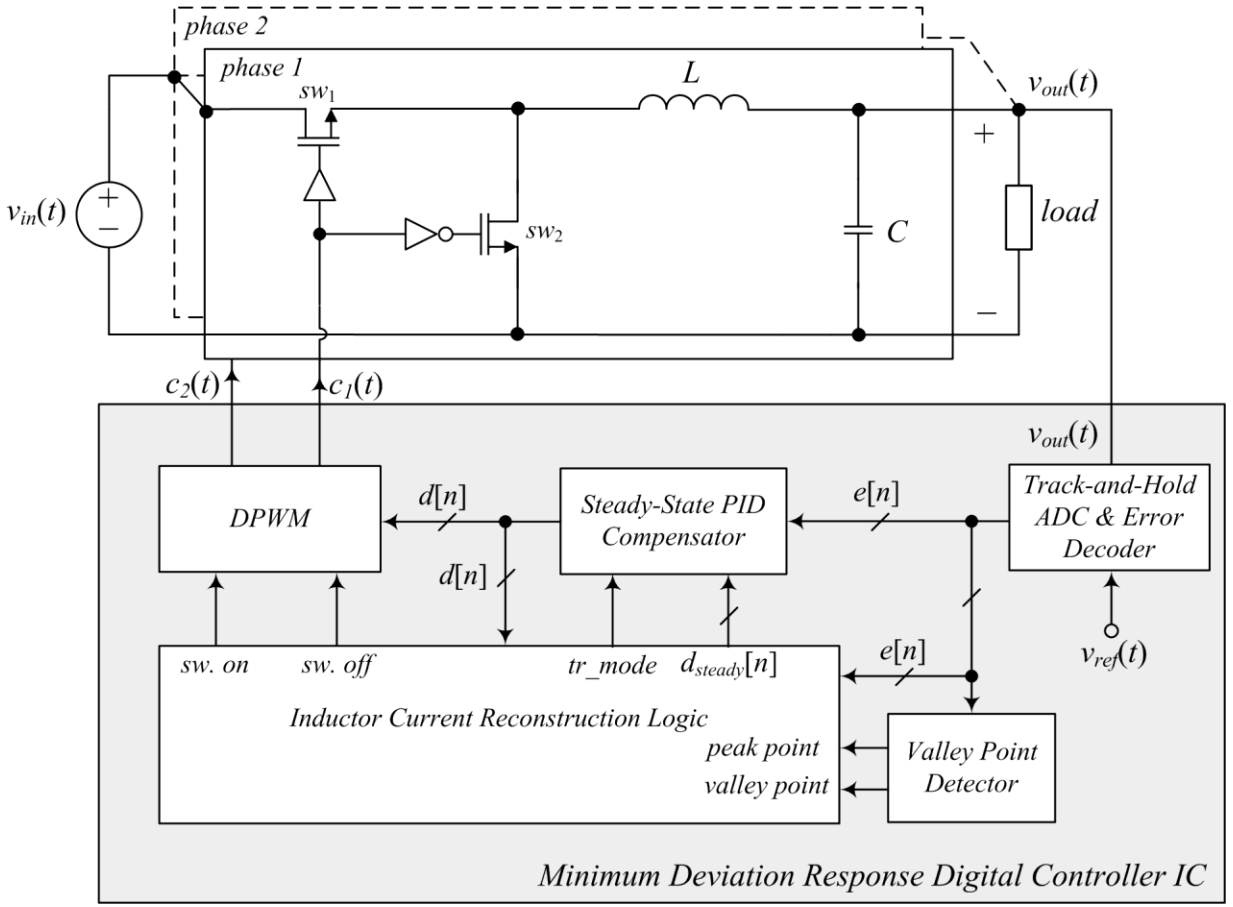
[2] A. Costabeber, L. Corradini, P. Mattavelli, and S. Saggini, "Time optimal, parameters-insensitive digital controller for DC-DC buck converters," in *Proc. IEEE Power Electronics Specialist Conf.*, 2008, pp. 1243–1249.

Minimum Deviation Controller



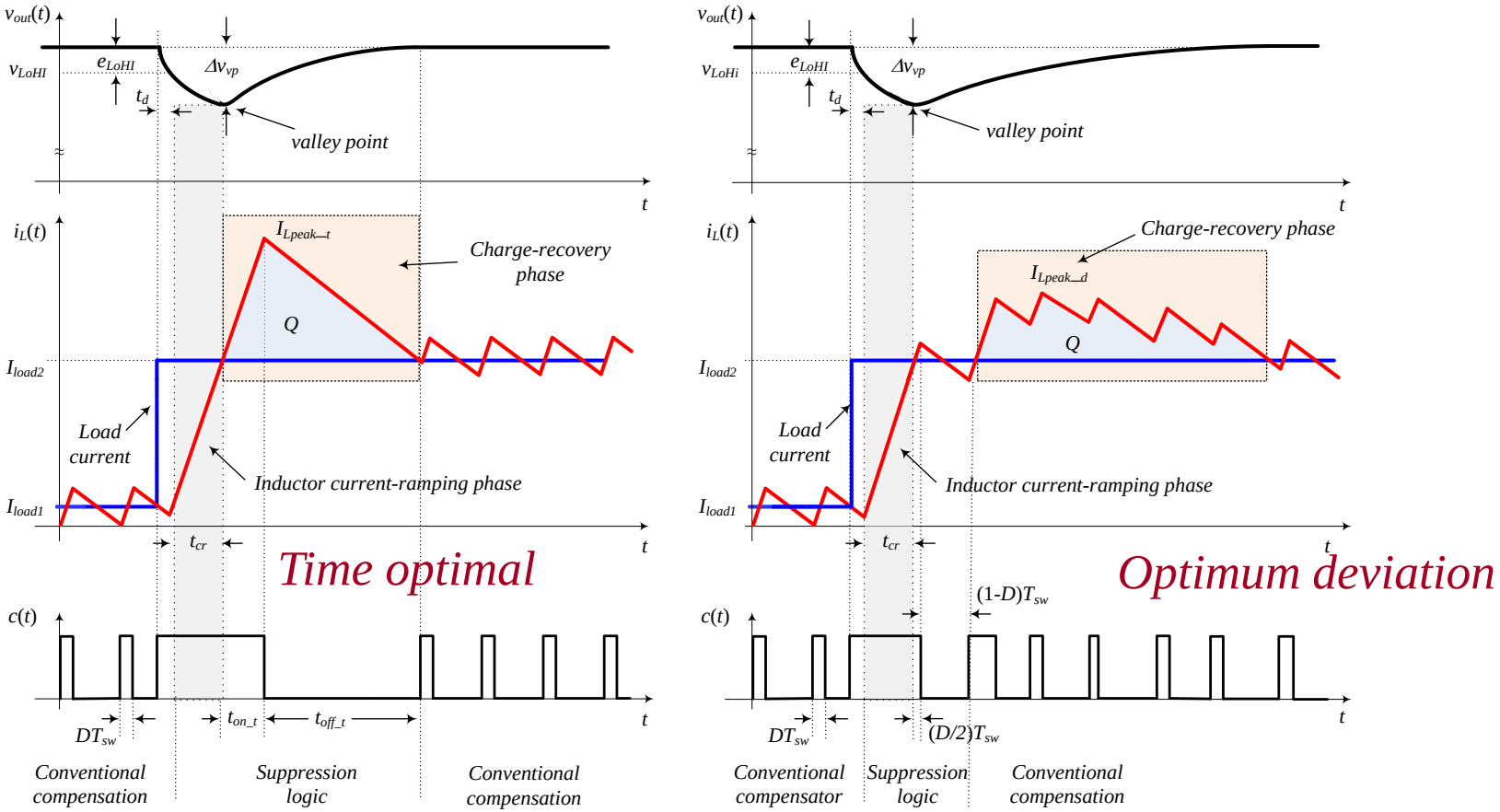
Rather than focusing on speed, focusing on the ultimate goal, minimization of the output voltage deviation, i.e. Δq_{trans} reduction

Minimum (Optimum) Deviation Controller



[1] A. Radić, Z. Lukić, S.M. Ahsanuzzaman, A. Prodić, and R. de Nie, "Minimum Deviation Digital Controller IC for Dc-Dc Switch-Mode Power Supplies," IEEE Trans. on Power Electronics, Sept. 2013,Vol.28.

Minimum (Optimum) Deviation Controller

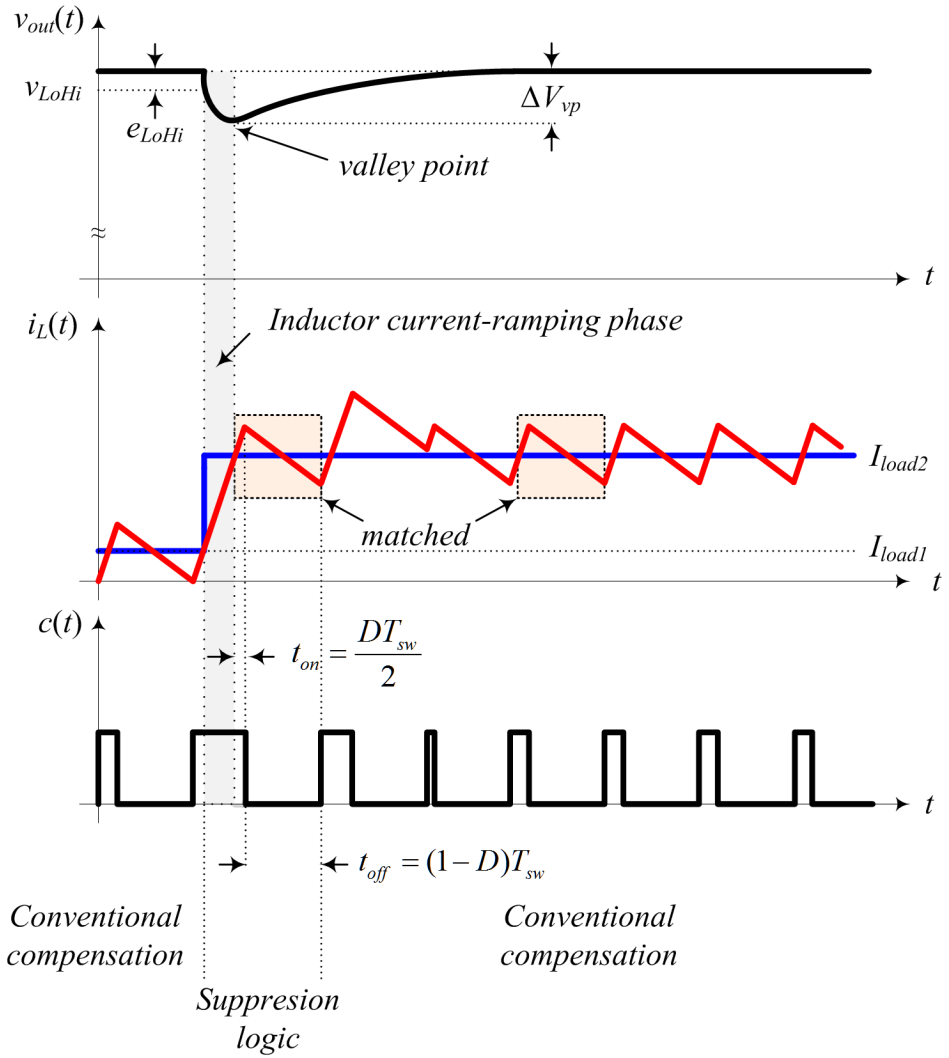


Transient recovery circuit recovers inductor current and ripple, compensator voltage = > No current overshoot, no need to know converter parameters, simple calculations

Minimum (Optimum) Deviation Controller

Light-to-heavy load transient

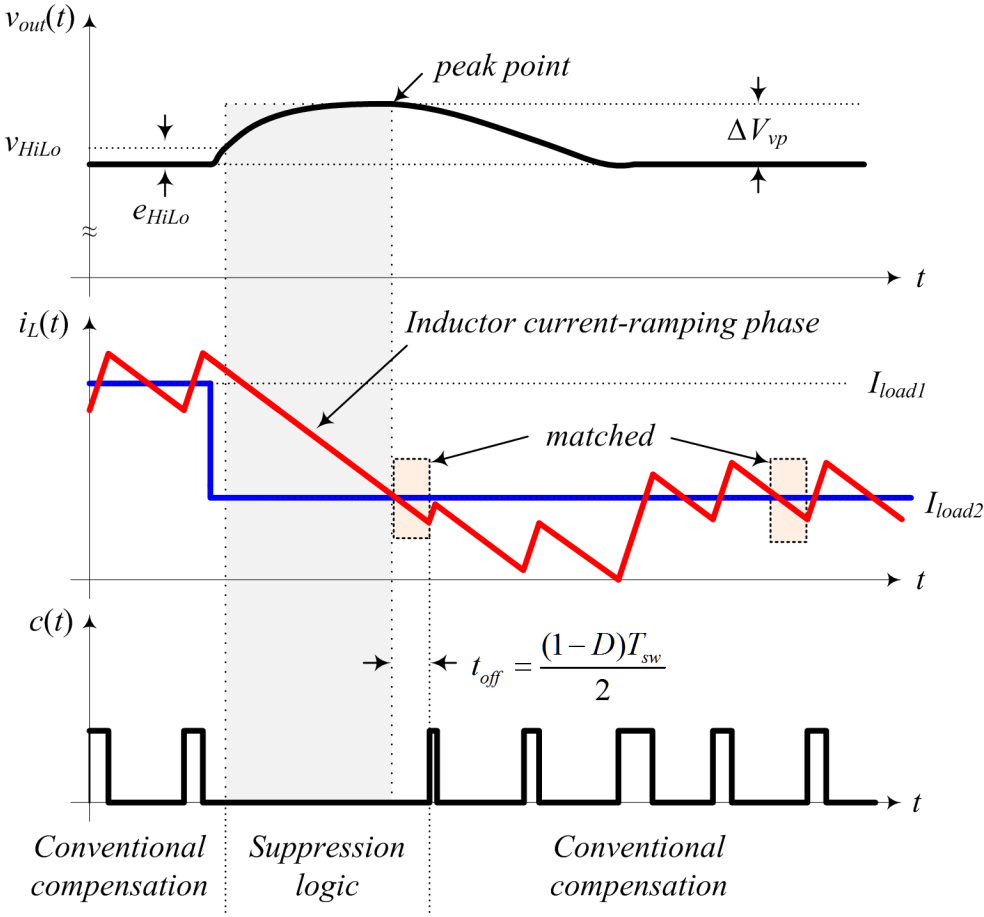
- *The reconstruction of the inductor current is performed only based on the previously known duty ratio value (D) and the detection of valley point ($i_c = i_{load\_new}$).*
- *Simple calculation (almost no calculations needed), allowing simple implementation*



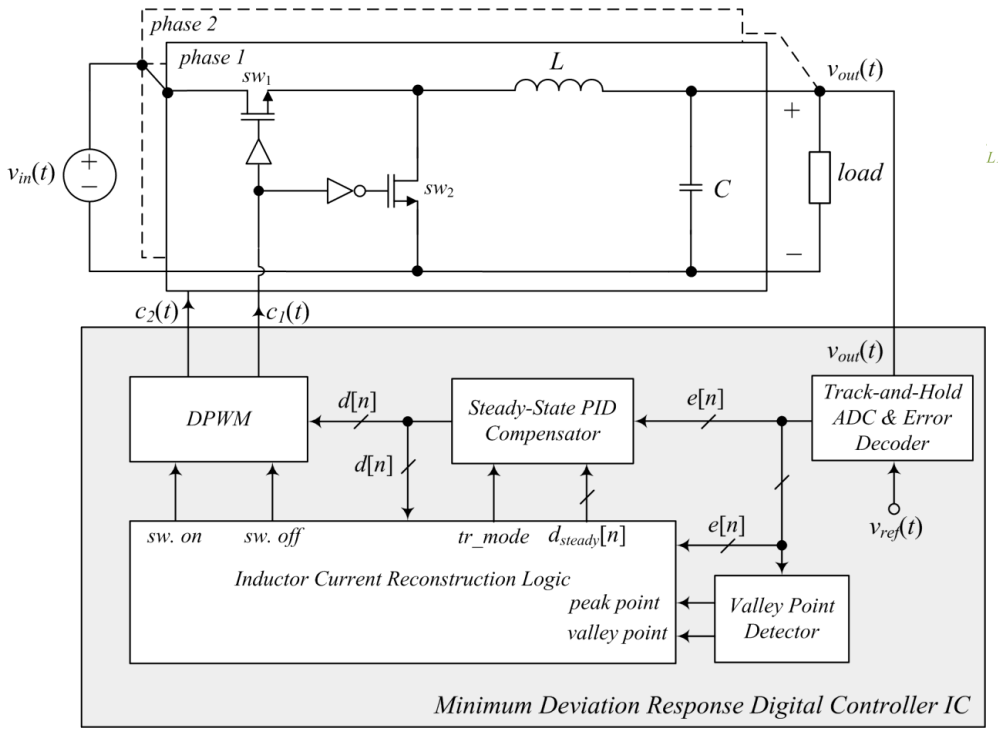
Minimum (Optimum) Deviation Controller

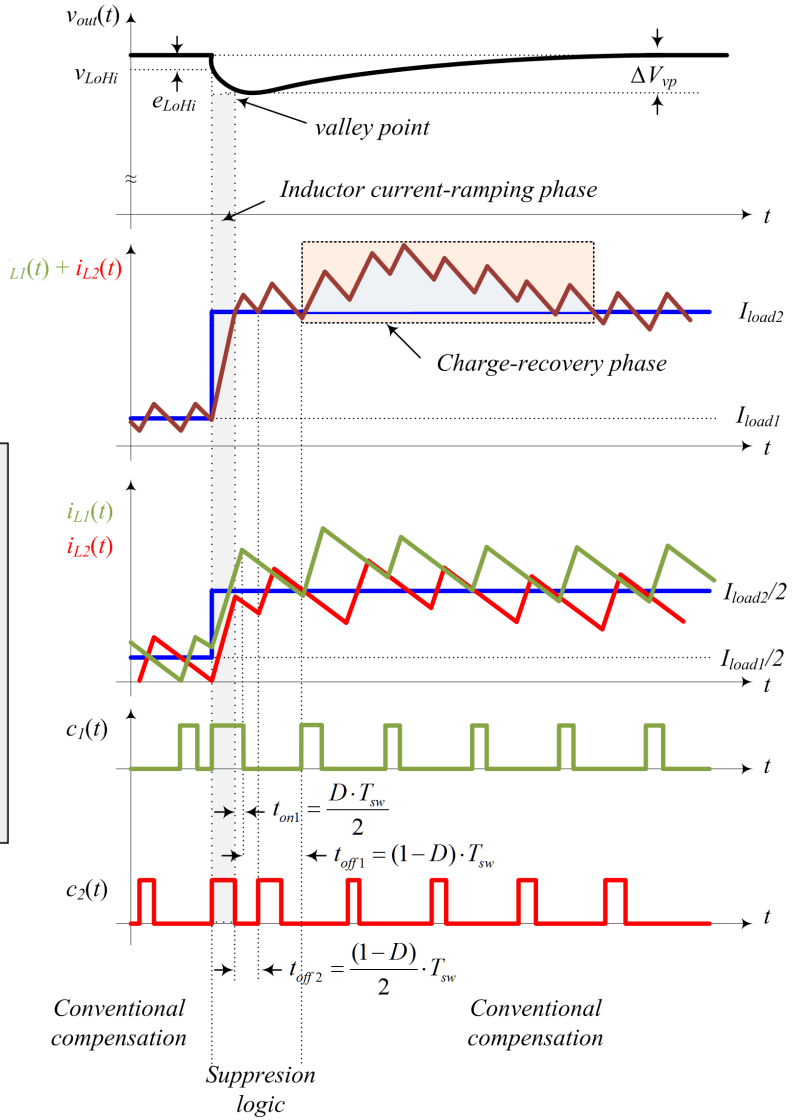
Heavy-to-light load transient

- *The reconstruction of the inductor current is performed only based on the previously known duty ratio value (D') and the detection of valley point ($i_c = i_{load\_new}$).*
- *Simple calculation (almost no calculations needed), allowing simple implementation*

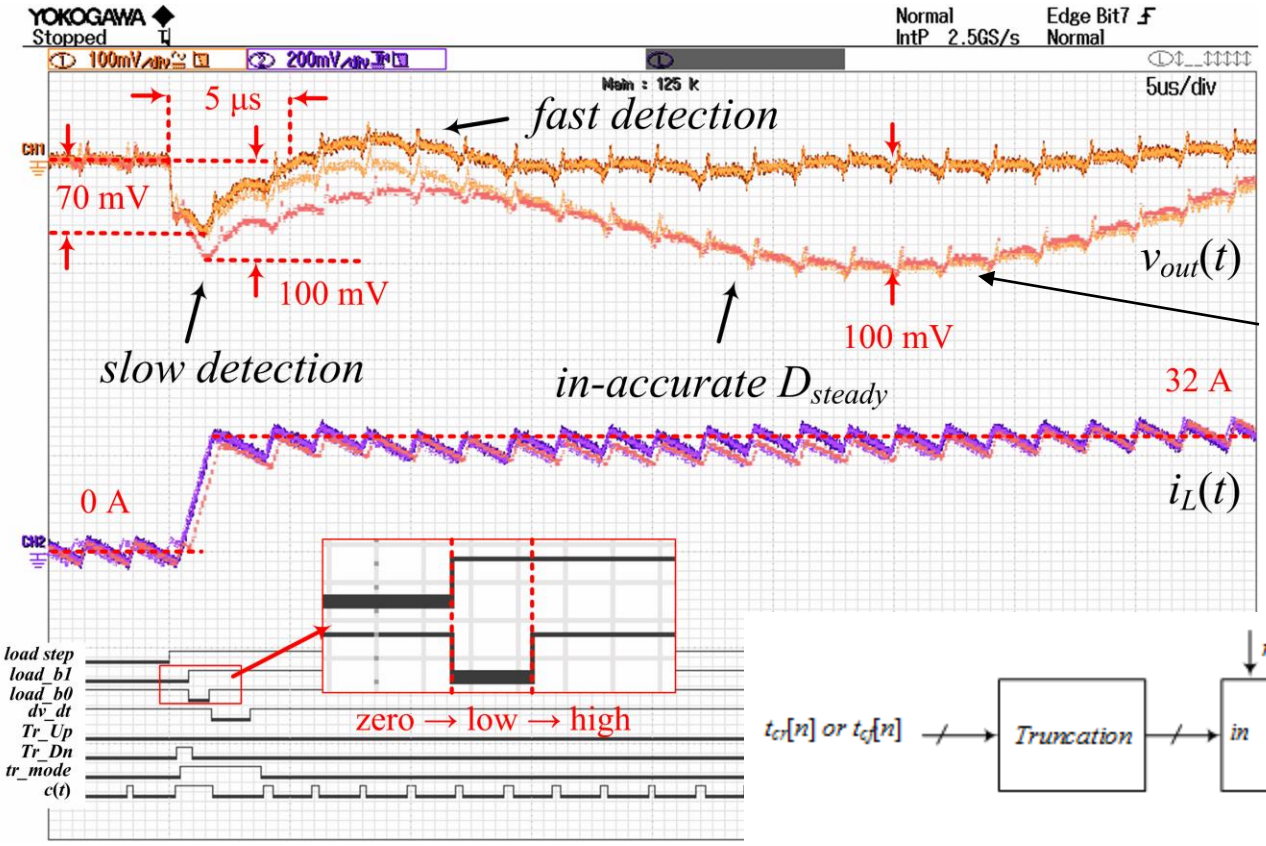


Implementation for a 2-Phase System

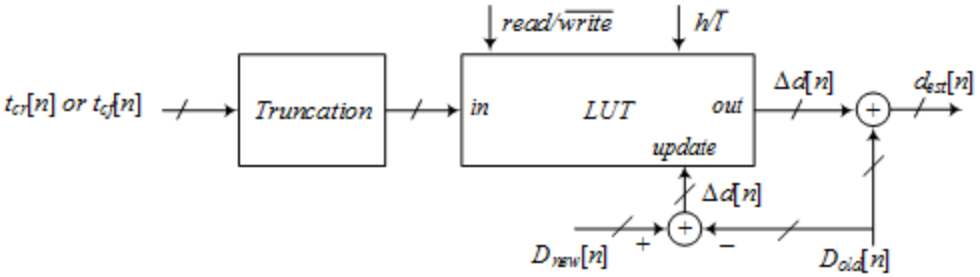




Correction for Duty Ratio Mismatch (Losses)

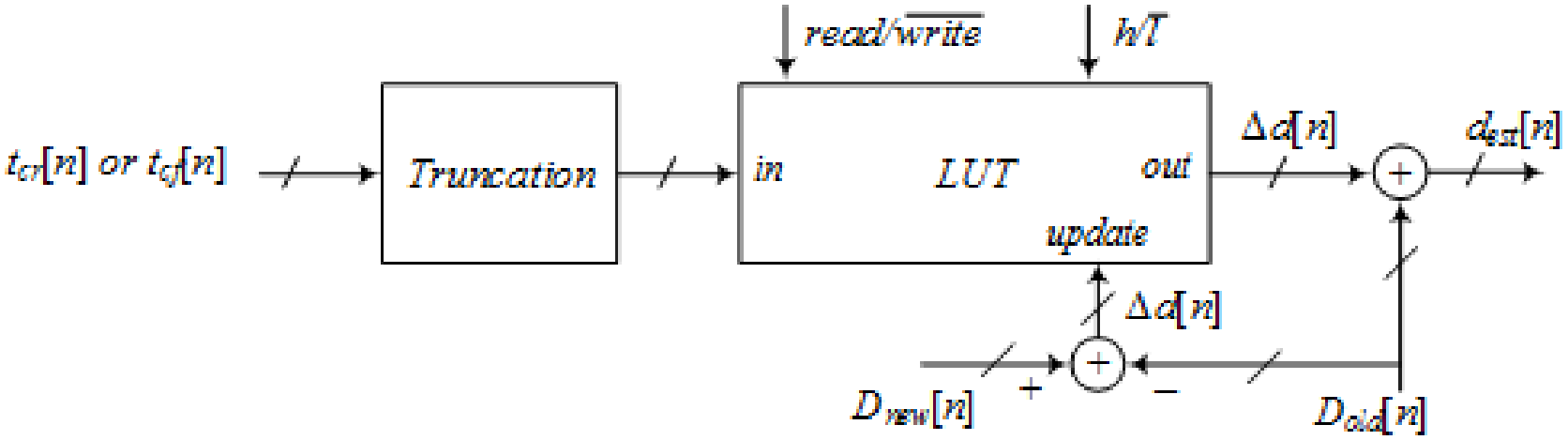


Secondary transient



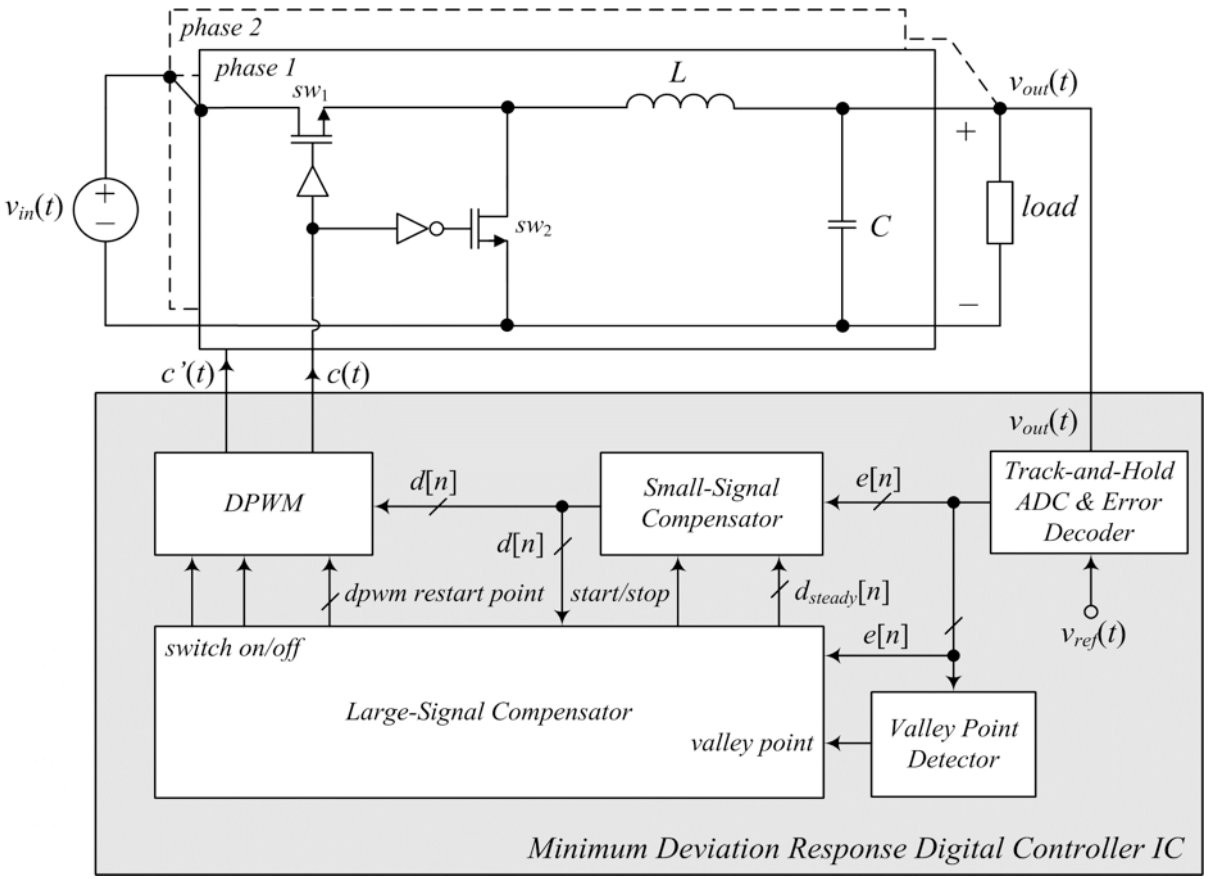
Losses of the converter cause D before and after the transient to have different values, as a result a secondary transient can occur. To compensate for that extra logic is developed.

Correction for Duty Ratio Mismatch (Losses)



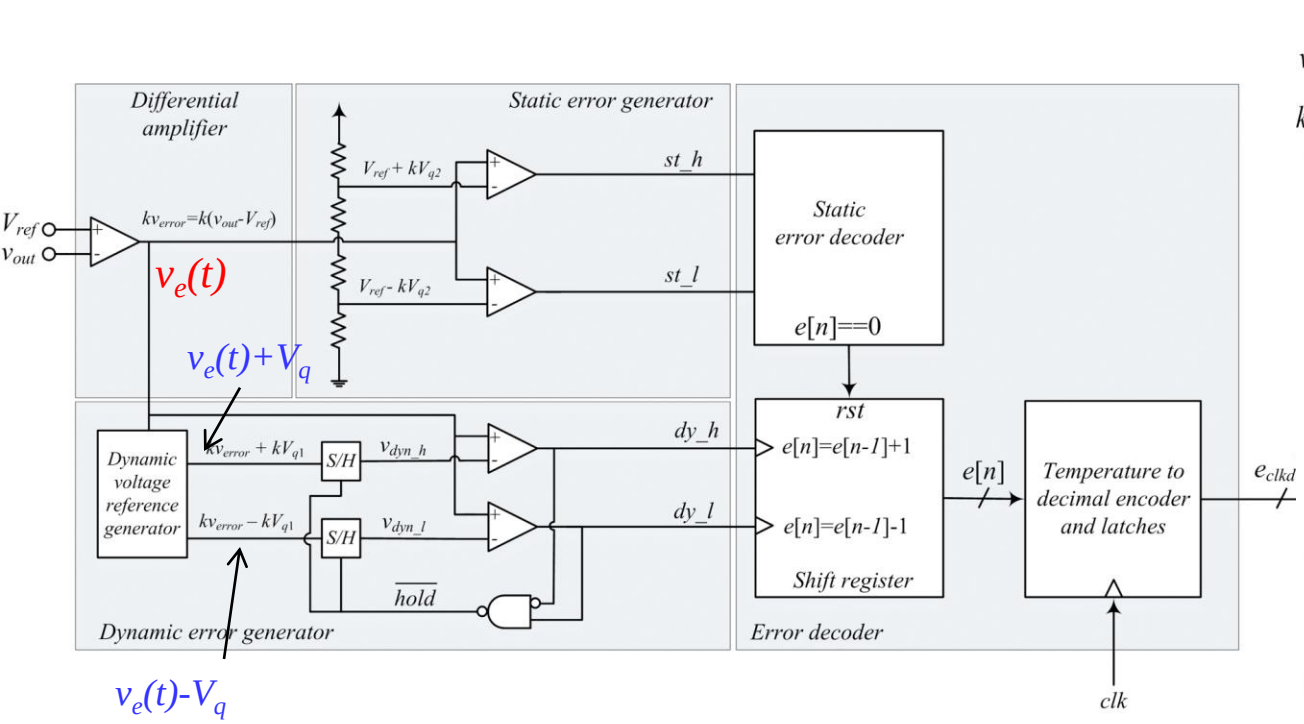
Based on previously noticed voltage deviations it memorizes differences between duty ratio values and uses them later on as a correction factors

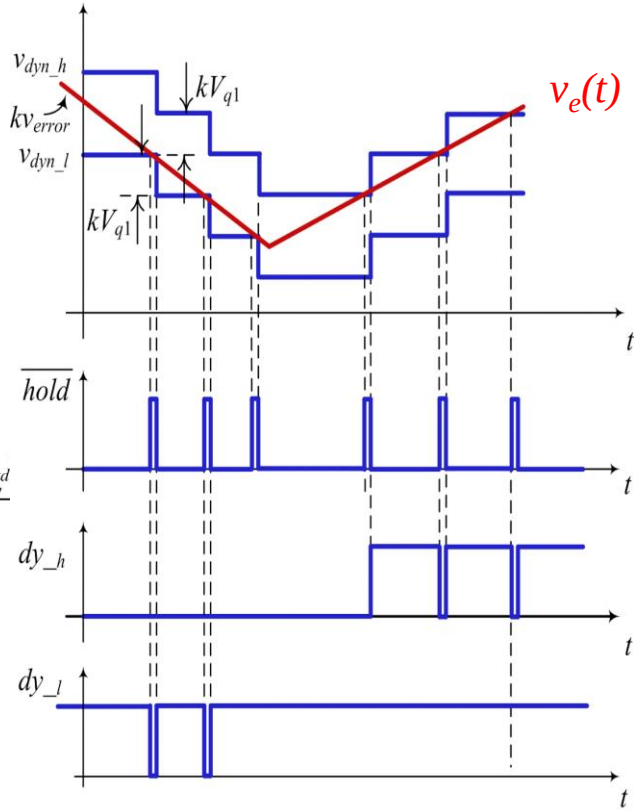
Minimum (Optimum) Deviation Controller IC



Simple logic: Only needs to remember D before transient and, in a realistic case, adjusts duty ratio to compensate for dc load-dependent duty ratio variations.

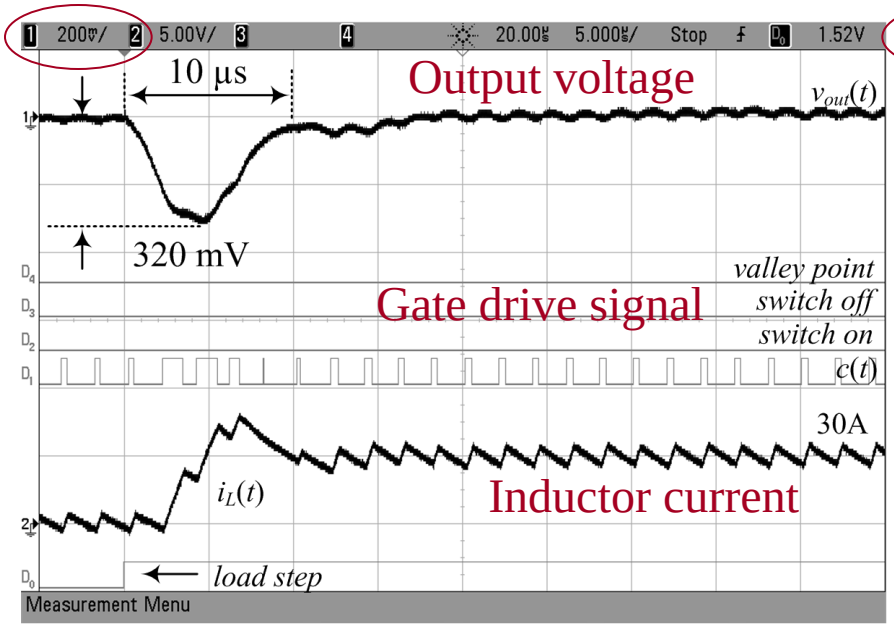
Self-Calibrating SAR Track & Hold ADC

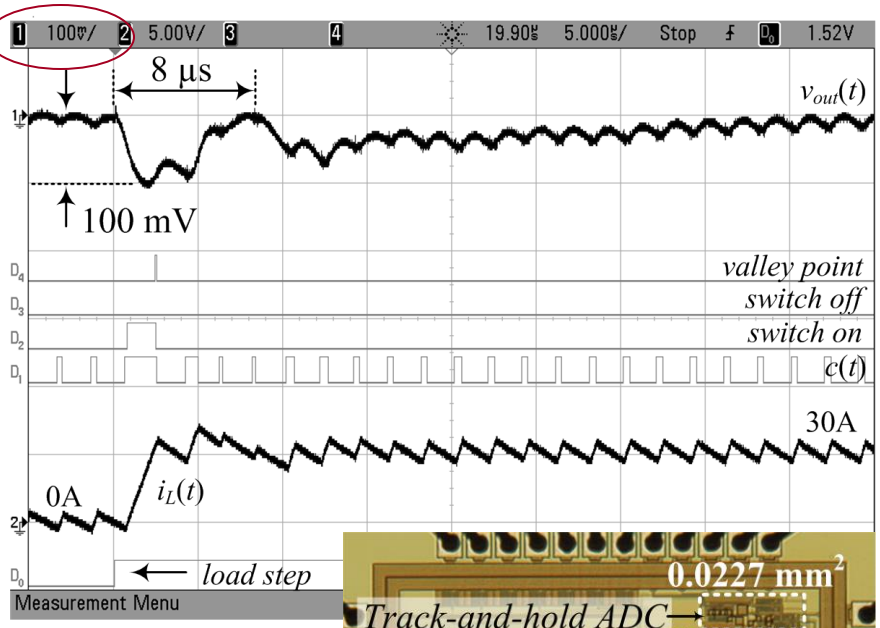




A simple modification of a one-bit successive approximation ADC for transient detection and steady-state voltage regulation.

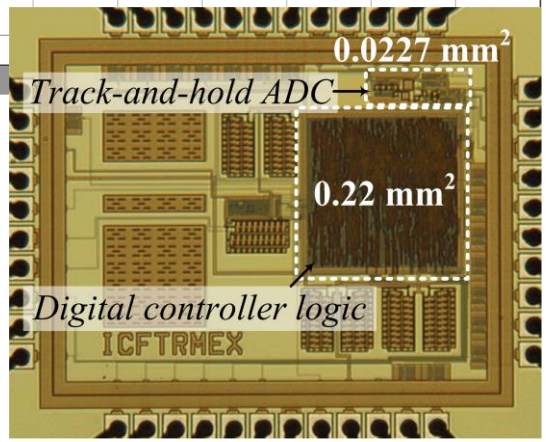
Practical Implementation (500 kHz VRM)





Fast PID (f_{sw}/10)

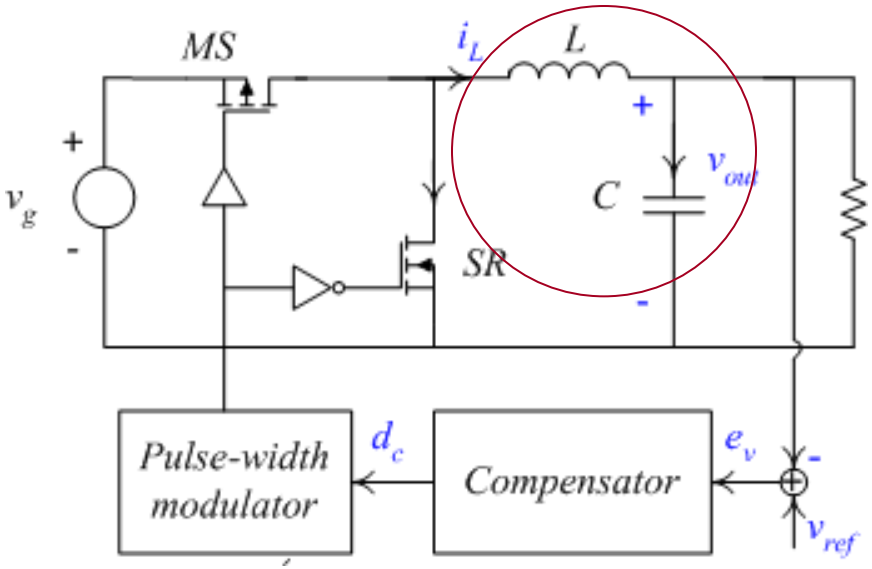
Optimum Deviation



No current overshoot, about 3x smaller output capacitor

Digital Control and Physical Limitations

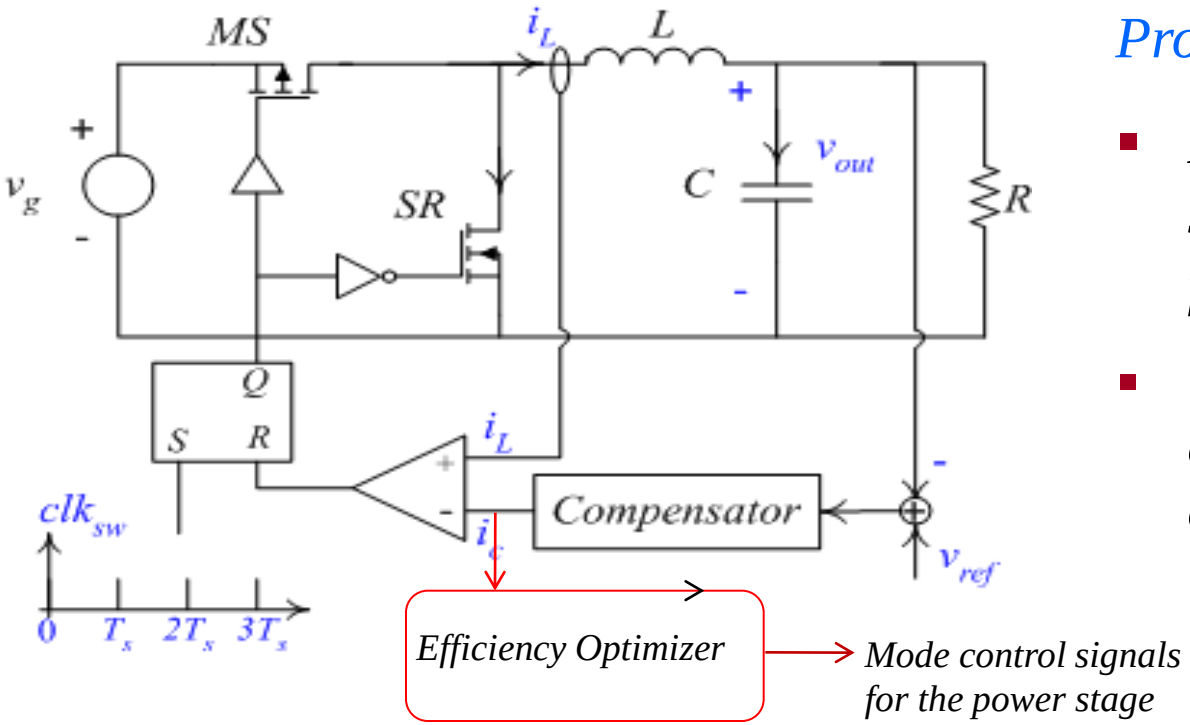
- Operation at high switching frequencies ✔
- Fast dynamic response of the controller ✔ - Pushed to physical limits



Load current

High Frequency (10 MHZ) Mixed-Signal CPM Controller IC with Instantaneous On-Line Efficiency Optimization

Mixed-Signal HF CPM Controller

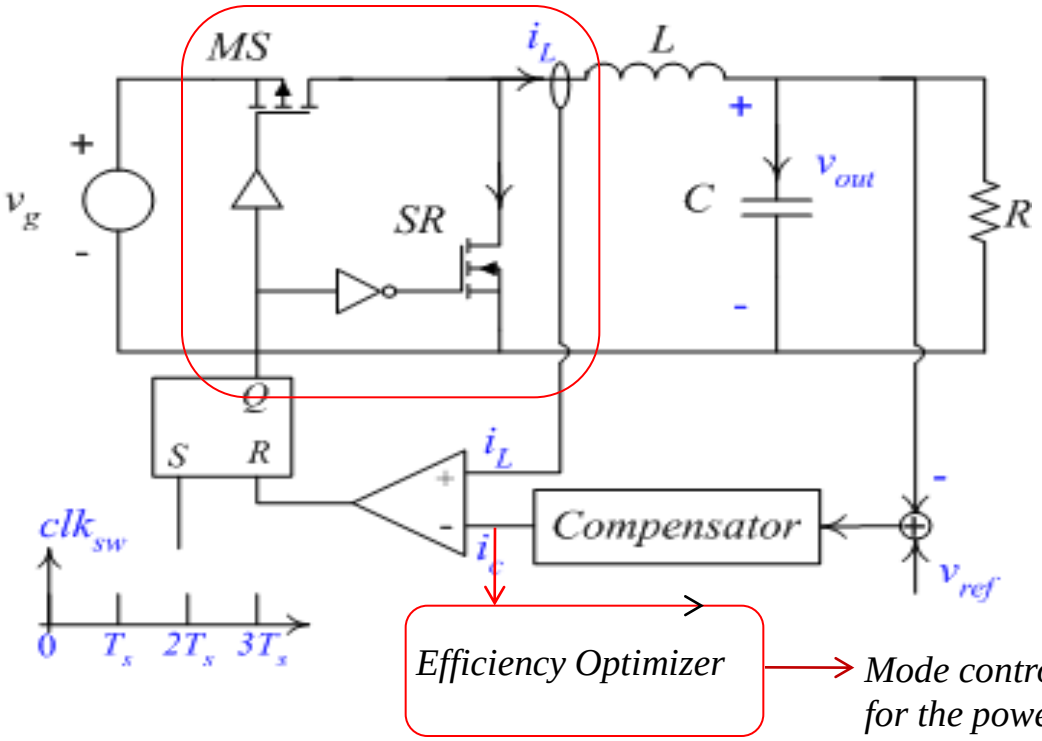


Provides solutions:

- *Power efficient current sensing at high switching frequencies*
- *Instantaneous efficiency optimization in the presence of highly dynamic loads*

[1]A. Parayandeh, B. Mahdavikkhah, S.M. Ahsanuzzaman, A. Radić, and A. Prodić, "A 10 MHz mixed-signal CPM controlled DC-DC converter IC with novel gate swing circuit and instantaneous efficiency optimization," in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), 2011, pp. 1229-1235.

Principle of Operation (Mixed-Signal Loop)



Efficiency optimization performed through:

-Power stage segmentation

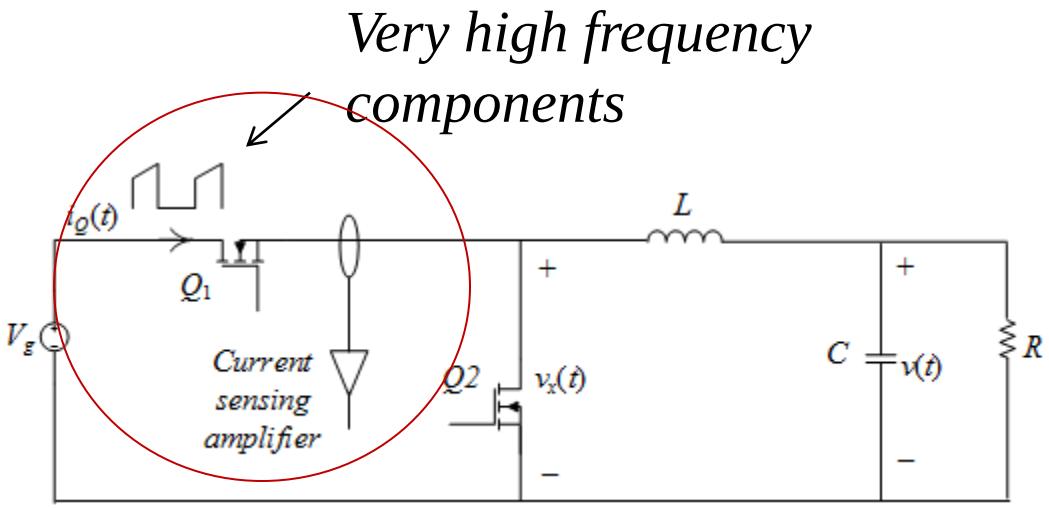
- Gate swing variation

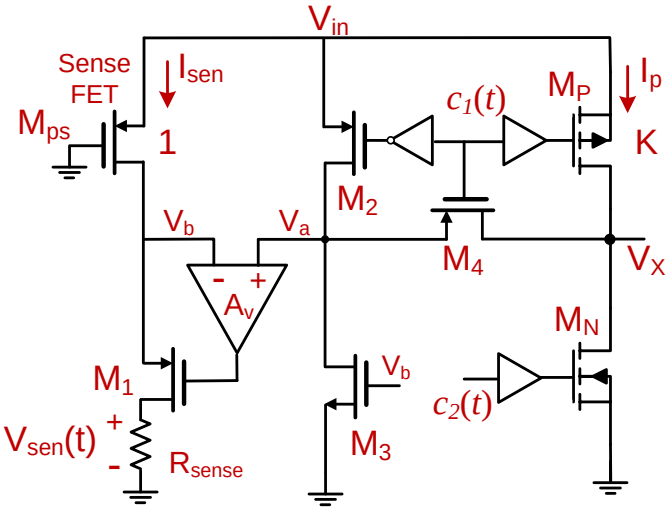
- PFM/PWM mode switching

The current loop compensator contain information about the transistor current over the next switching cycle. Based on that prediction parameters of the power stage are adjusted.

[1]A. Parayandeh, B. Mahdavikkhah, S.M. Ahsanuzzaman, A. Radić, and A. Prodić, "A 10 MHz mixed-signal CPM controlled DC-DC converter IC with novel gate swing circuit and instantaneous efficiency optimization," in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), 2011, pp. 1229-1235.

Current Sensing Amplifier Problem

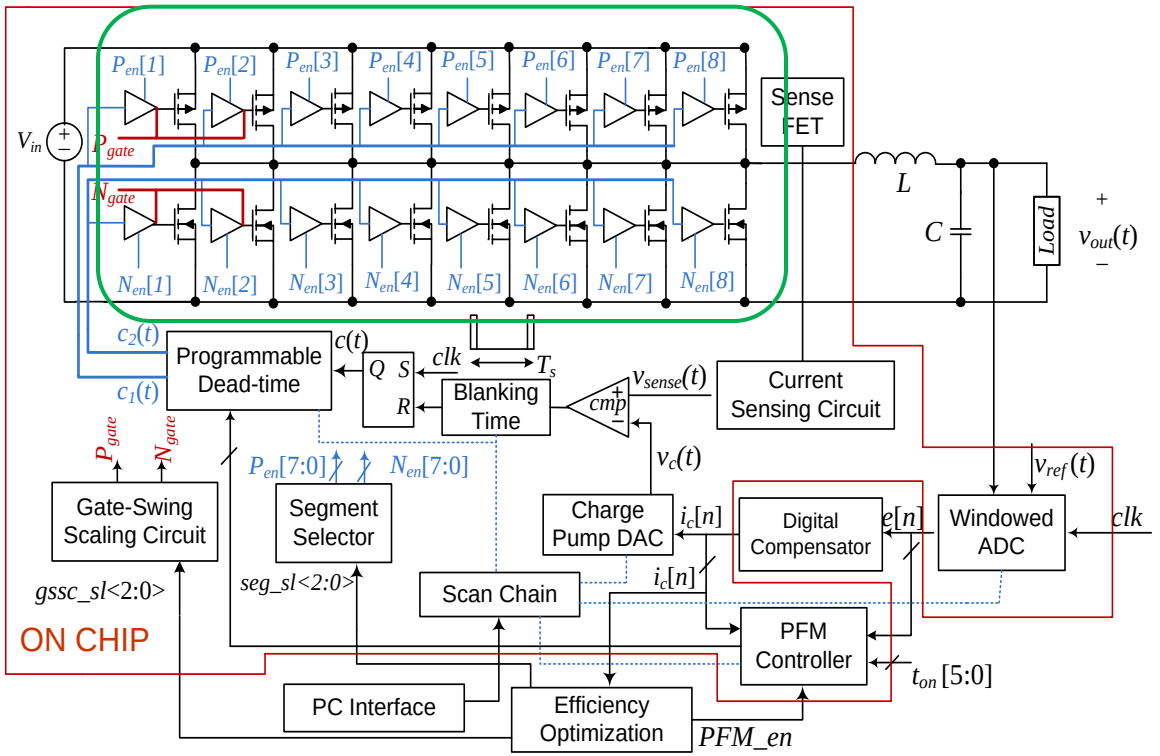




The transistor current is pulsating and has very high frequency components that need to be sensed, also the range of current varies a lot, need for a high GBW amplifier (hard to make and consumes a lot of power)

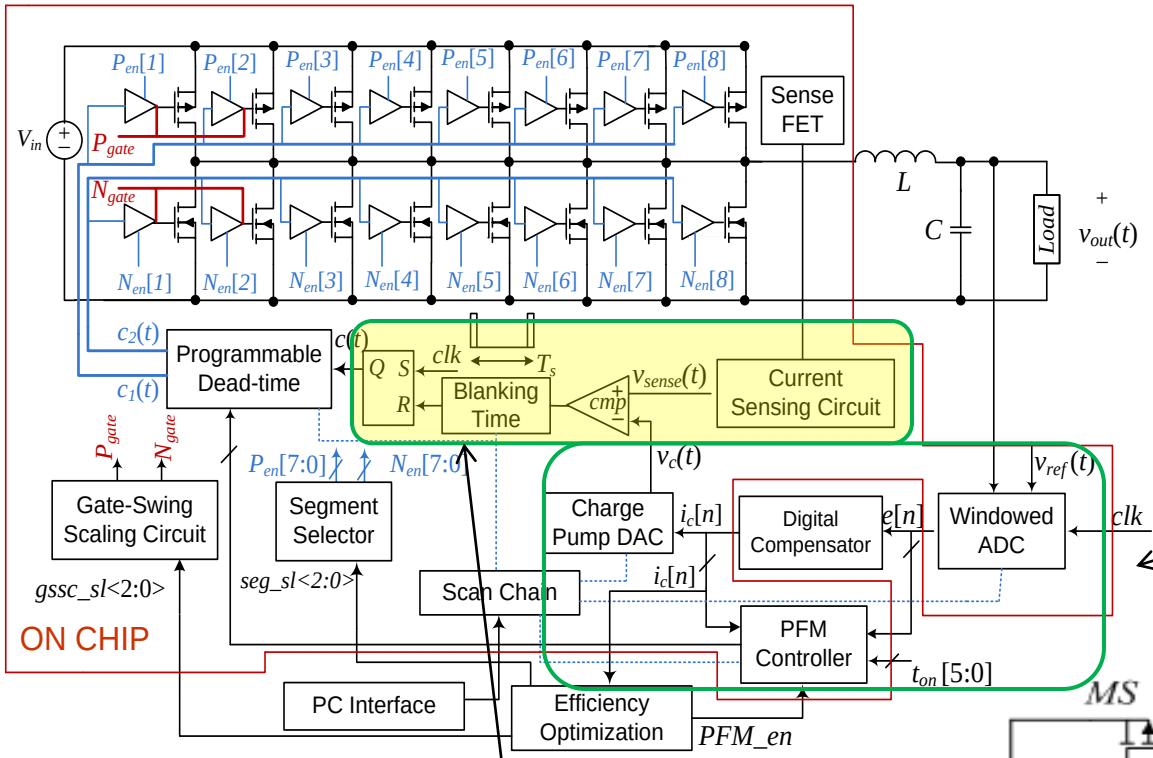
[1]A. Parayandeh, B. Mahdavikkhah, S.M. Ahsanuzzaman, A. Radić, and A. Prodić, "A 10 MHz mixed-signal CPM controlled DC-DC converter IC with novel gate swing circuit and instantaneous efficiency optimization," in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), 2011, pp. 1229-1235.

10 MHz Power Module IC Block Diagram



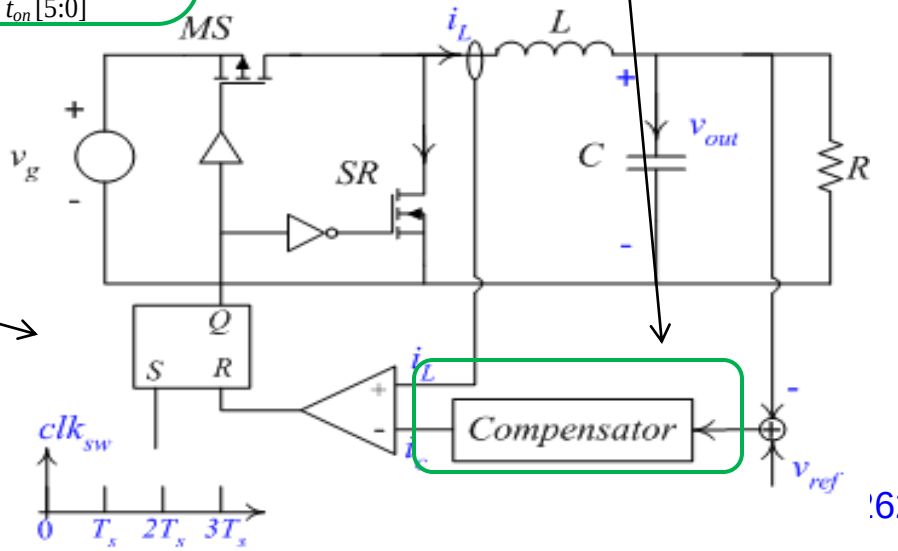
- *Segmented power stage, i.e. transistors made of 8 identical smaller ones. Seven transistors have the same gate voltage and one of them has variable gate voltage.*
- *In this way very accurate tradeoff between switching losses and conduction losses can be made.*

10 MHz Power Module IC Block Diagram

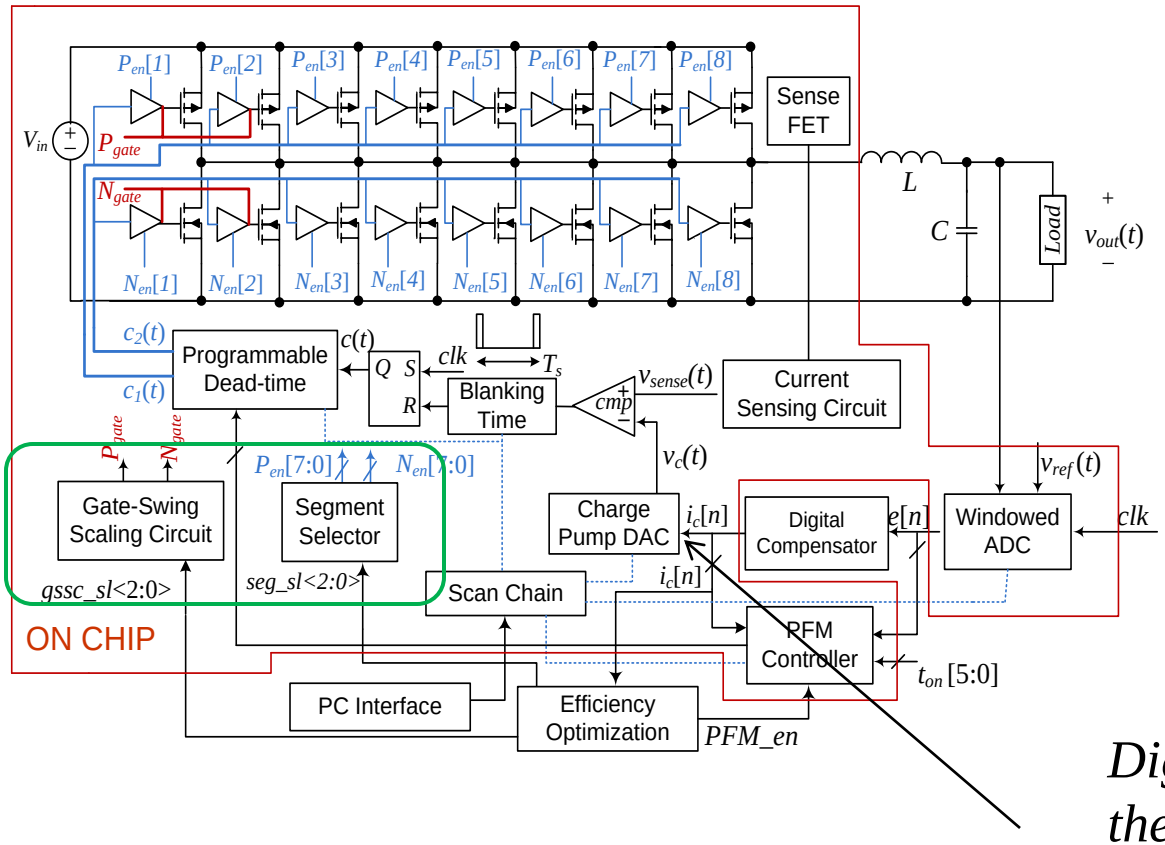


Digital voltage loop implements optimum deviation controller

Conventional "analog" current loop



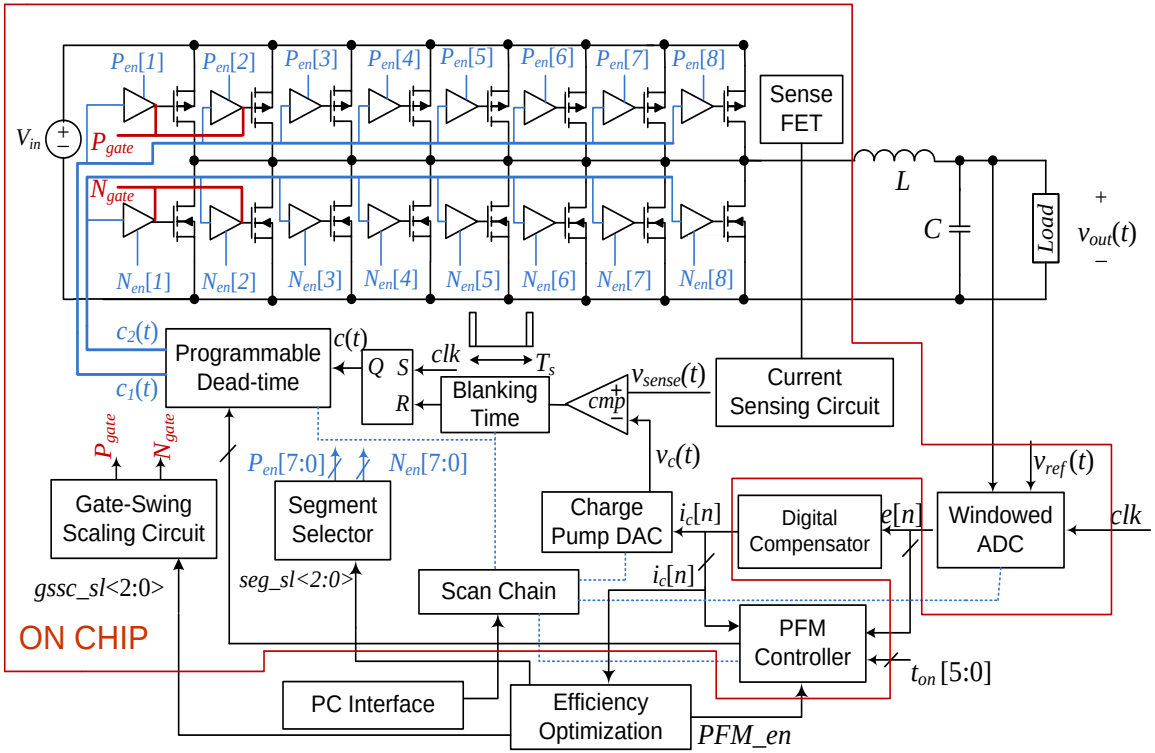
10 MHz Power Module IC Block Diagram



Digital logic that based on the info from the voltage loop, i.e. known current value in the next switching cycle changes the mode of operation

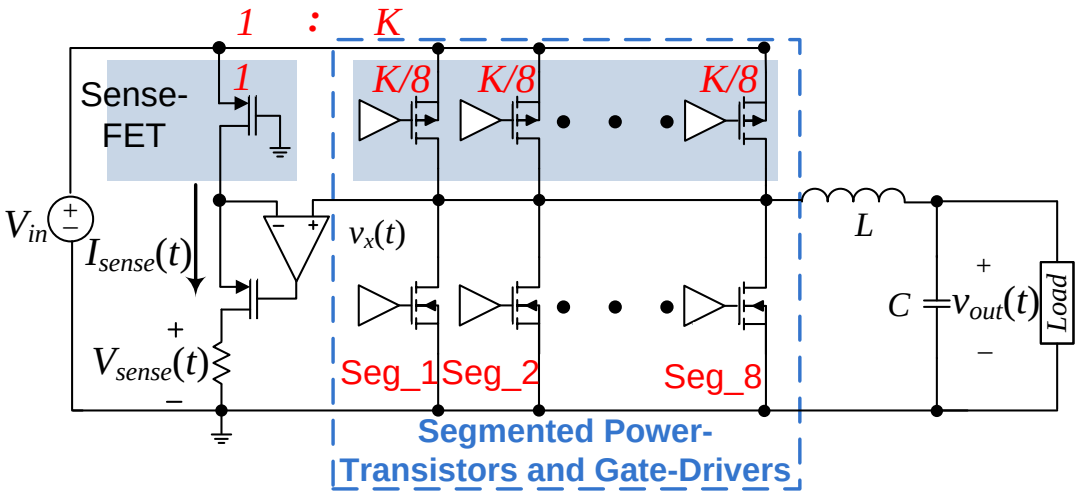
Digital control variable from the voltage loop (transistor current of the next switching cycle)

Principle of Operation



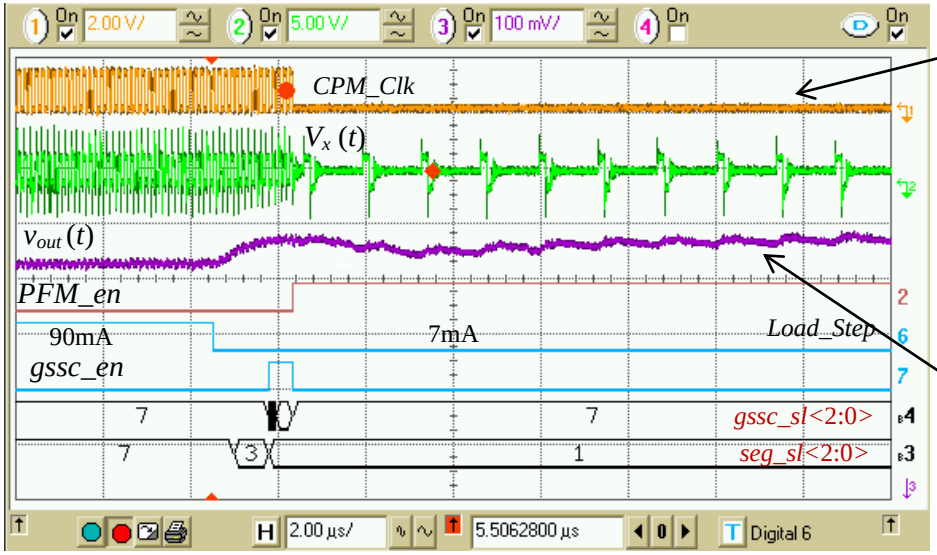
At heavy and medium loads the number of power stage segments is dynamically adjusted. At lighter loads only one segment operates and the gate drive voltage is changed. At even lighter loads the controller enters PFM mode of operation.

Low-Power High-Frequency SensFET



- *GBW requirements for the amplifier reduced since the amplitude is always relatively large (but not the losses)*
- *Provides operation at 10 MHz switching frequency*

Experimental Results

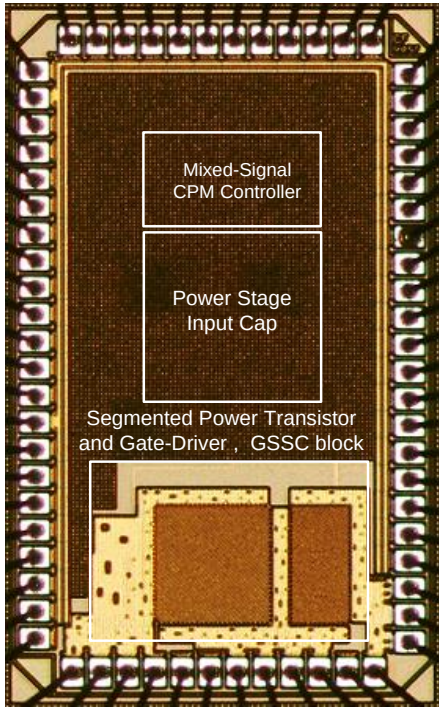


Inductor current

Output voltage

Heavy to light load transient and change from PWM mode of operation to PFM, which is more efficient at light loads.

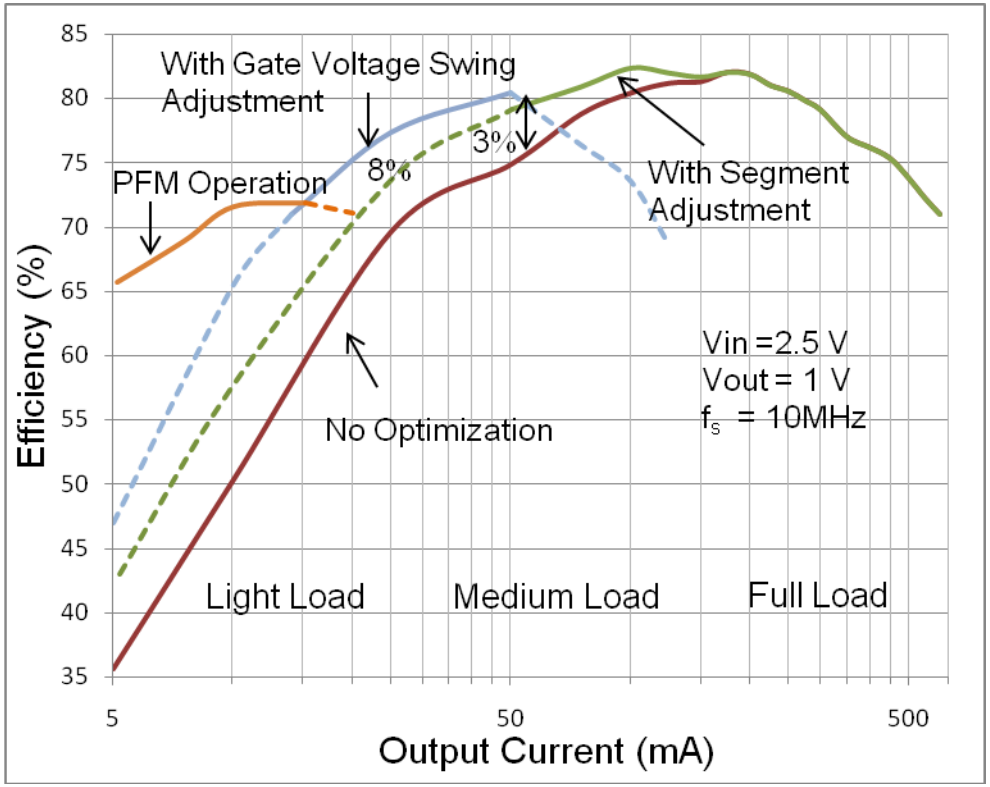
10 MHz CPM IC Power Module (Implementation)



2 W/ 10 MHz On-chip CPM controlled power module

Specifications	Value	Units
CMOS Process	0.13	µm
Area	2.5	mm2
Input Voltage	2.5	V
Output Voltage	0.8-1.3	V
Rated Load	500	mA
Filter L,C	400, 0.9	nH,µF
Switching Frequency ,	10	MHz
Ron Pmos , Nmos	0.26 , 0.234	Ω
Supply Analog , Digital	1.2, 2.5	V
Peak Efficiency	83	%
CPM Controller Current	500	µA
PFM Controller Current	10	µA
Digital Core	200	µA

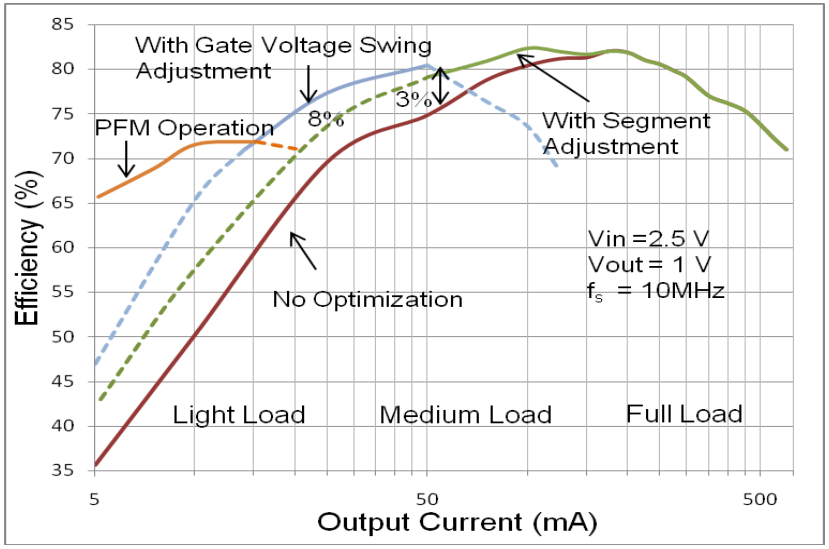
Experimental Results



Comparison with a conventional single mode power stage. Improvement of efficiency curve throughout the full range of operation.

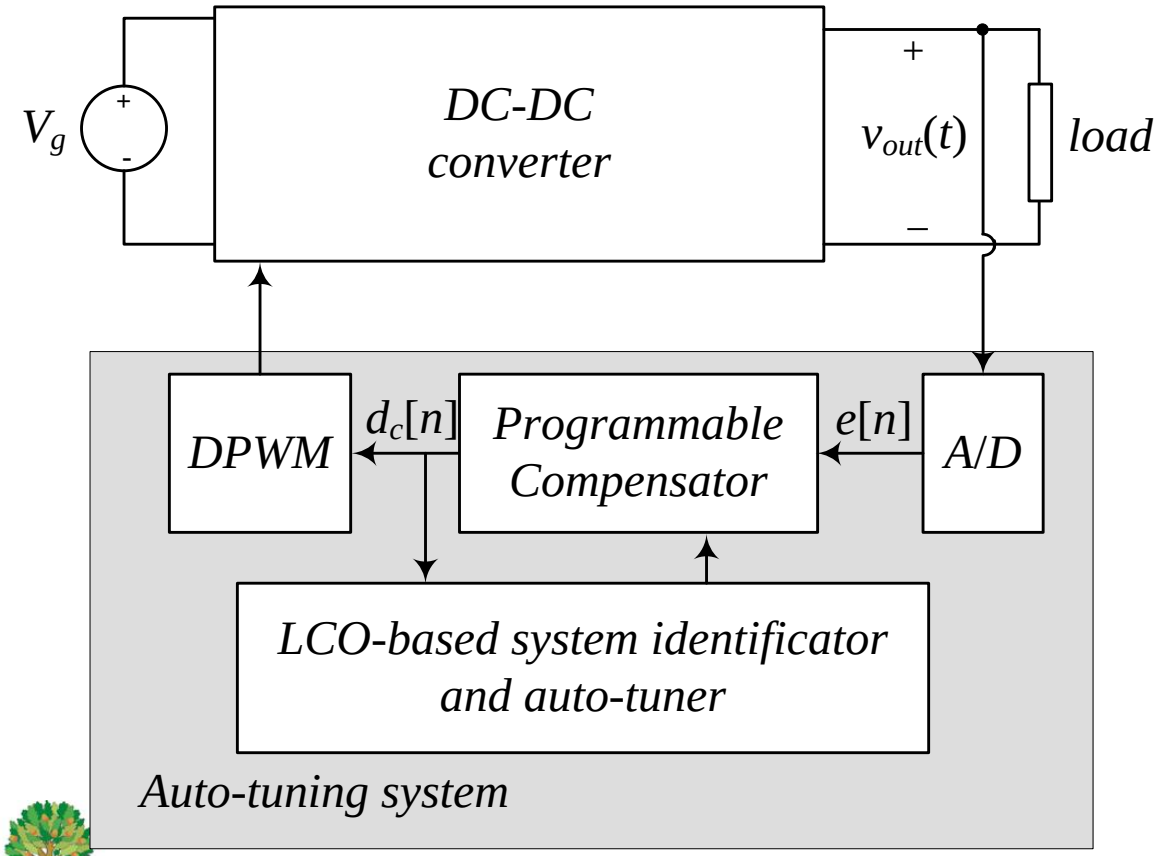
Digital Control and Physical Limitations

- Operation at high switching frequencies ✔
- Fast dynamic response of the controller ✔ - Pushed to physical limits
- Flat and high efficiency curve (efficiency close to the limit) ✔



Limit-Cycling Based Auto-Tuning Controller for Digitally Controlled LP HF SMPS (Plug & Play Controller)

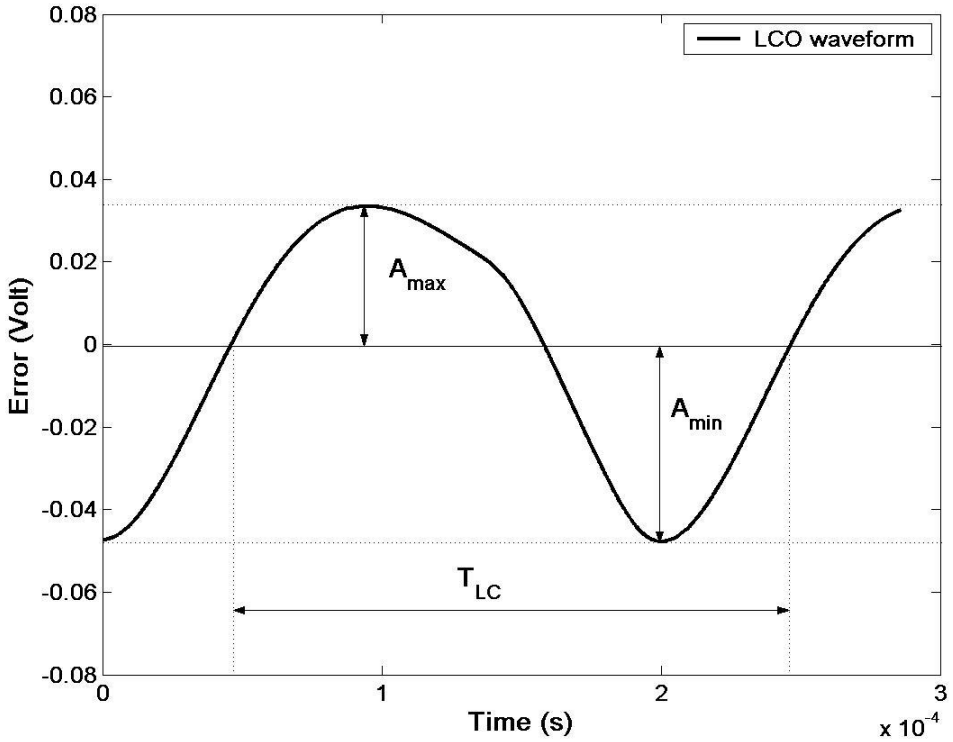
Objective



- *To design a controller that will identify power stage parameters and, accordingly self-tune compensator parameters, such that stability and fast dynamics are maintained in all operating conditions.*

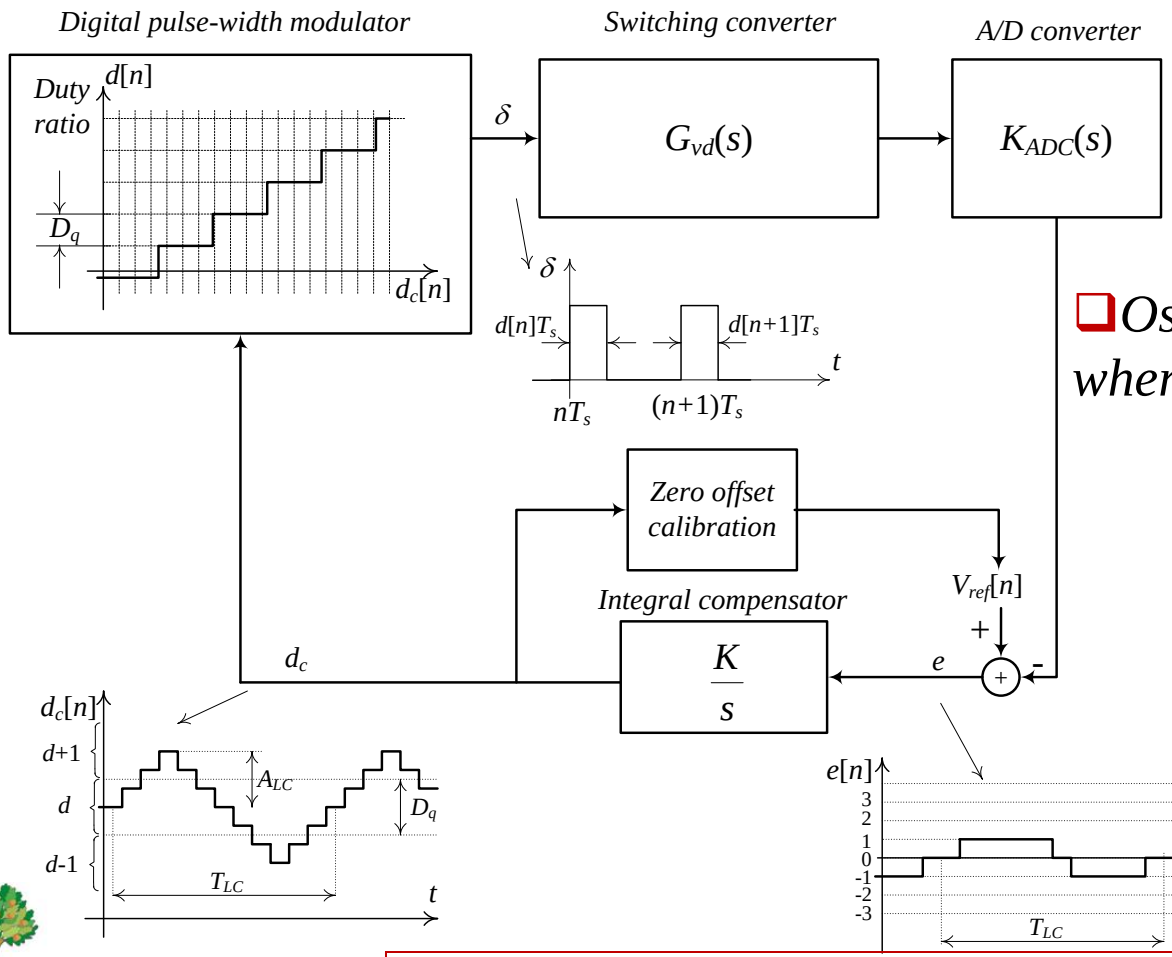
- *Save the cost of the development make an universal solution*

Principle of Operation



- *During a short-lasting identification period limit cycling oscillations are intentionally introduced and from their frequency and amplitude the parameters of the power stage are estimated.*

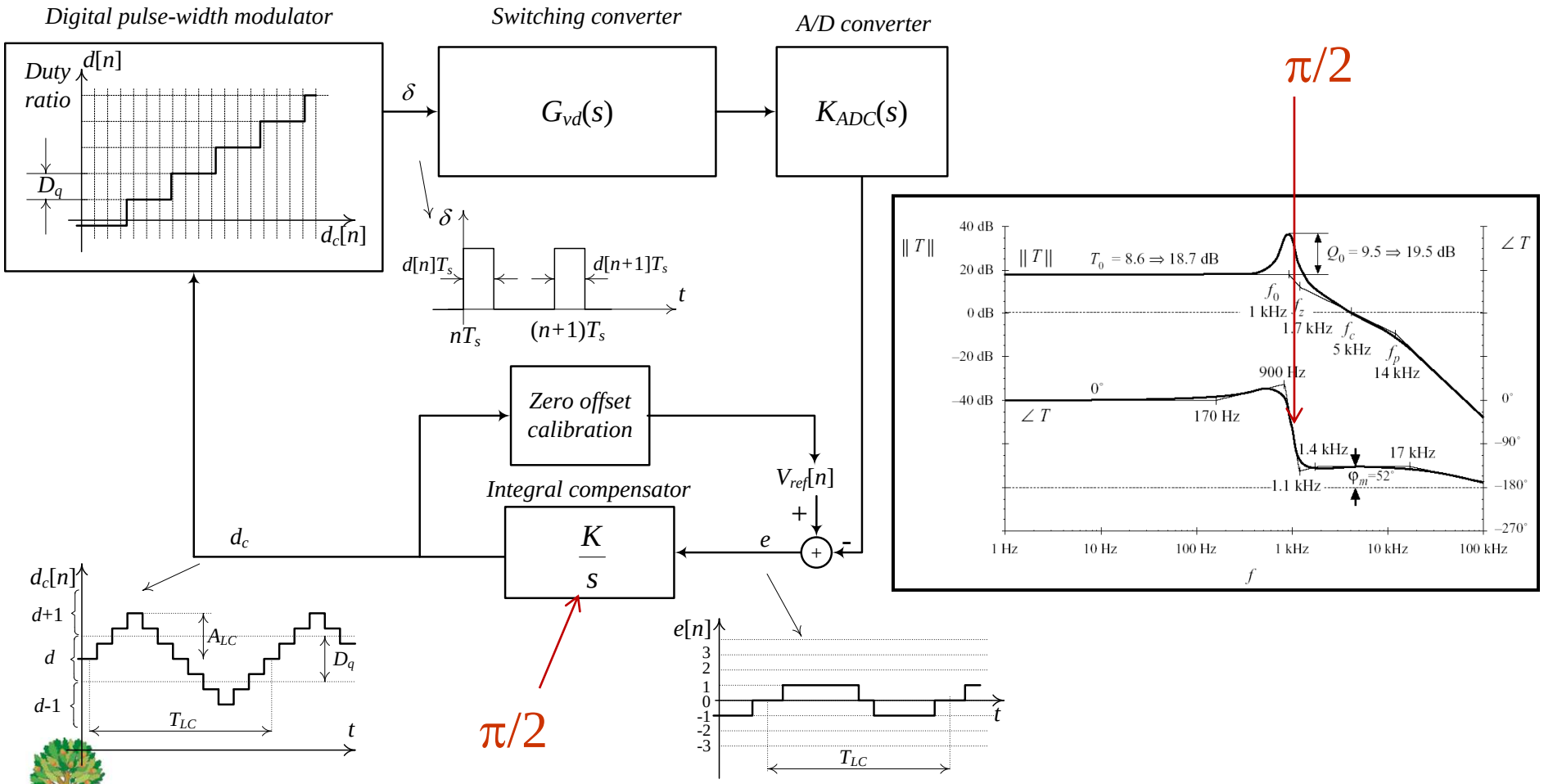
Implementation – block diagram



- *Oscillations occur at the point where the loop gain is -1.*

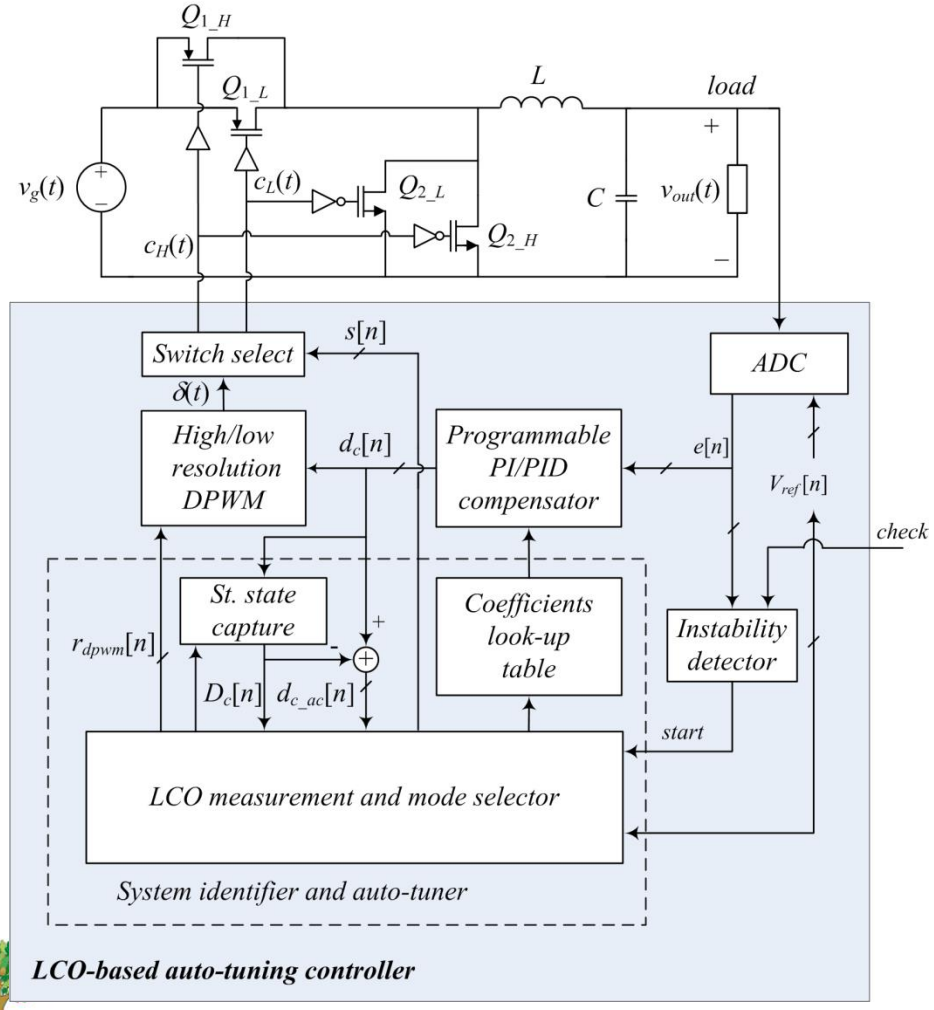
$$-1 = 1\angle 180° = N_{DPWM}(A_{LC}, \varepsilon) G_{vd}(j\omega_{LC}) K_{ADC}(j\omega_{LC}) \frac{K}{j\omega_{LC}}$$

Implementation – block diagram



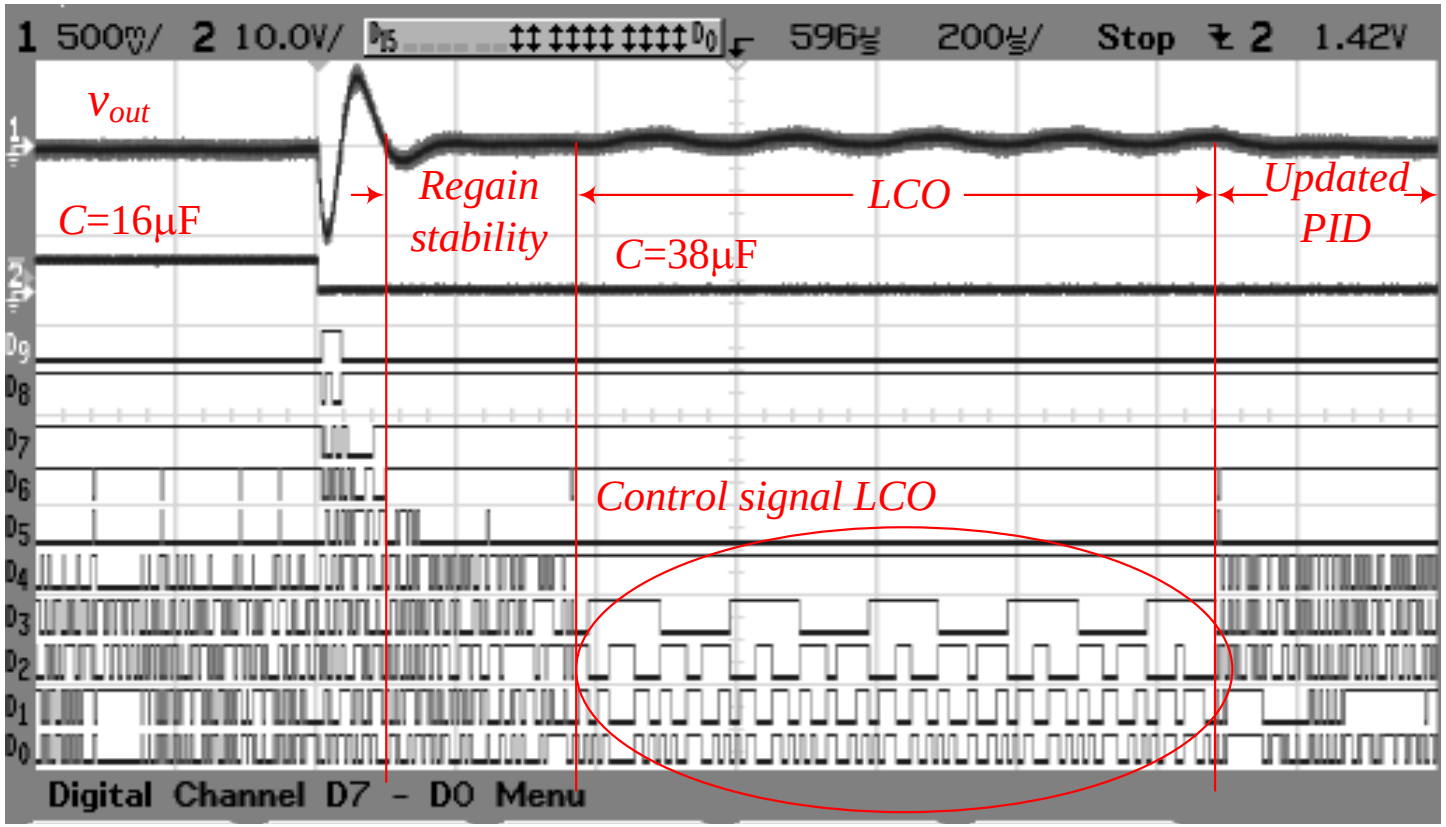
Oscillations occur at the corner frequency of the power stage, i.e. where the phase shift is π

Implementation – Practical Realization

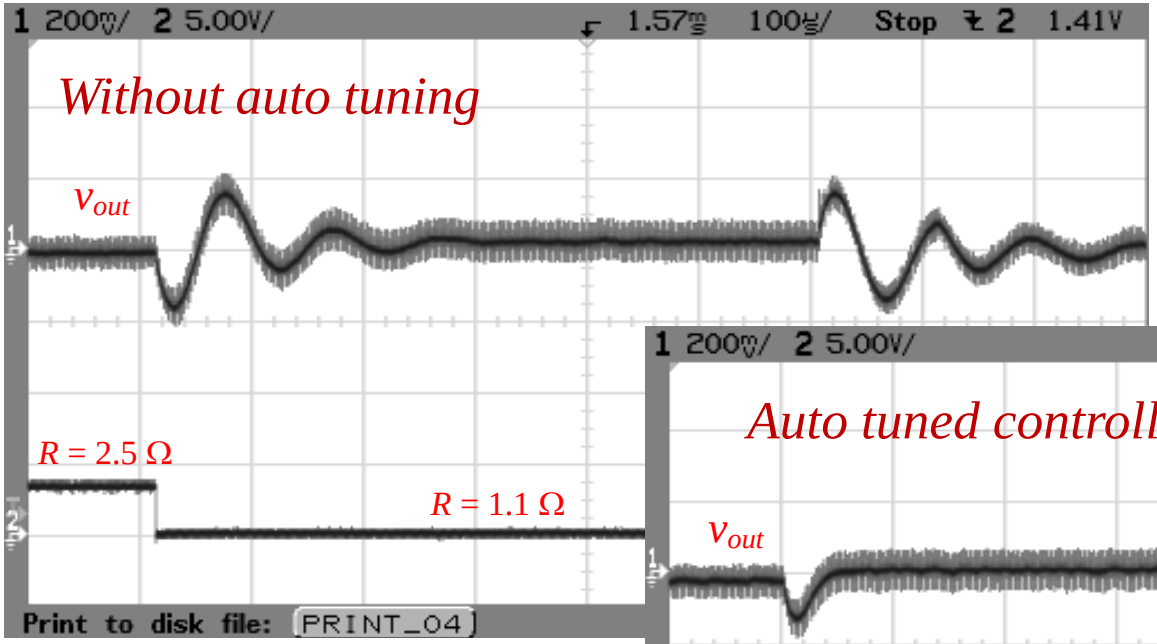


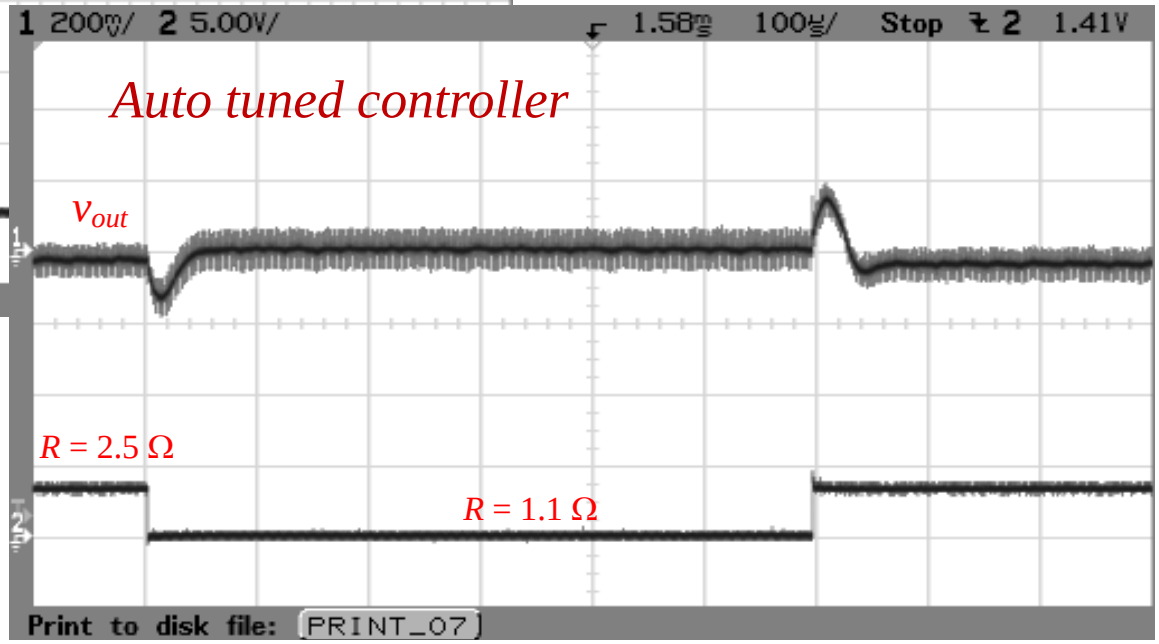
- *Based on the frequency of the oscillations LC product, i.e. corner frequency of the power stage is calculated.*
- *From the amplitude of the oscillation, a rough estimation of the load is performed.*

Experimental Results

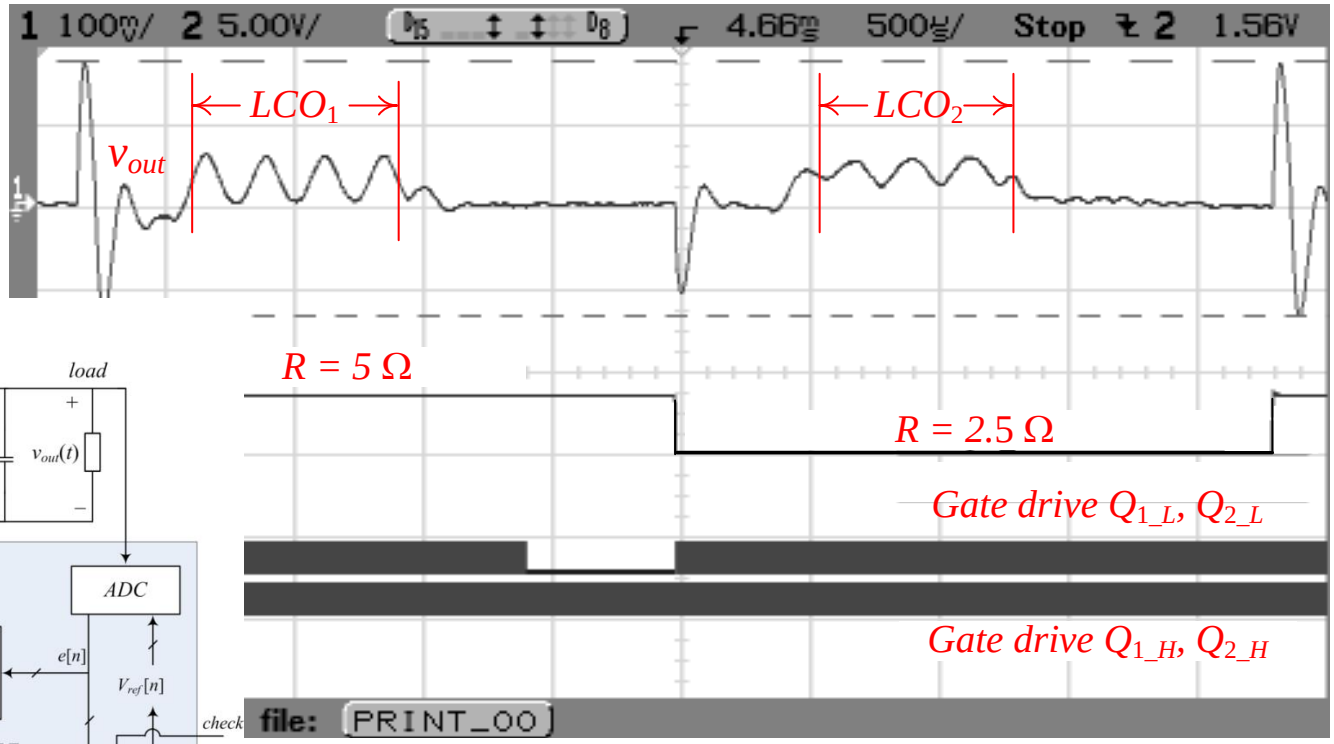


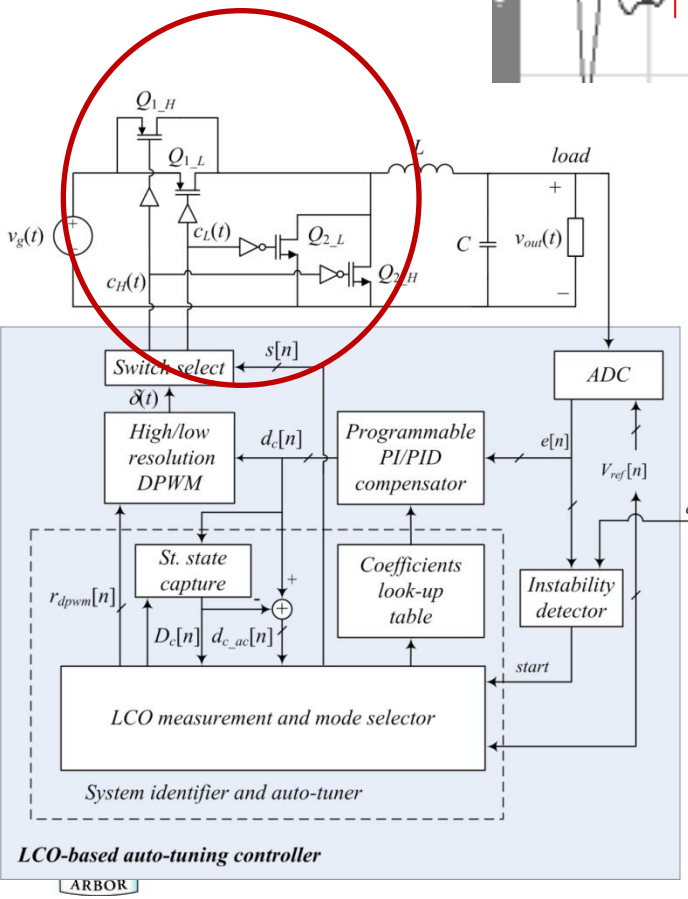
Experimental Results





Efficiency Optimization





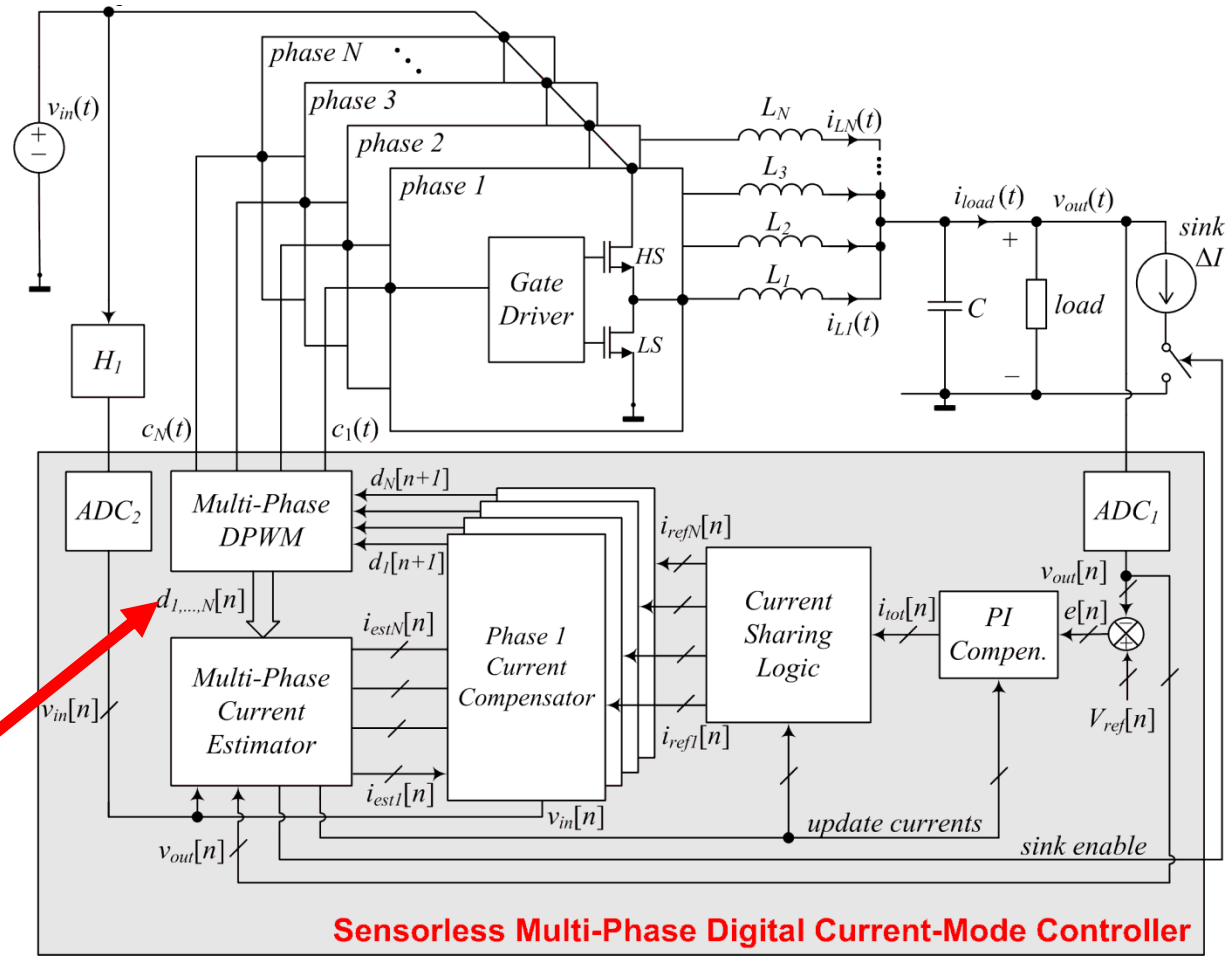
Self-Tuning Averaged Current Programed Mode Controller with Current and Temperature Estimator

Basic Idea

To obtain information about the current (and other converter parameters) without using current sensors.

Benefits: no wires, reliability, less expensive…

Digital Current Loops



Current-Sensing Methods

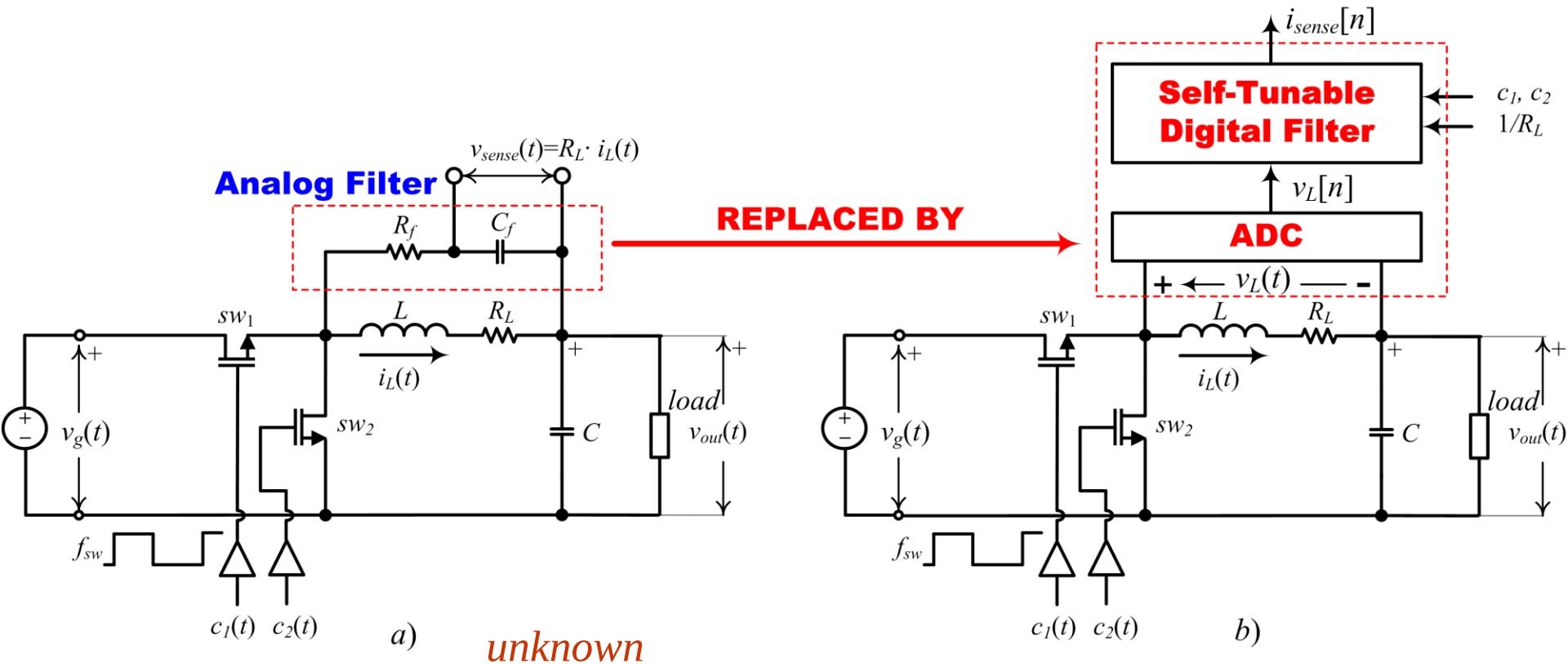
❑ Voltage drop based methods

- Utilize a sense resistor or the parasitic on-resistance of the power MOSFET in the current path to measure the current

❑ Observer based methods

- The inductor current is estimated from the inductor voltage
- Highly sensitive to parameter variations (large error)

Digital Estimator: Principle of Operation



unknown

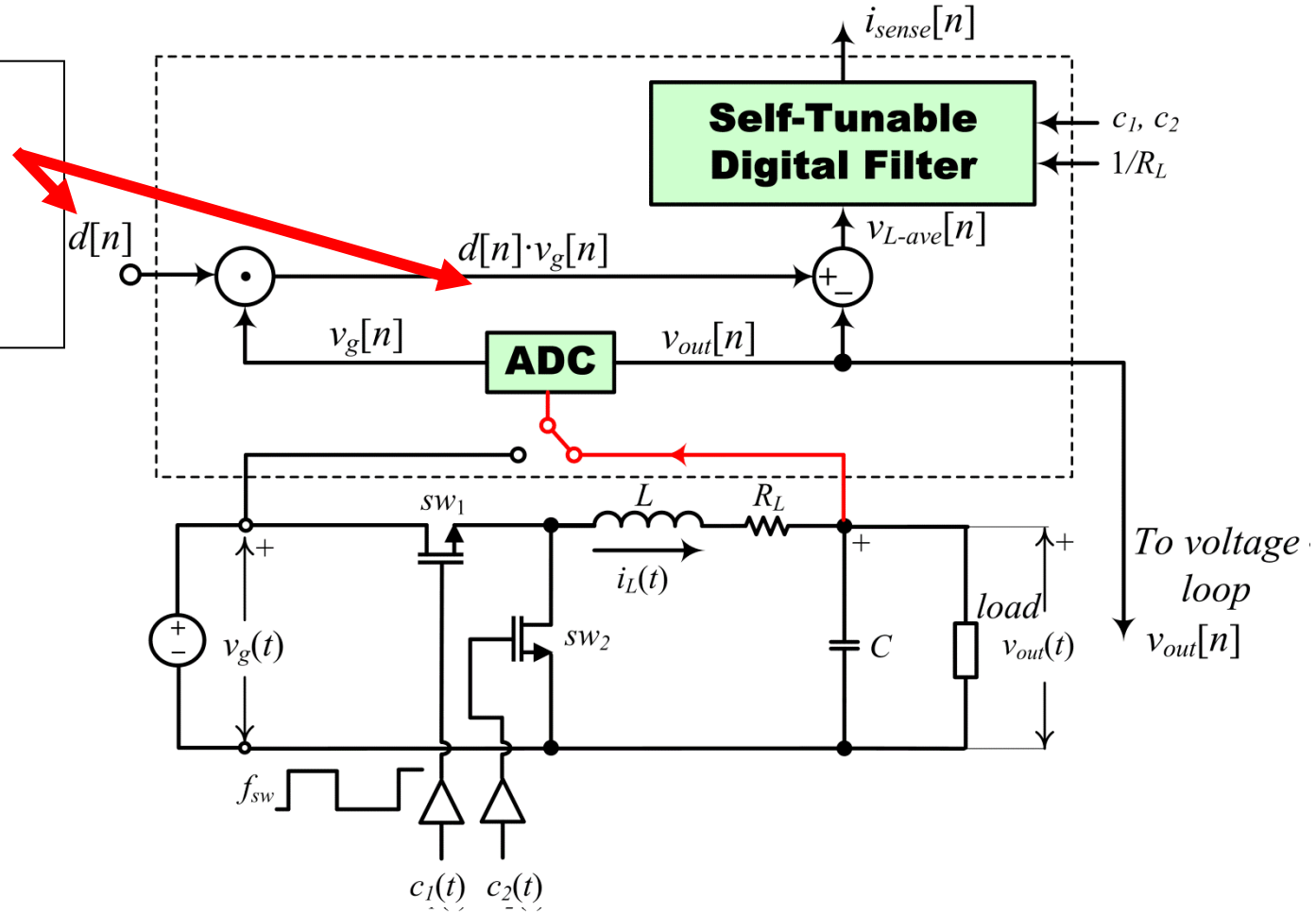
$$V_{sense}(s) = I_L(s) \cdot R_L \cdot \frac{1 + s \cdot \frac{L}{R_L}}{1 + s \cdot R_f C_f} = I_L(s) \cdot R_L \cdot \frac{1 + s \cdot \tau_L}{1 + s \cdot \tau_f}$$

$$\tau_L = \tau_F$$

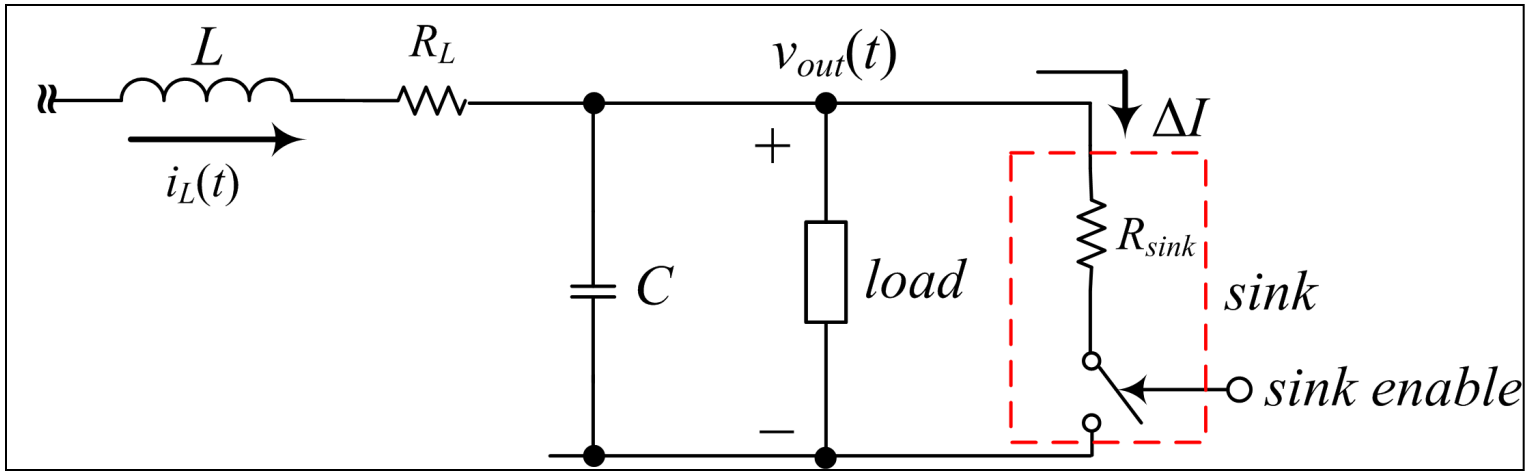
$$I_{sense}(s) = \frac{V_{sense}(s)}{R_L}$$

Implementation with Reduced Number of ADCs

The ADC of the voltage loop is shared and info about d[n] used

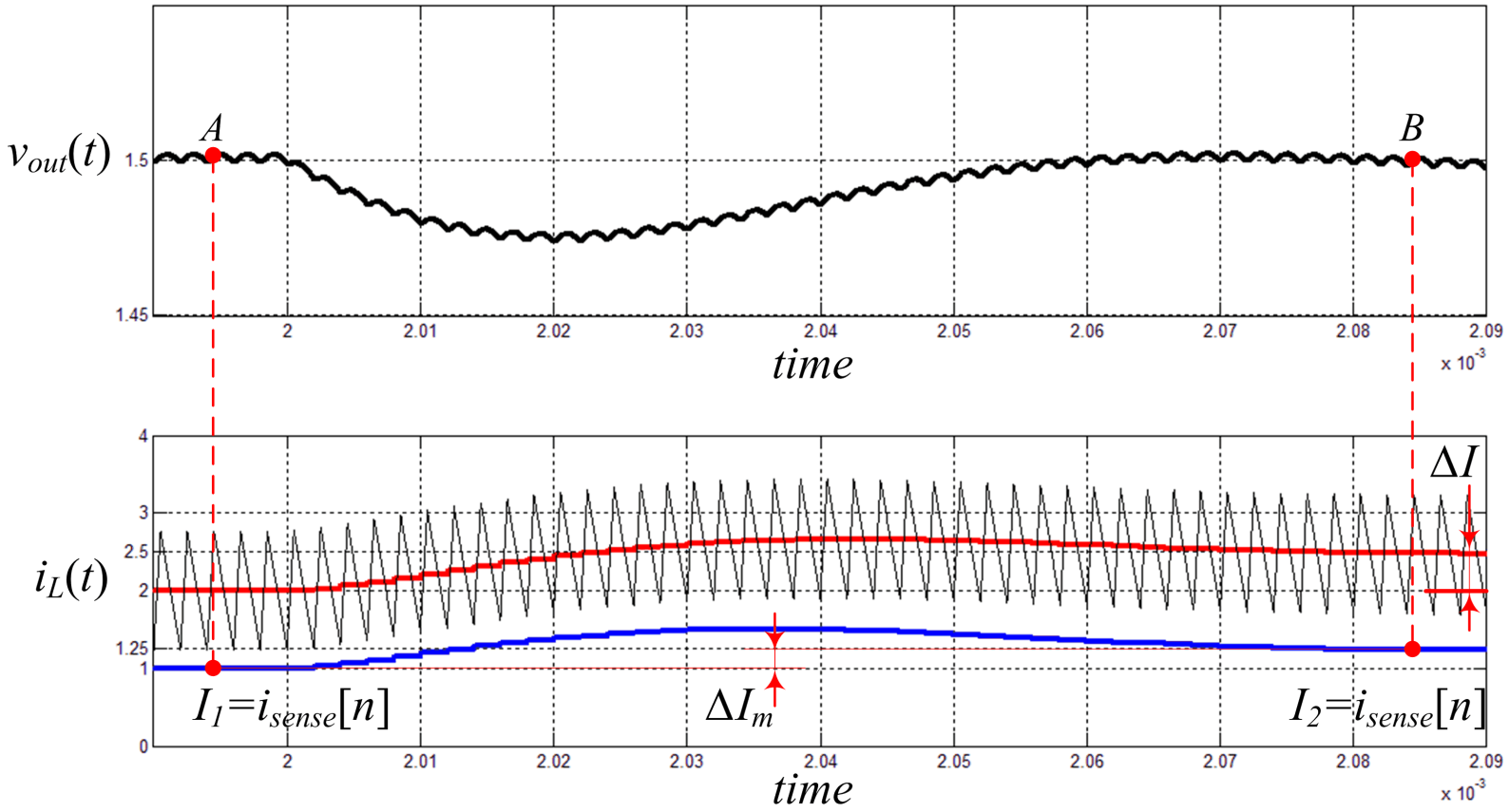


Filter Calibration With a Current Sink



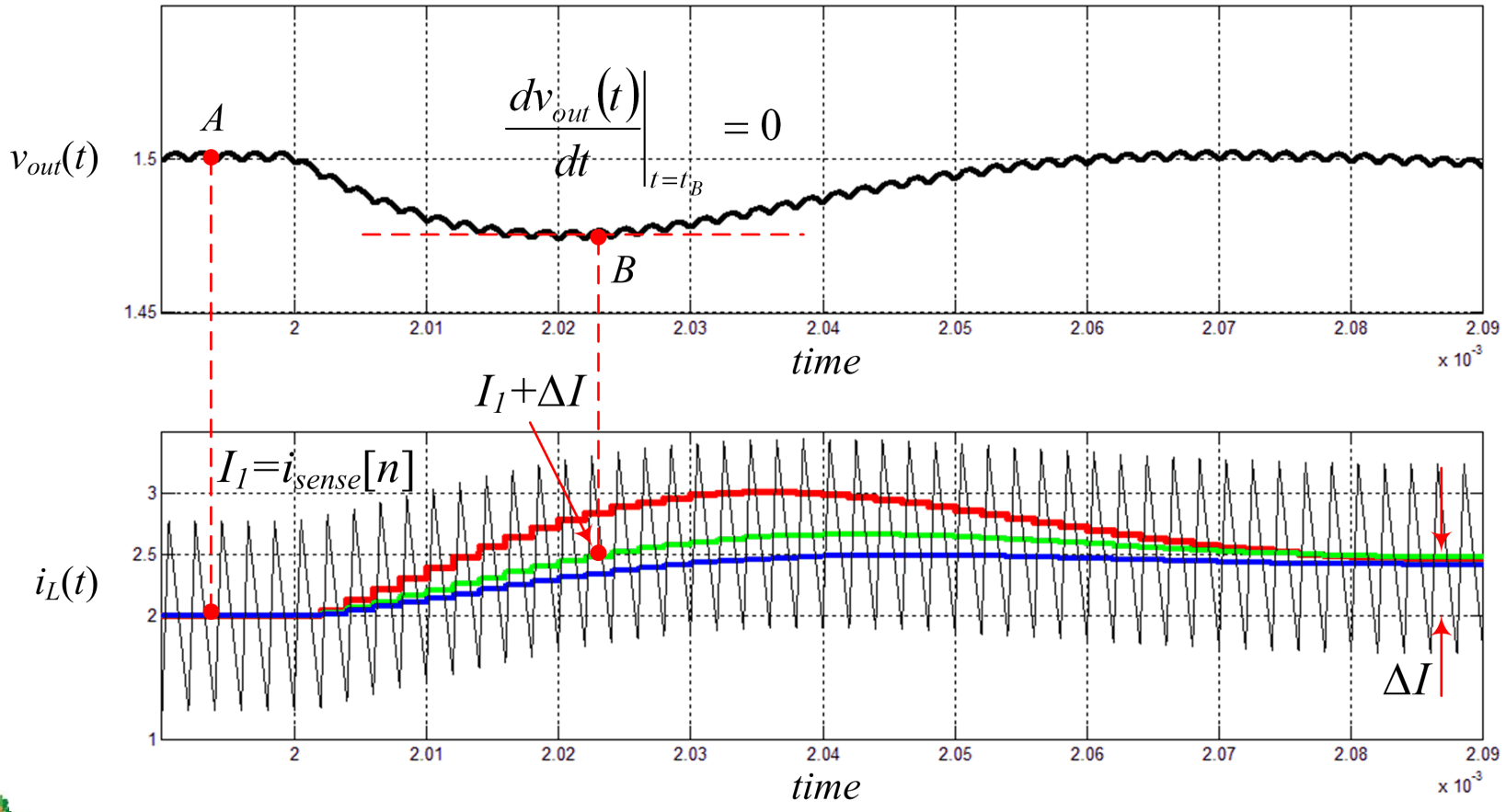
A known current step is introduced with a current sink and the response of the filter is observed

Filter Calibration: R_L



$$R_L = \frac{\Delta I_m}{\Delta I} R_{L\_inital}$$

Filter Calibration: L/R_L



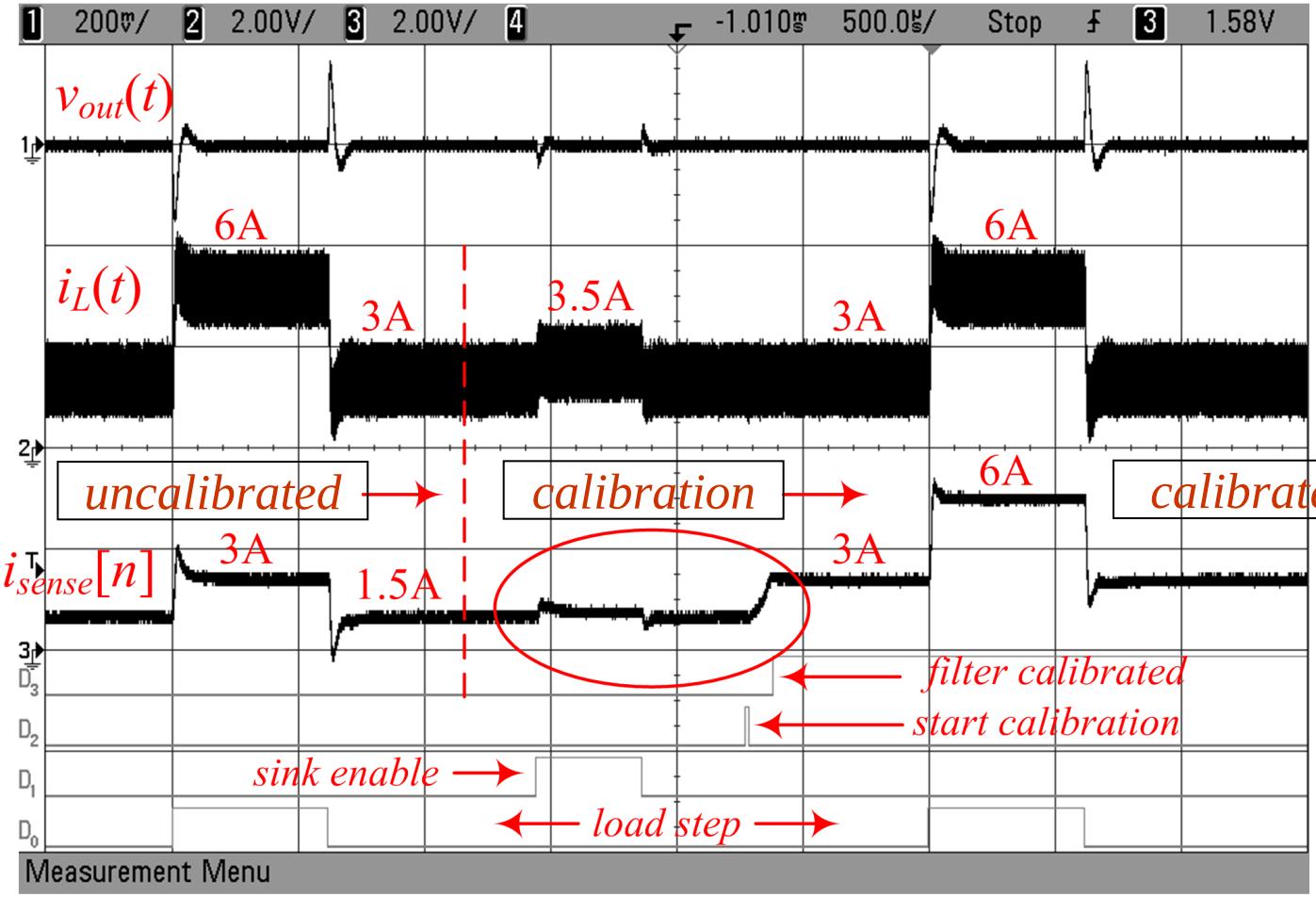
When the time constants are matched , values at the valley point are the same

Experimental Results: Calibration

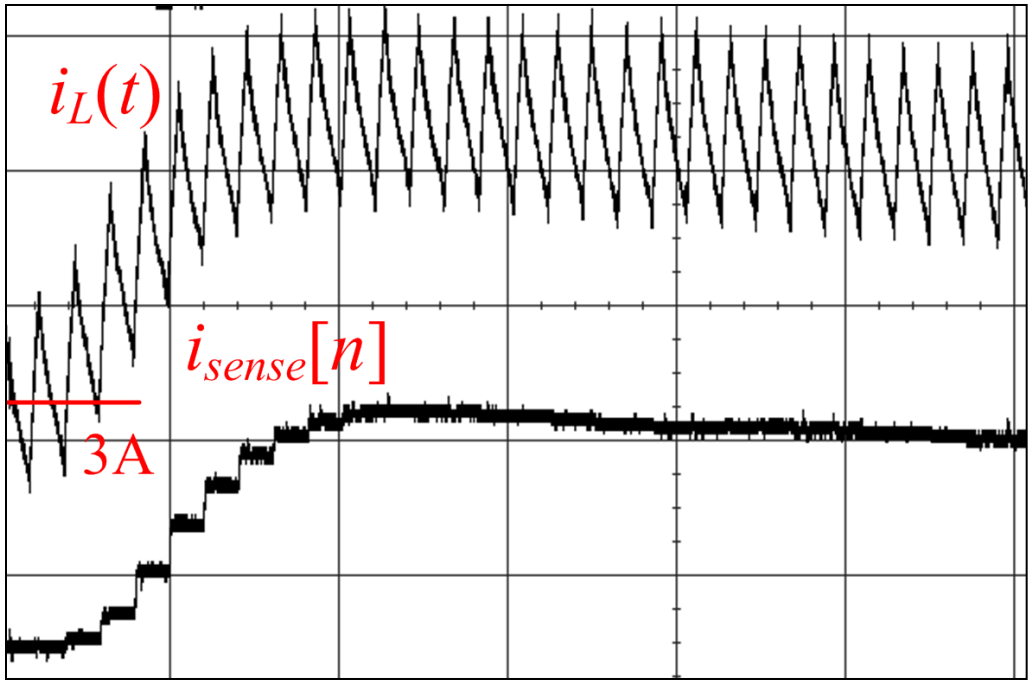
Output voltage

Inductor current

Estimated current



Experimental Results: Calibrated Operation

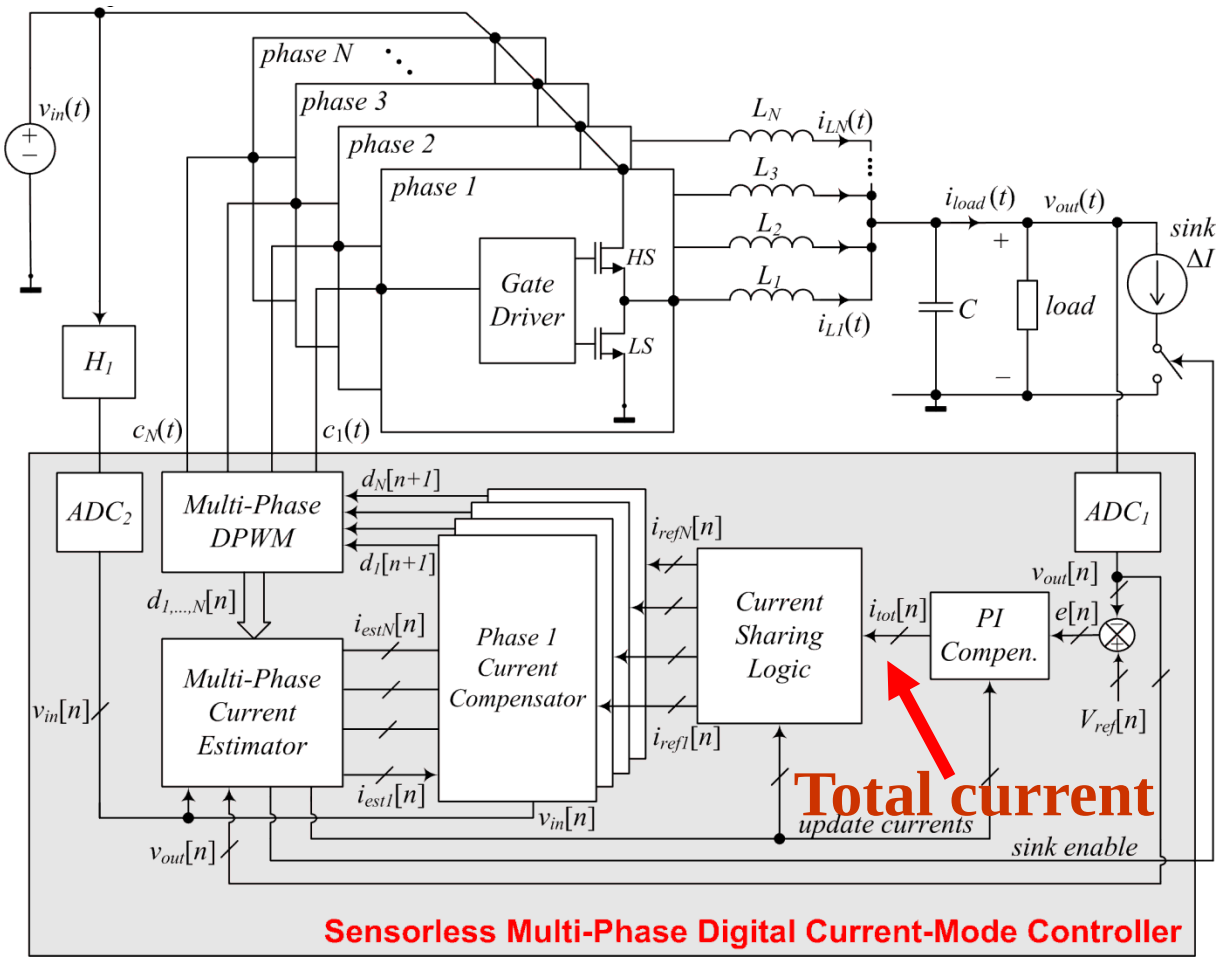


Inductor current

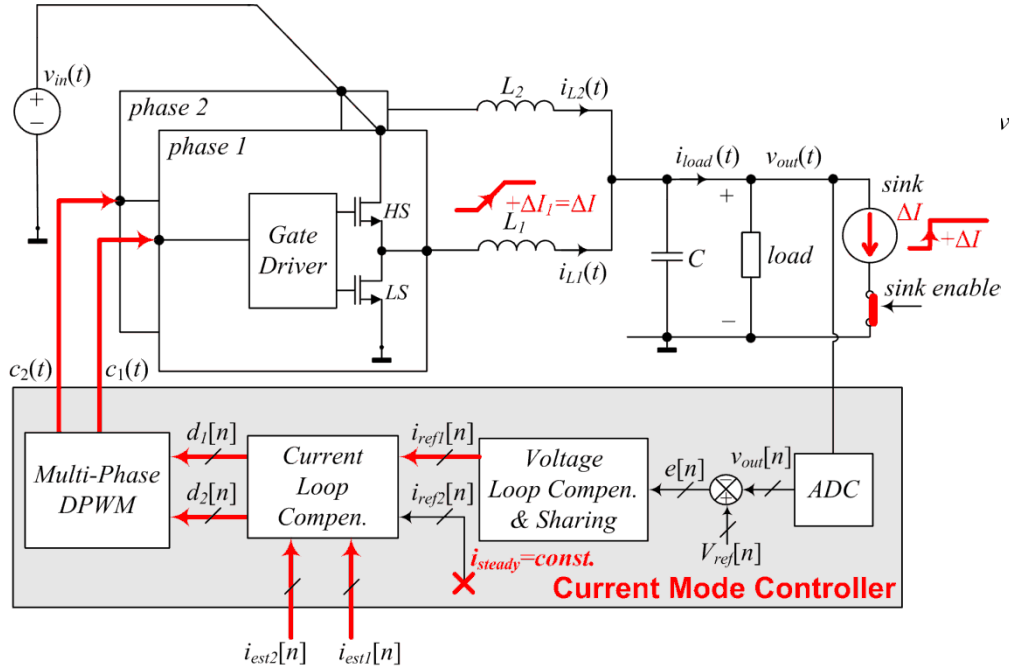
Estimated current

Extension on Multi-Phase Case

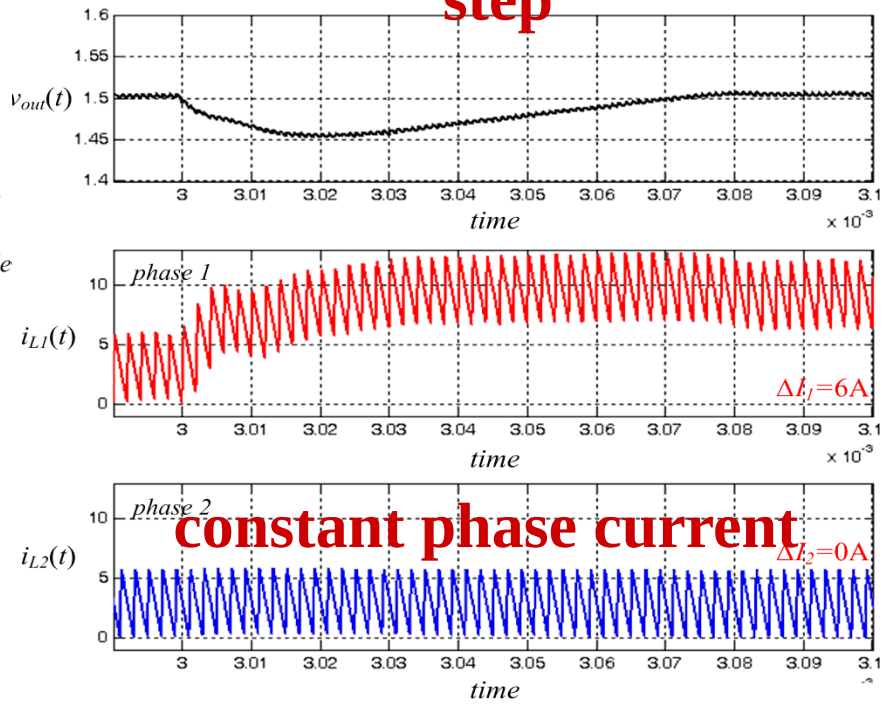
- *Total current is given by the voltage loop and the digital logic defines currents in each of the phases*
- *The currents are divided such that equal temperature is achieved between phases*



Phase-by-Phase Calibration



response to the sink circuit step



constant phase current

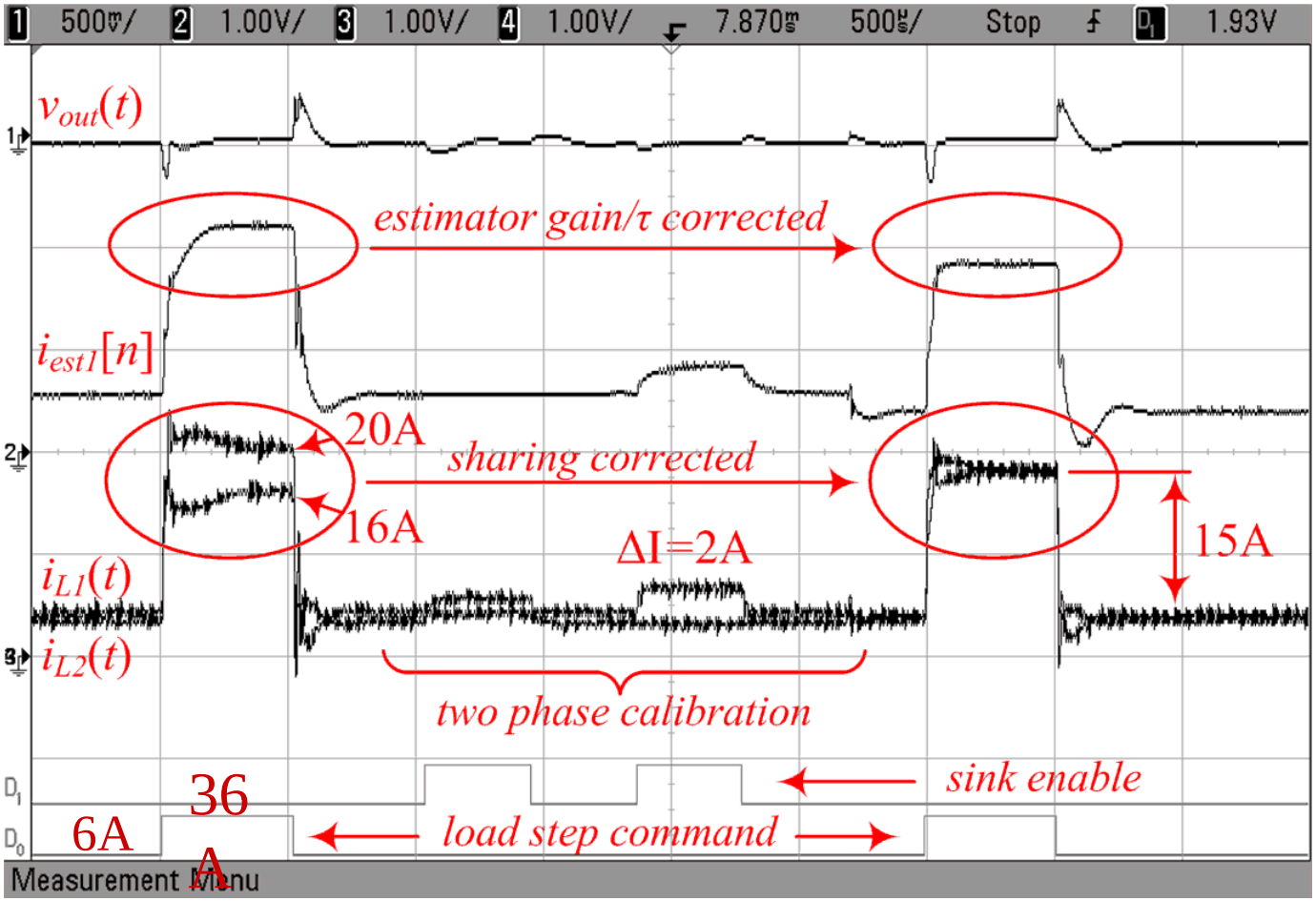
All current references but one are "frozen" and the active phase is calibrated

Experimental Results

Output voltage

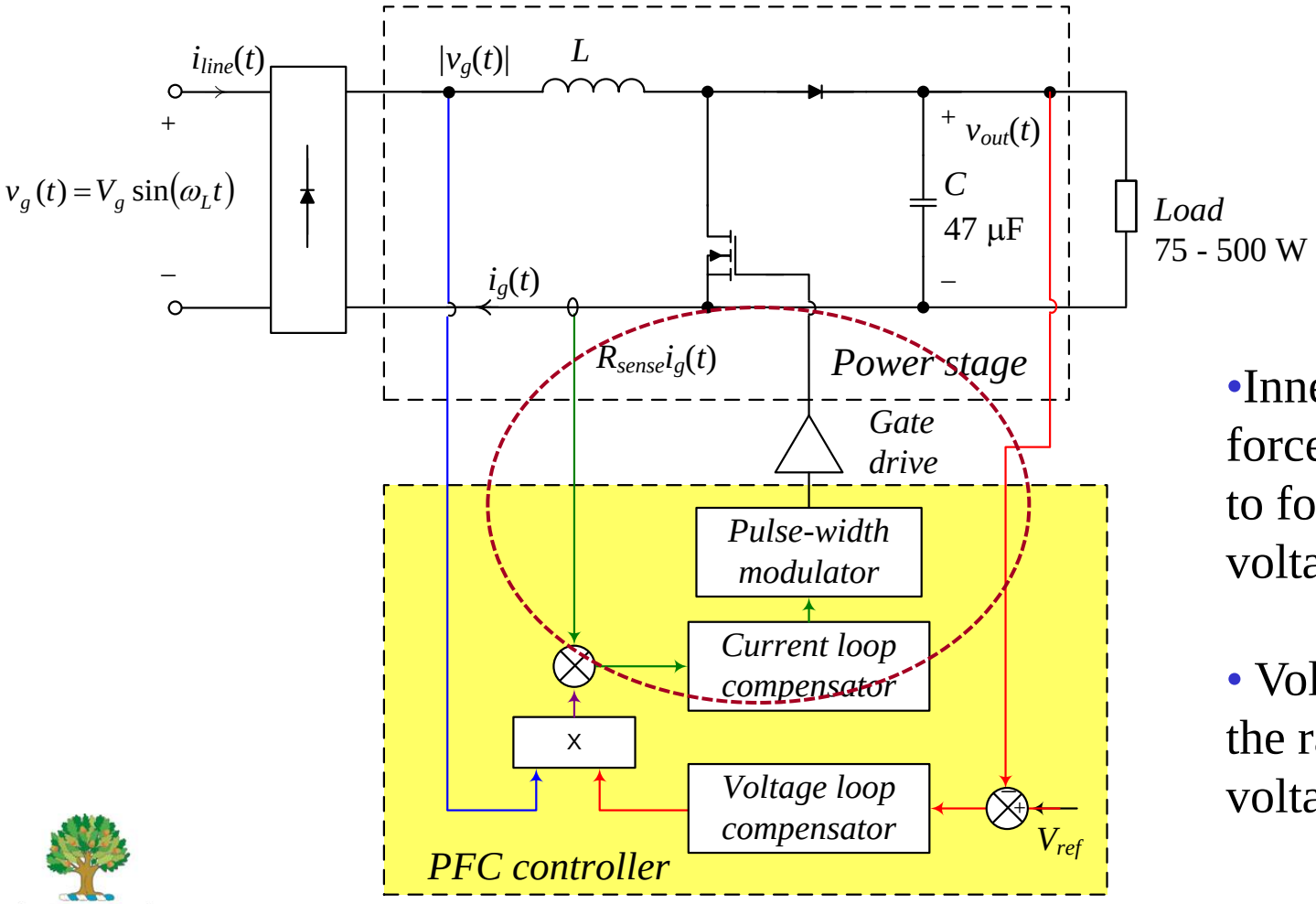
Estimated current of phase 1

Phase currents



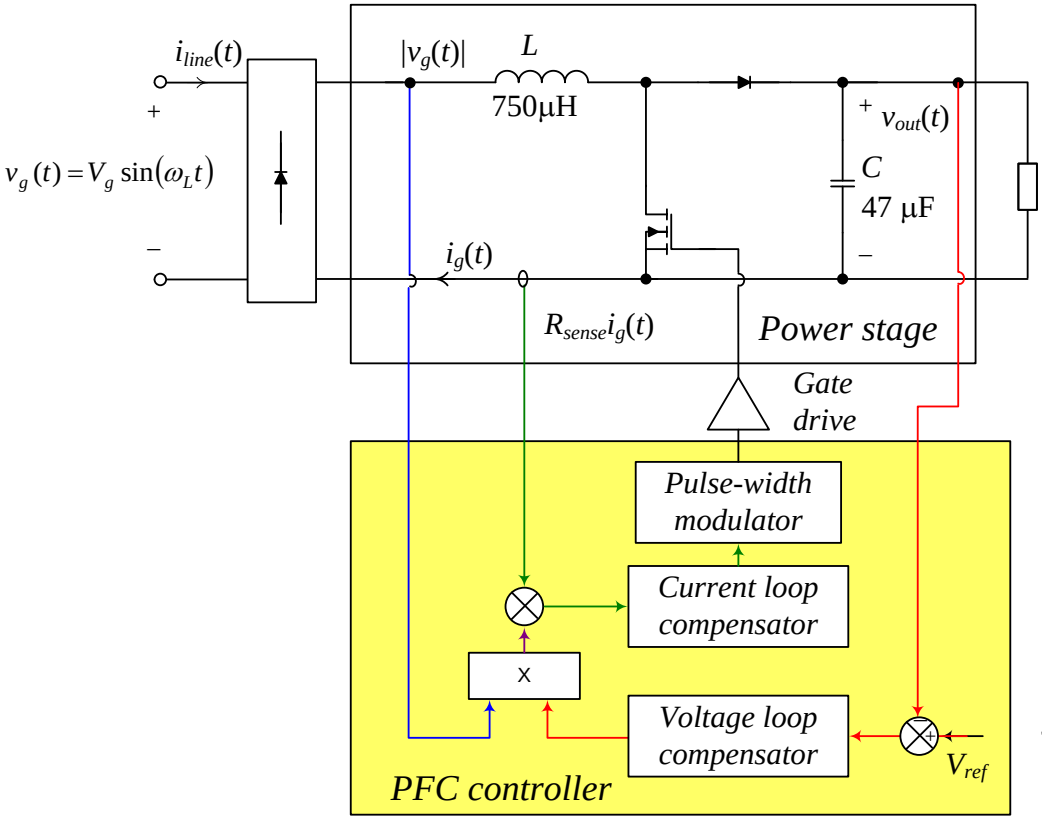
Advanced Digital Control for Rectifiers with Power Factor Correction (PFC Rectifiers)

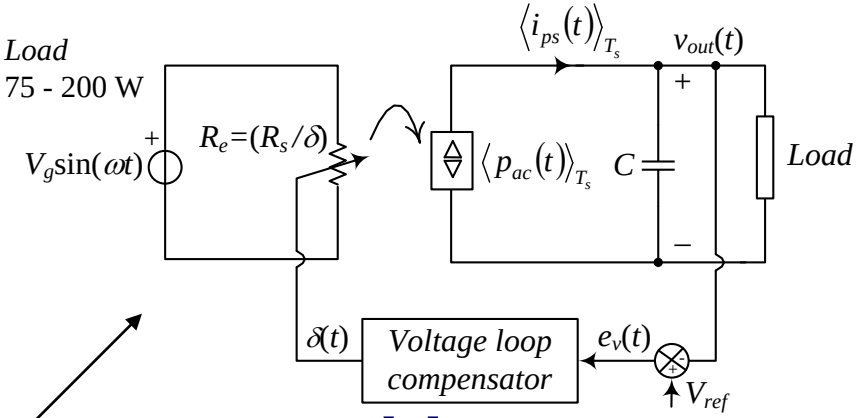
Boost – Based PFC Rectifier



- Inner current loop forces the input current to follow the input voltage waveform
- Voltage loop controls the ratio of the input voltage and current

Voltage Loop - Low Bandwidth Problem



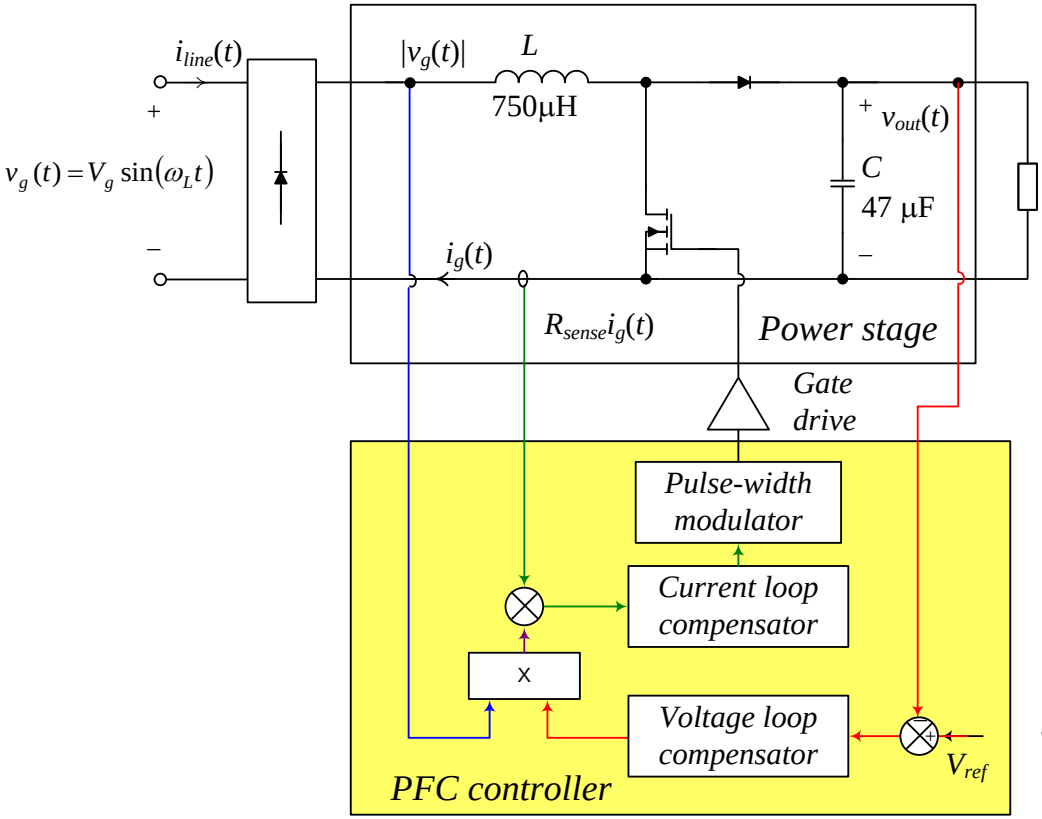


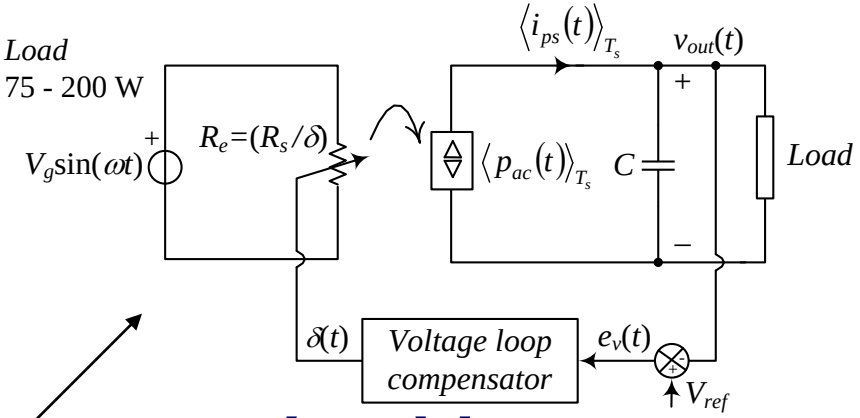
Average model

$$\langle p_{ac}(t) \rangle_{T_s} = \frac{V_g^2 \sin^2(\omega_L t)}{R_e} = \frac{V_g^2}{2R_e}(1 - \cos(2\omega_L t))$$

The voltage loop must not attempt to eliminate the output capacitor ripple through Re variations. Hence, it is usually designed to be very slow. We have a bulky high voltage cap.

PFC and Low-Bandwidth Voltage Loop Problem



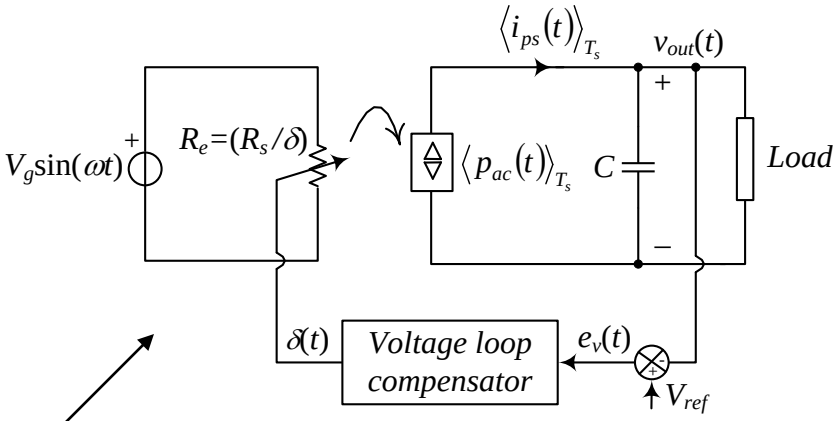


Averaged model

$$\langle p_{ac}(t) \rangle_{T_s} = \frac{V_g^2 \sin^2(\omega_L t)}{R_e} = \frac{V_g^2}{2R_e}(1 - \cos(2\omega_L t))$$

The voltage loop must not attempt to eliminate the output capacitor ripple through Re variations. Hence, it is usually designed to be very slow. Has a bulky high voltage cap.

General Ripple Problem

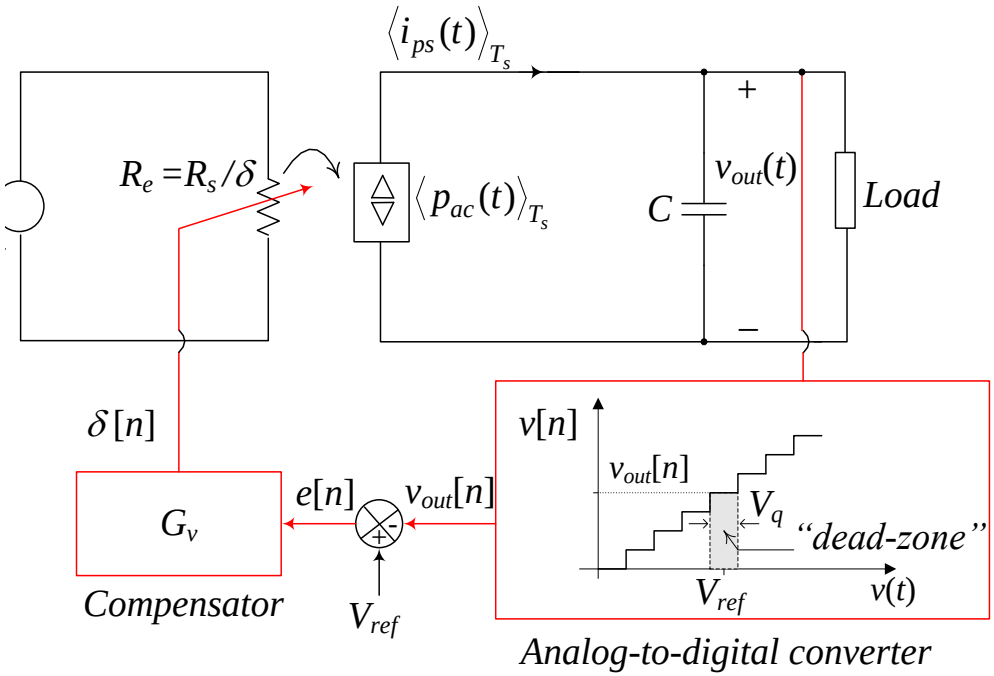


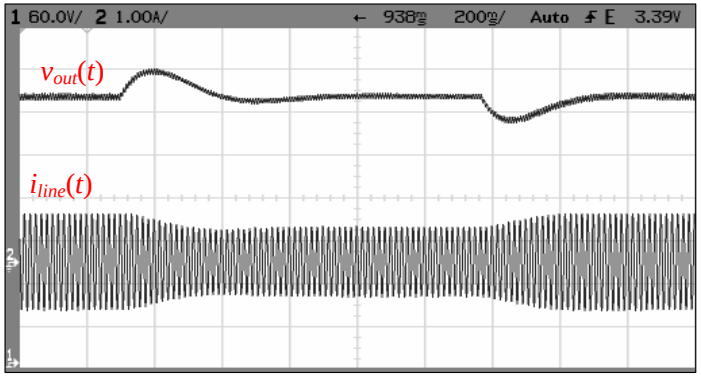
Averaged model

$$\langle p_{ac}(t)\rangle_{T_s} = \frac{V_g^2 \sin^2(\omega_L t)}{R_e} = \frac{V_g^{\,2}}{2R_e}\left(1-\cos(2\omega_L t)\right)$$

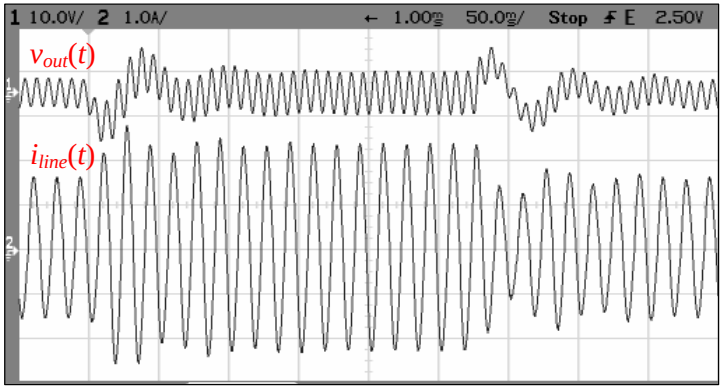
Also causes flicker in LED applications and puts unreasonable requirements for the output capacitor size in both LED supplies and universal adapter applications

Insensitive Zone Digital Controller





Time: 200 ms; Ch-1: vout(t) 60 V/div; Ch-2: iline(t) 1 A/div.



Time: 50 ms; Ch-1: vout(t) 10 V/div; Ch-2: iline(t) 1 A/div.

By utilizing insensitive zone in ADC we can drastically improve transient response.

Digital Control and Physical Limitations

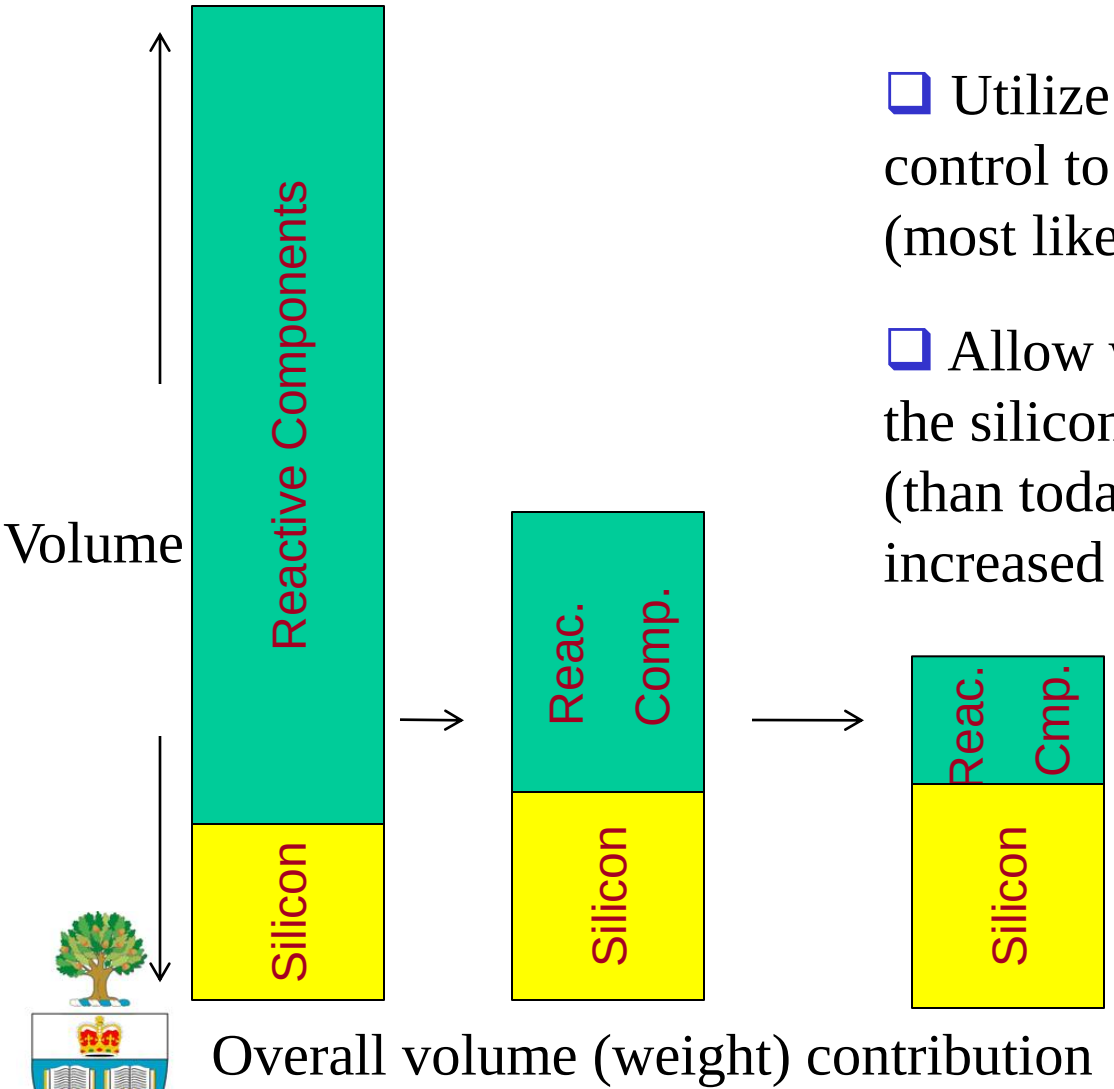
- Operation at high switching frequencies ✔
- Fast dynamic response of the controller ✔ - Pushed to physical limits
- Flat and high efficiency curve (efficiency close to the limit) ✔
- Introduced new features improving reliability and simplifying design ✔

Digital control is not only feasible but has also pushed existing converter topologies to their physical limits

Part IV

High Power Density Mixed-Signal Controlled Dc-Dc Converters (Emerging Topologies)

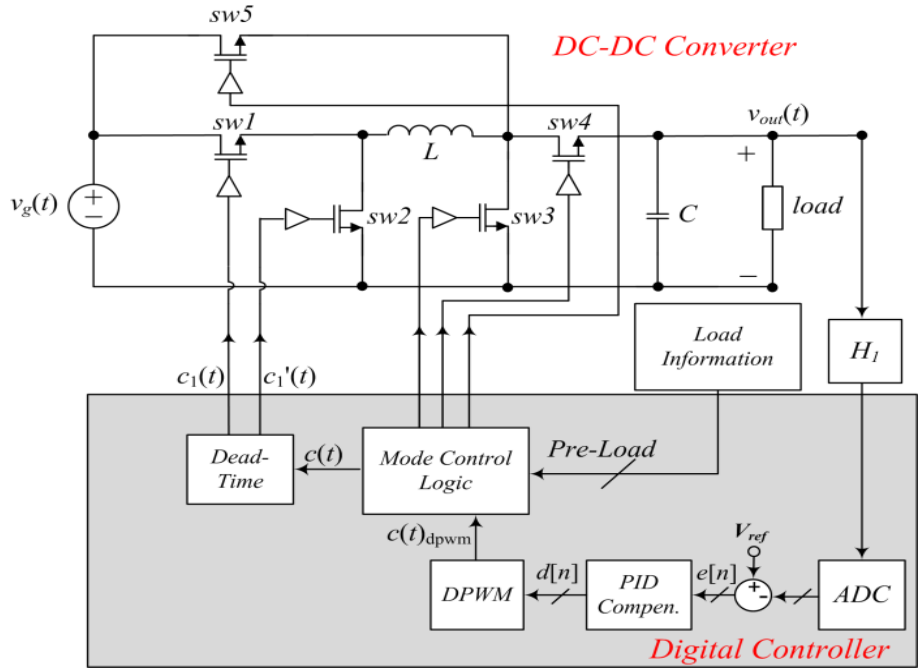
Moving Forward- Utilization of Digital (Mixed) Signal Control



- Utilize flexibility of mixed-signal control to develop higher power density (most likely more complex) topologies.
- Allow weight (cost) distribution where the silicon will take a large percentage (than today). Note, not necessarily increased silicon area.
- Improved power processing efficiency
- Natural evolution, seen in other areas, i.e. higher power applications

Example 1: Load-Interactive Steered-Inductor DC-DC Converter with Minimized Output Filter Capacitance

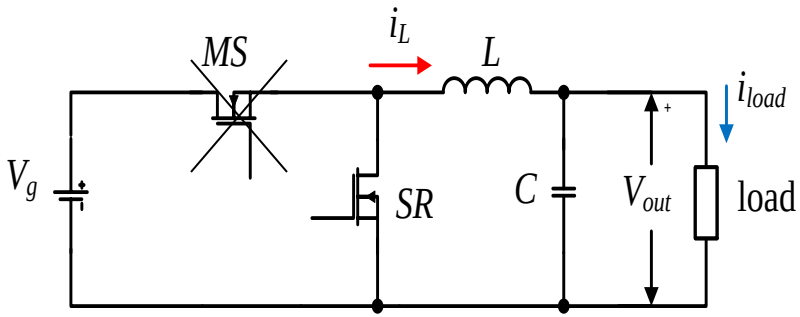
Load Interactive SMPS with Current Steering

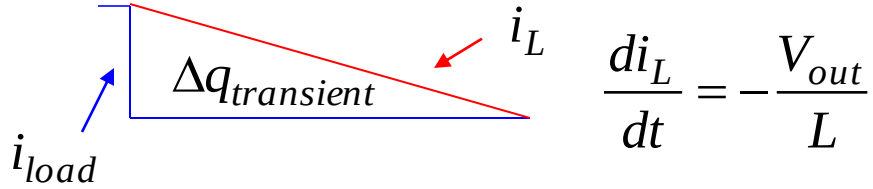


- Uses improved interaction (bidirectional comm.) with the digital loads: uses info about upcoming load change to either pre-charge inductor current or steer it away.
- At the expense of few transistors (two with low voltage) and more complex control, ideally, allows selection of the capacitor based on the ripple criteria only.

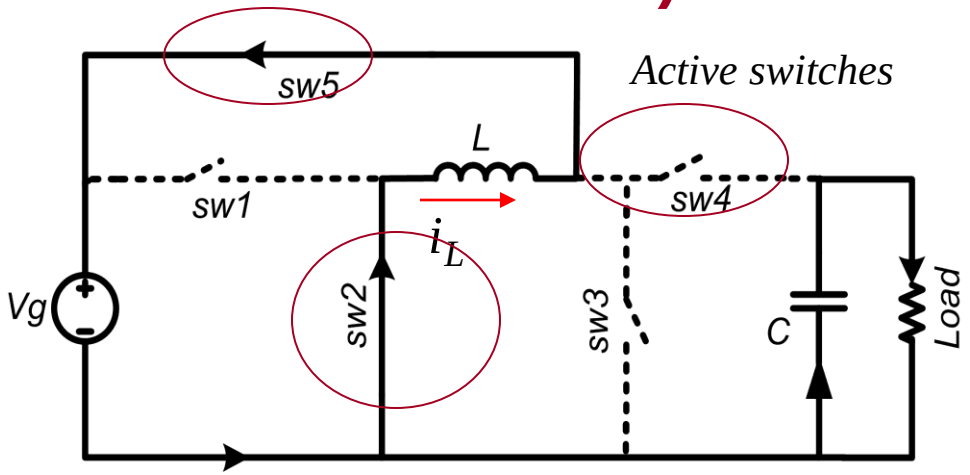
[1] S.M. Ahsanuzzaman, A. Parayandeh, A. Prodić, D. Maksimović, "Load-interactive steered-inductor dc-dc converter with minimized output filter capacitance," in Proc. IEEE (APEC), 2010, Pg. 980-985.

Steered Inductor Buck-Boost: Heavy to Light load Transient Operation (Comparison with Standard Buck)





$$\frac{di_L}{dt} = -\frac{V_{out}}{L}$$



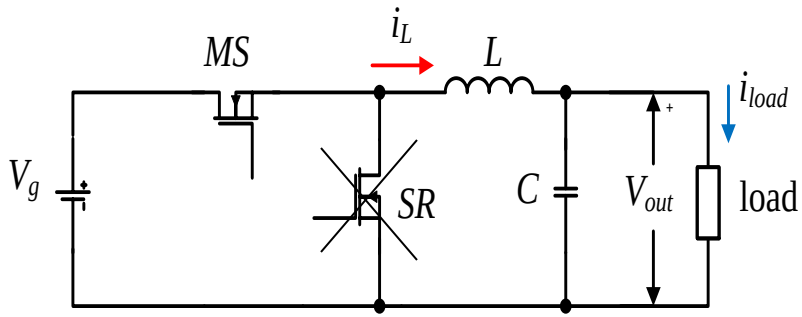
- After a heavy-to-light transient is detected ,the current is steered away from the capacitor to the source.

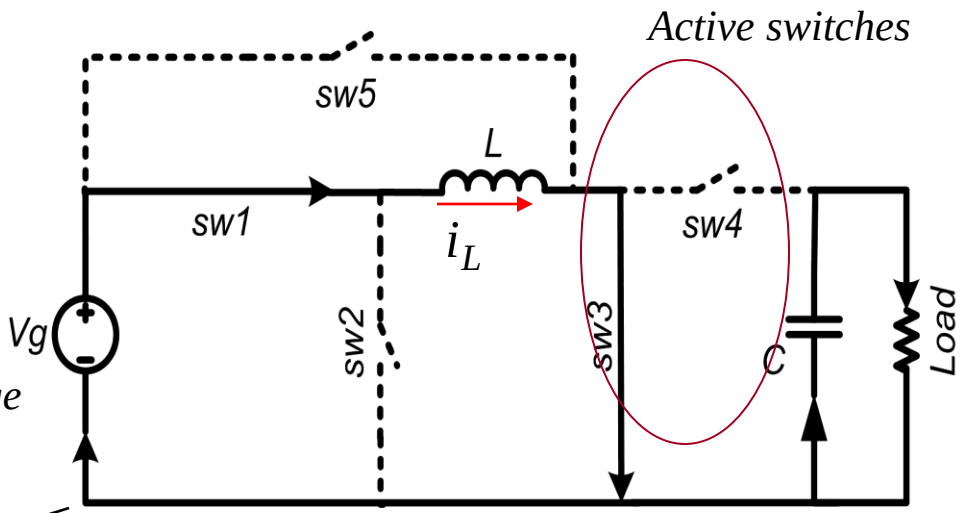
  - Voltage overshoot $\Delta v = \Delta q_{trans} C$ is eliminated

  - Transient excess of energy ($W = 1/2 \Delta q_{trans} C$) is recycled (rather than burnt on the load), for highly dynamic loads this represents a significant savings

- The current slew-rate is increased to $-V_g/L$ from $-V_{out}/L$ in buck mode

Steered Inductor Buck-Boost: Light to Heavy Load Operation (Comparison with Standard Buck)





Pre-load command from the load

Load change OK

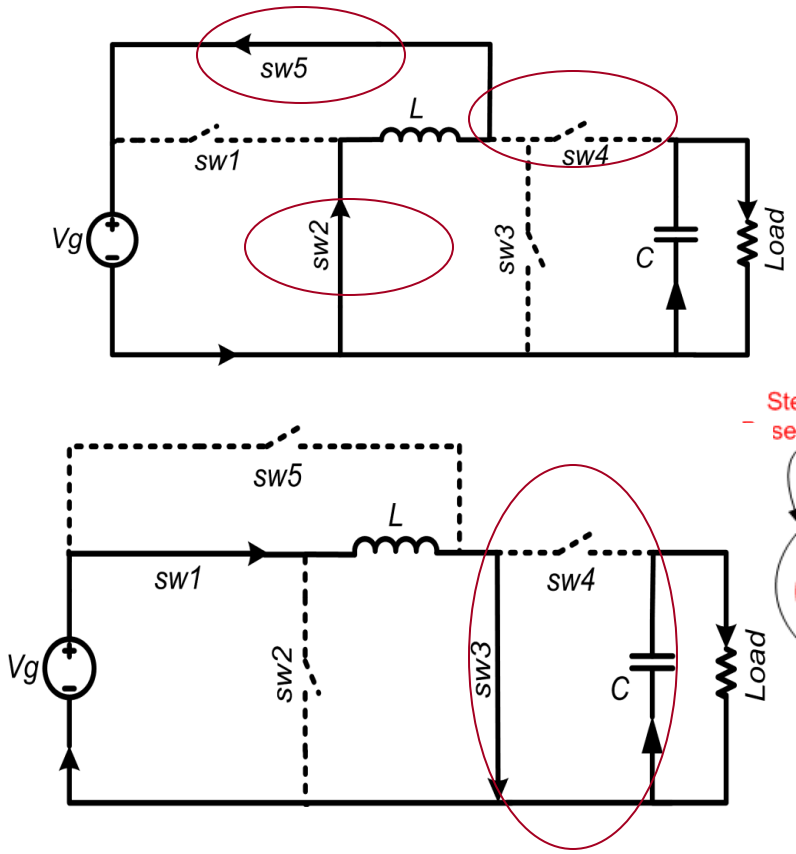
i_L

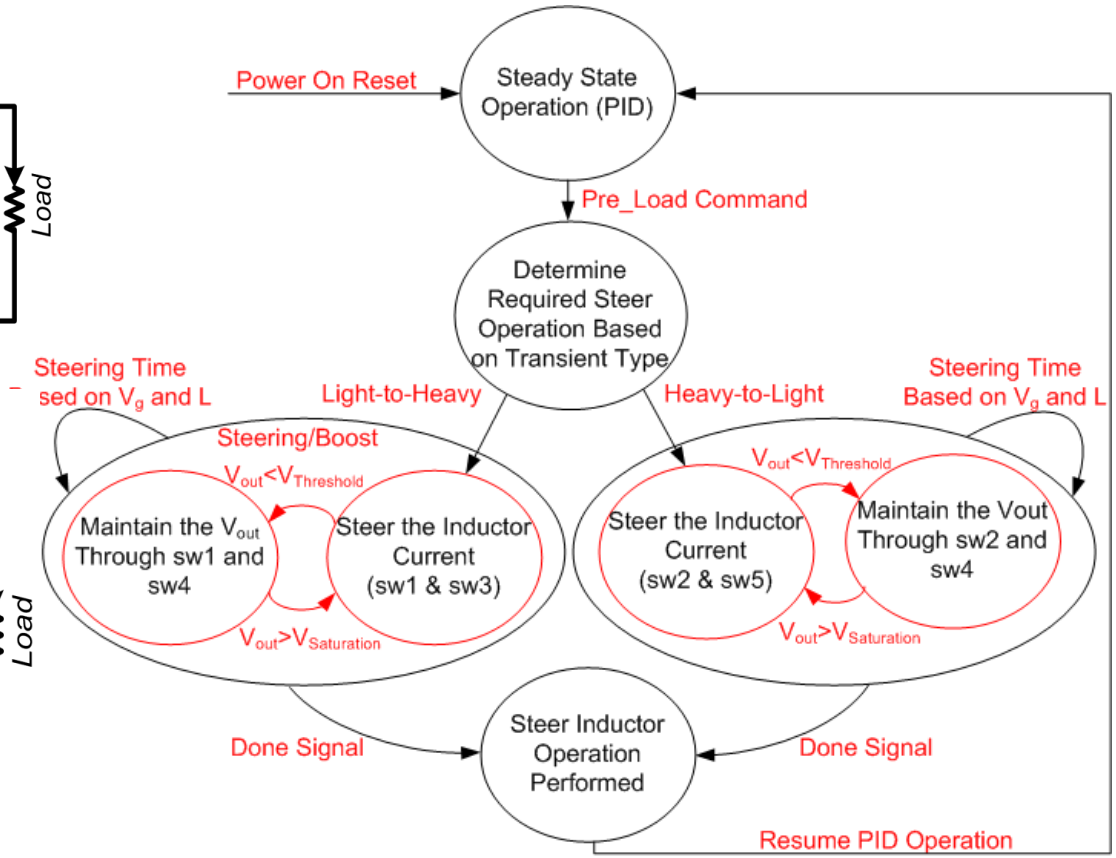
$$\frac{di_L}{dt} = \frac{V_g}{L}$$

$$\frac{di_L}{dt} = \frac{V_g - V_{out}}{L}$$

- Light-to heavy pre-transient condition current "pump-up"
- At the point when the inductor current is equal to the new load value
- Ideally, capacitor has zero Δq_{trans} since no extra current is taken from it.

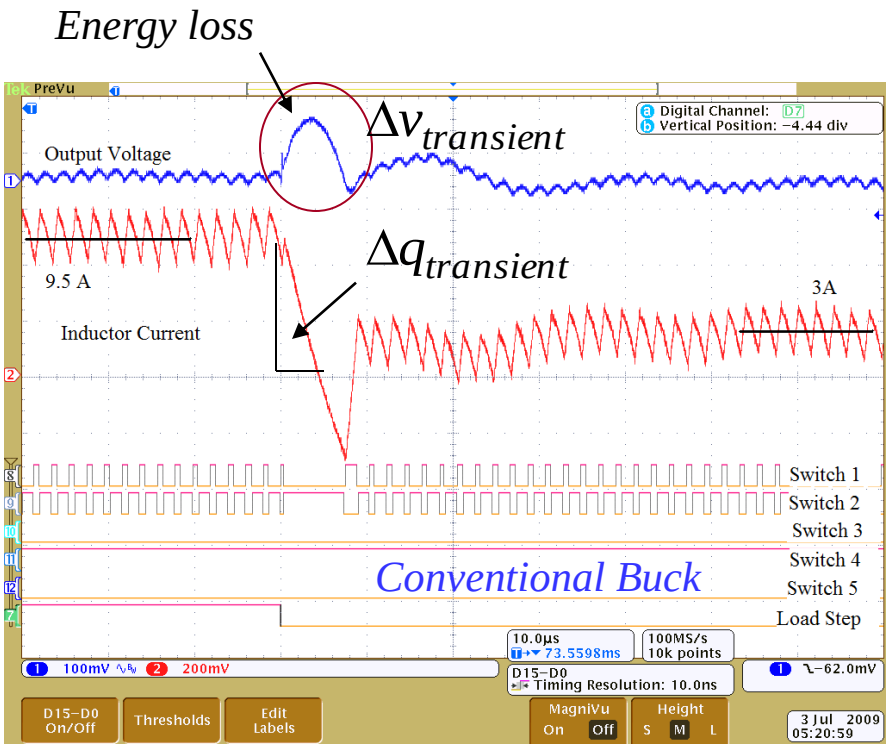
State-Machine Digital Logic

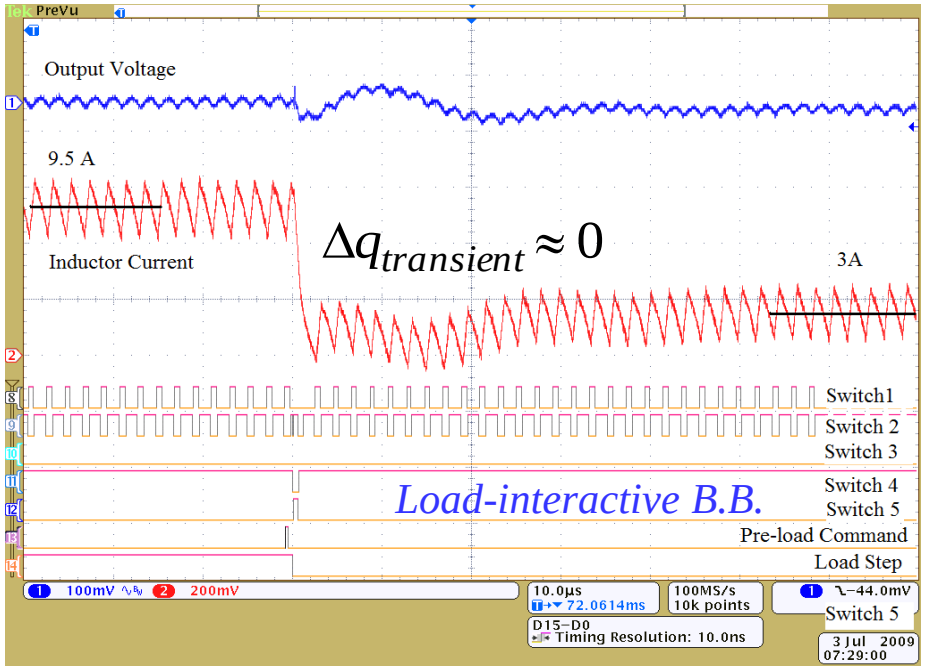




The digital logic keeps voltage regulated during charge up and current steering phase and also provides bump-less mode transitions.

Load Transient Performance – Realistic System





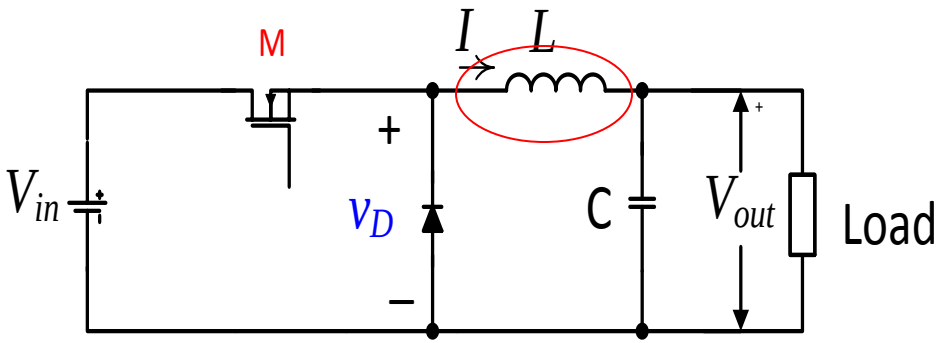
Exp. System: About 4 x smaller deviation than that of an optimum response system => allows for proportional reduction of the output filter capacitor.

Caution: system delays and mode transitions could cause significant overshoots and undershoots.

Reducing Inductor

We haven't fully addressed the inductor volume reduction yet and in numerous applications it is the largest contributor to the overall volume.

Inductor Volume Reduction – Basic Principles



$$Volume\_L \approx k_2\left(\frac{1}{2}LI^2\right)$$

k_2- *depends on the type of inductor*

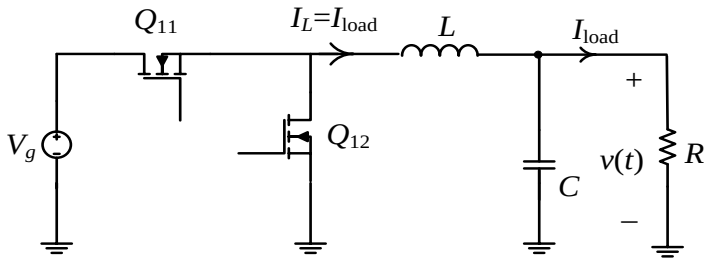
Three principles for the inductor volume reduction/elimination that will be shown here:

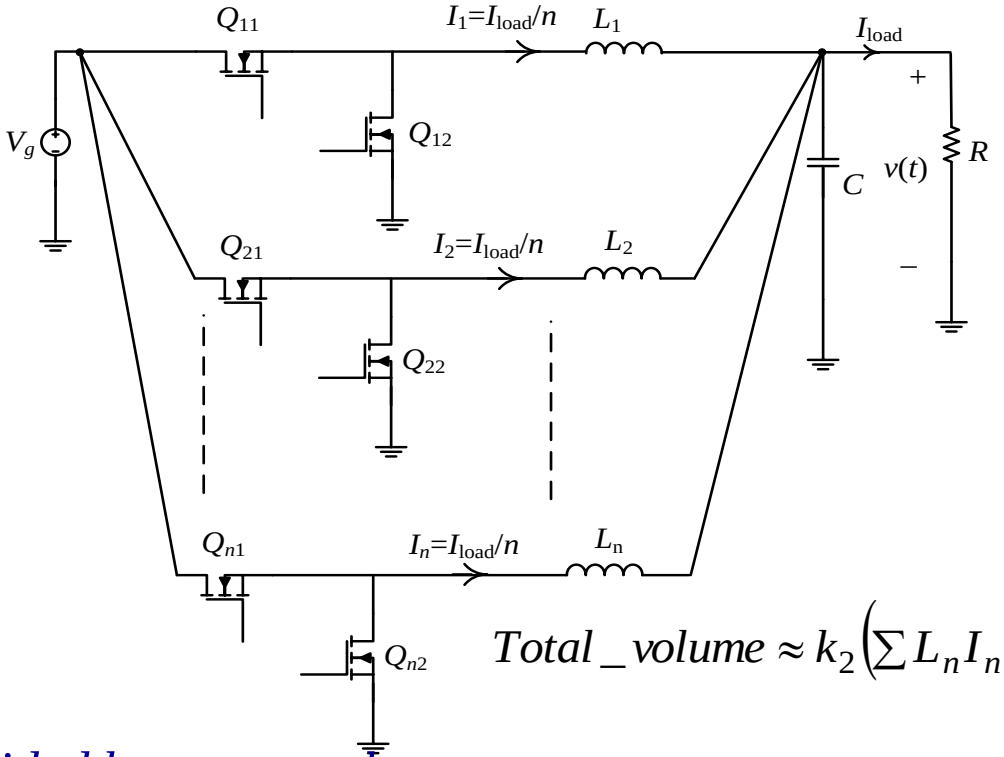
- *Current division (reduction of the inductor current)*
- *Elimination (switched capacitor based topologies)*
- *Inductor volt-second swing reduction (hybrid and multi-level converter topologies)*

Main focus

Current Division: Interleaved/Parallel Structures

Parallel (Interleaved) Structures[1]



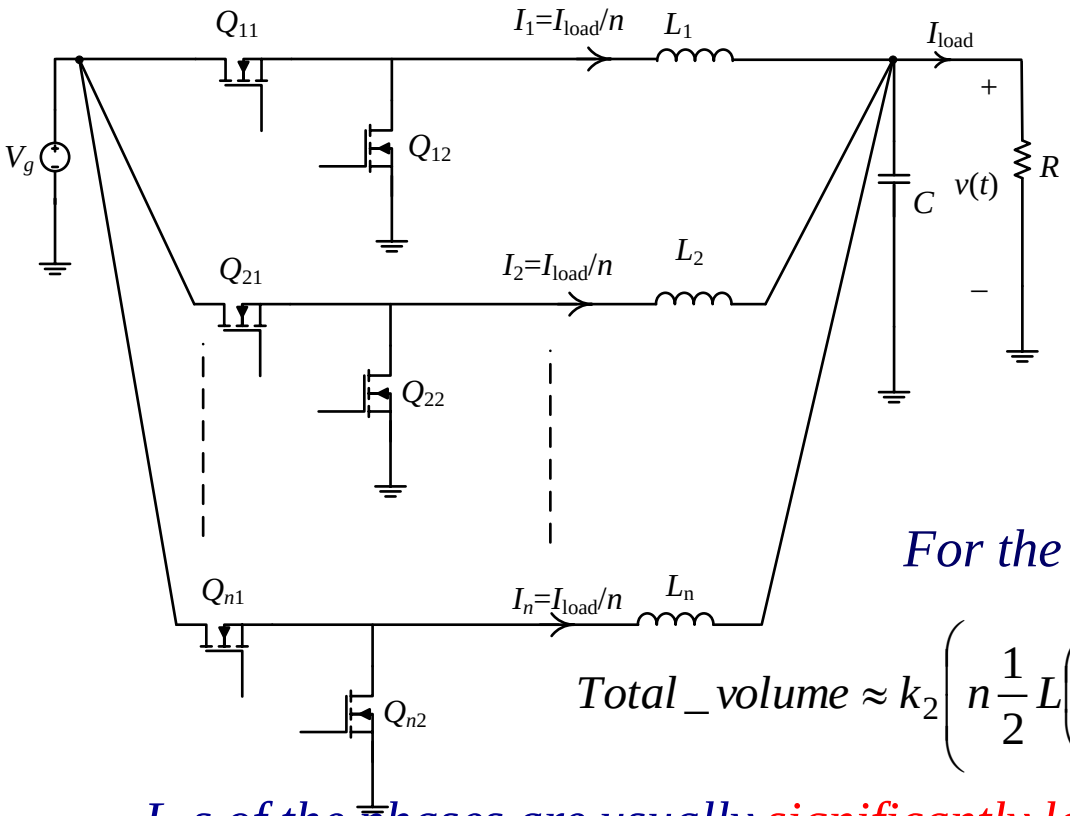


$$Total\_volume \approx k_2\left(LI_{load}^{\ 2}\right)$$

$$Total\_volume \approx k_2\left(\sum L_n I_n^{\ 2}\right)$$

- *Load (inductor) current is divided between n-phases*
- *Effectively => higher switching frequency is produced*
- *Smaller output capacitor and smaller input filter (including input filter)*
- *Total inductor volume can be reduced but we need to pay a price*

Interleaved Structures



For the same Ls (not working great)

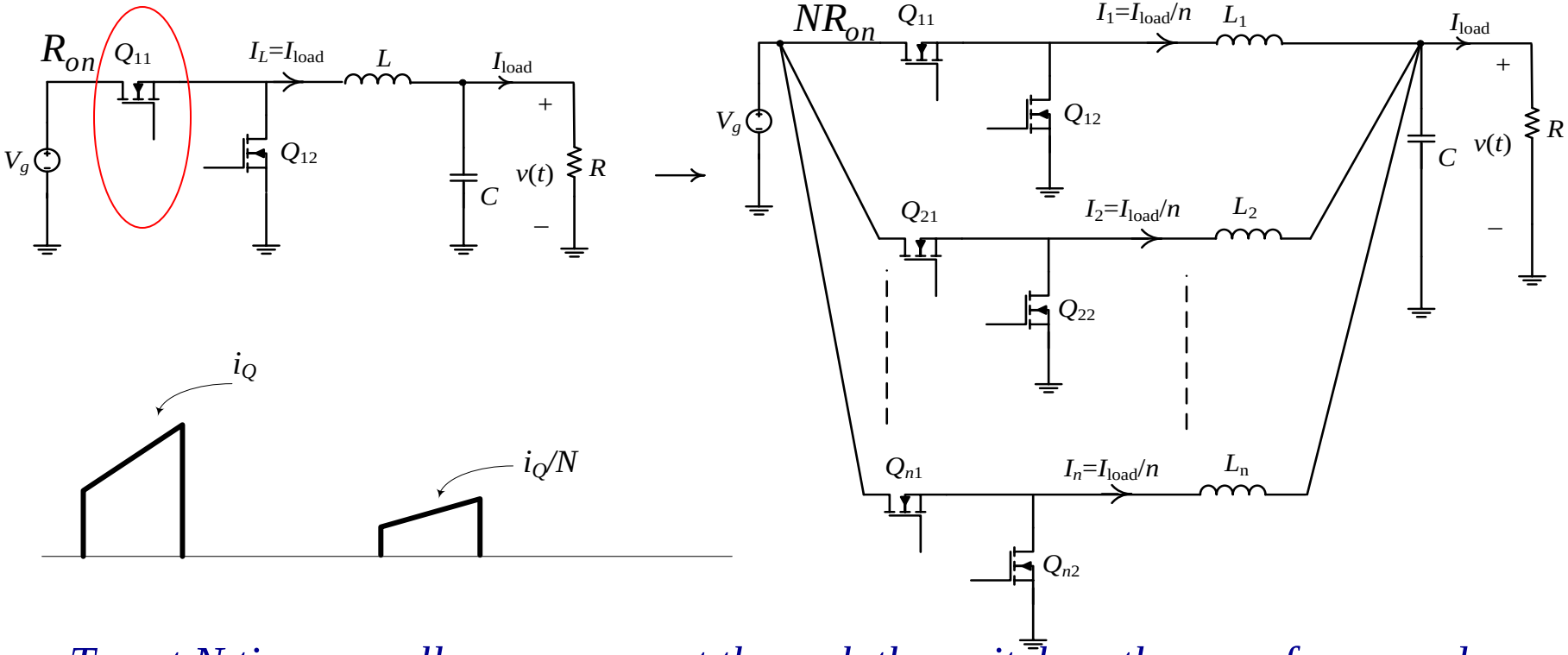
$$Total\_volume \approx k_2\left(n\frac{1}{2}L\left(\frac{I_{load}}{n}\right)^2\right)=\frac{Volume\_conventional}{n}$$

-L-s of the phases are usually significantly larger than that of the single phase

-Unfortunately, the silicon area and switching losses do not scale that well

- Still, the benefits of loss distribution C and input filter minimization are very significant

Interleaved Structures - Losses



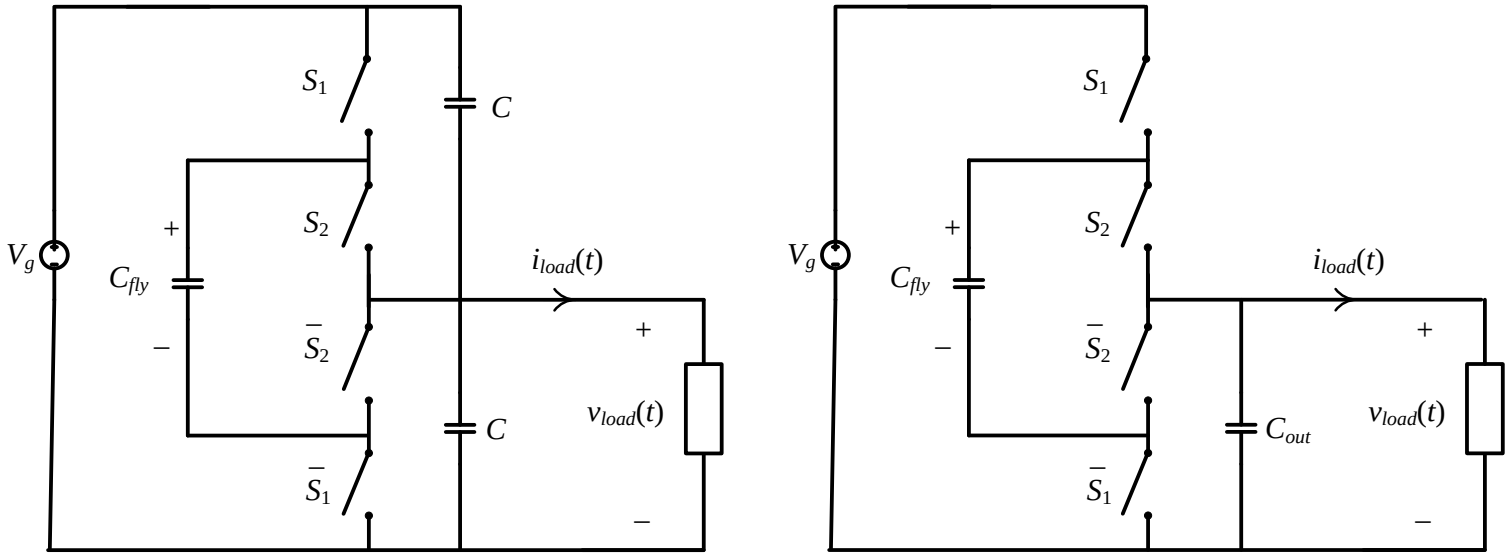
To get N times smaller rms current through the switches the waveform needs to be scaled version of the original current => inductance per phase needs to be N times larger

$$Total\_volume \approx k_2\left(n\frac{1}{2}nL\left(\frac{I_{load}}{n}\right)^2\right) = volume\_one\_phase$$

Elimination: Inductor-less structures

(Switched Capacitor Converters)

Inductor Elimination: Switched Capacitor Converters



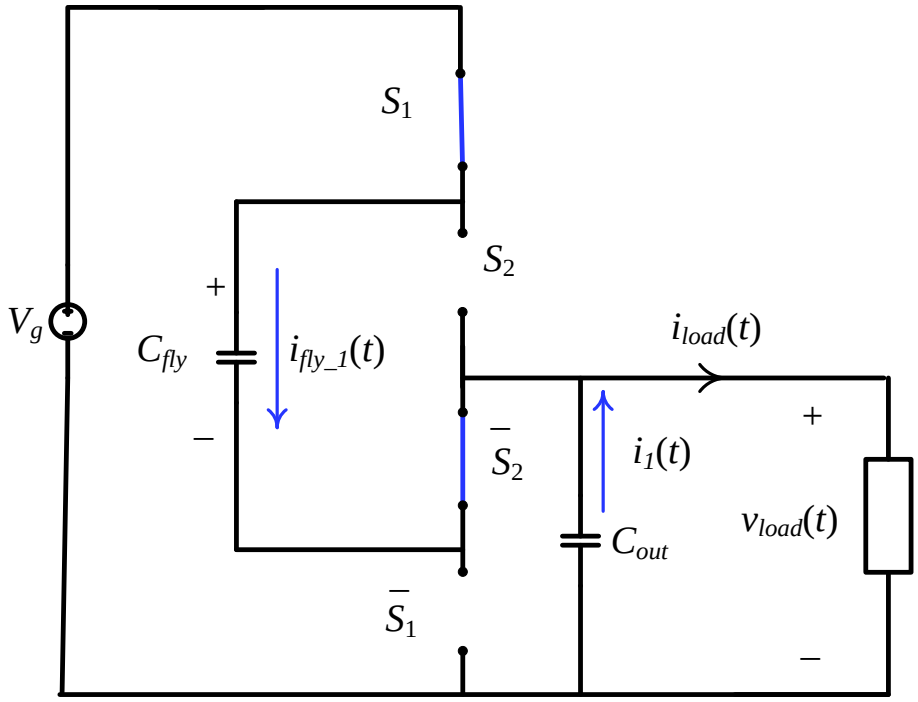
$$V_{out} = \frac{V_g}{2}$$

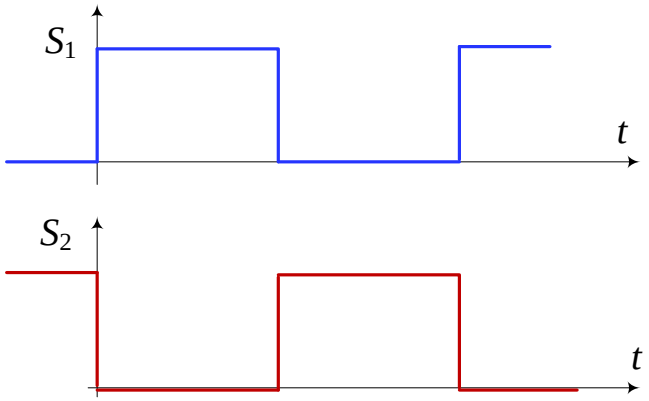
- *Idea: perform all power processing with capacitors only, since they have higher energy density than the inductors*

[1] M.D. Seeman, and S. R. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," IEEE Trans. on Power Electron., vol. 23, pp. 841 – 851, Mar. 2008.

[2] D. Maksimovic, and S. Dhar, "Switched-capacitor dc-dc converters for low-power on-chip applications," in Proc. IEEE Power Electronics Specialists Conf., 1999, pp. 54-59. Aug. 1999.

Principle of Operation

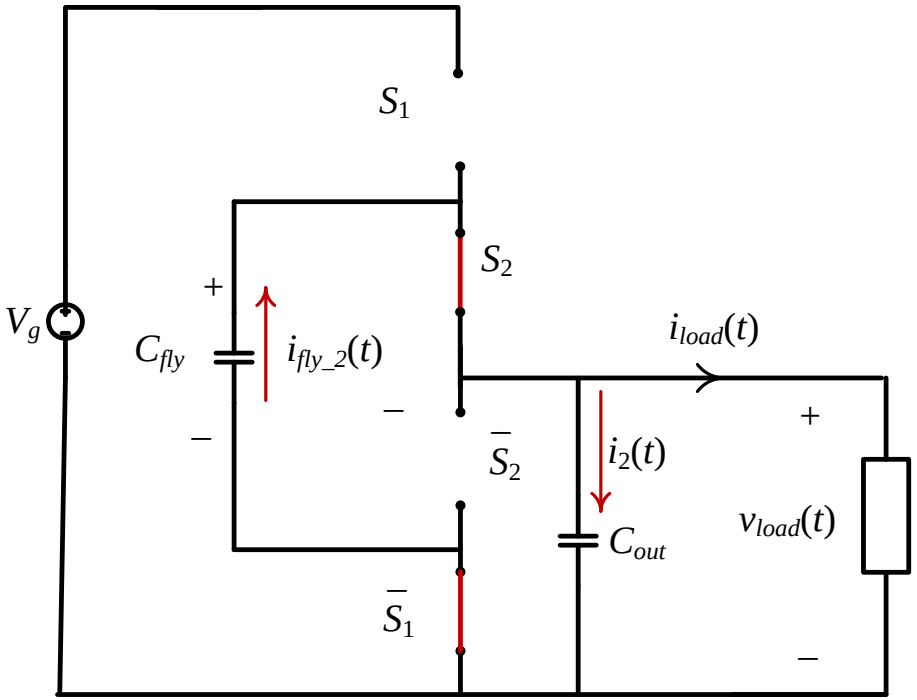


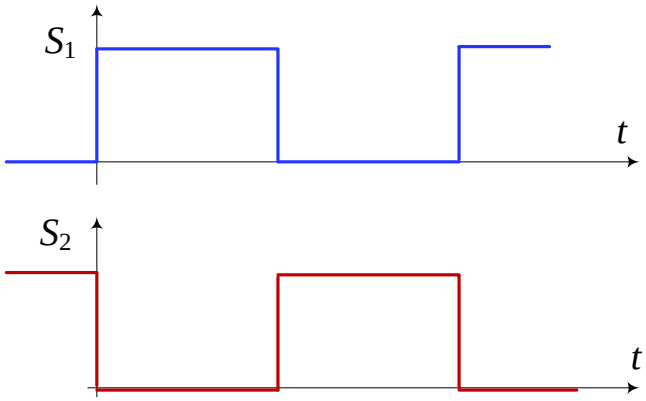


$$i_{load} = i_{fly} + i_1$$

Period 1: Flying capacitor C_{fly} is charging with i_{fly_1} and C_{out} discharging with i_1

Principle of Operation

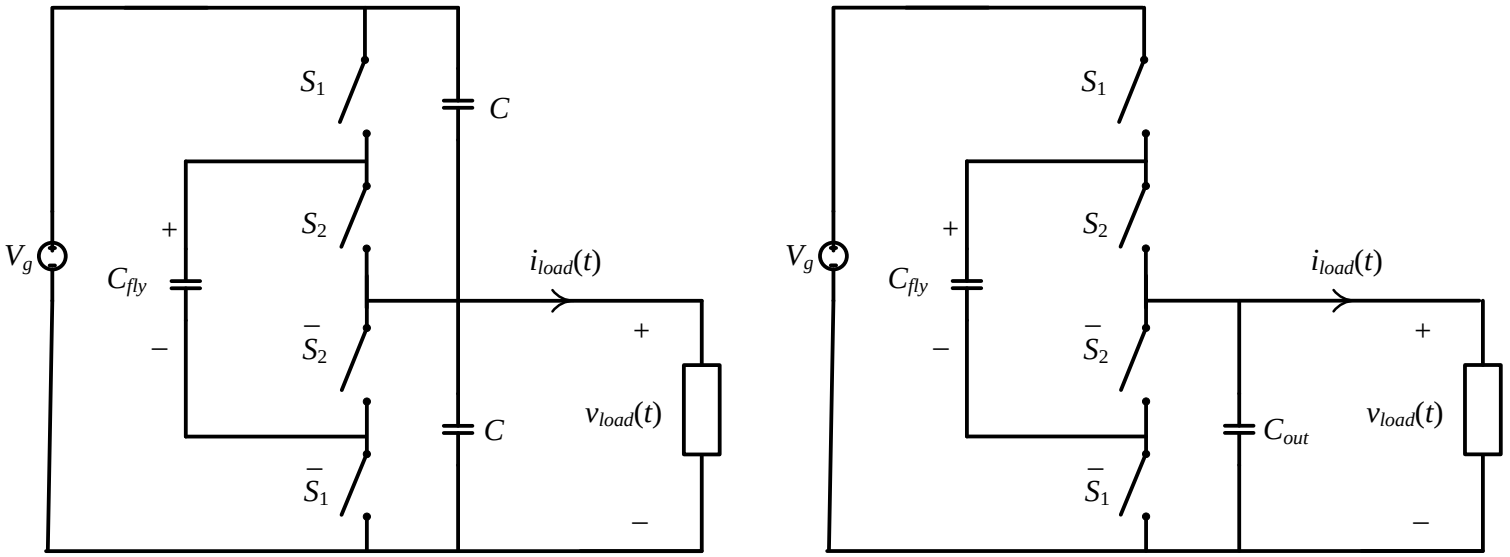




$$i_{fly\_2} = i_{out} + i_2$$

Period 2: The flying capacitor transfers extra charge to the output capacitor

Inductor Elimination: Switched Capacitor Converters



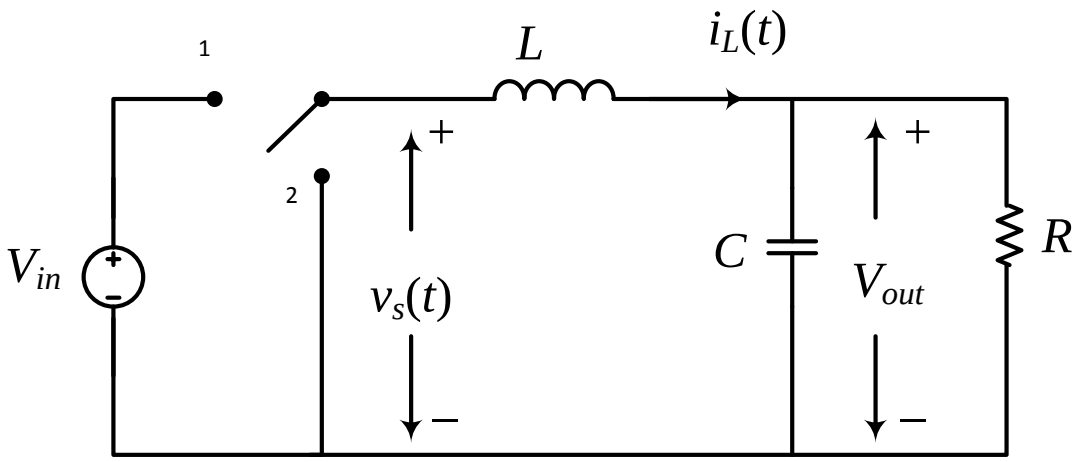
- Very high efficiency at fixed conversion ratios

$$V_{out} = \frac{V_g}{2}$$

- Significant drop at efficiency at other ratios
- Dynamic performance inferior to inductive solution, to make them equally effective with variable conversion ratio variations need extra elements => reduction of savings

Inductor Volt-Swing Reduction

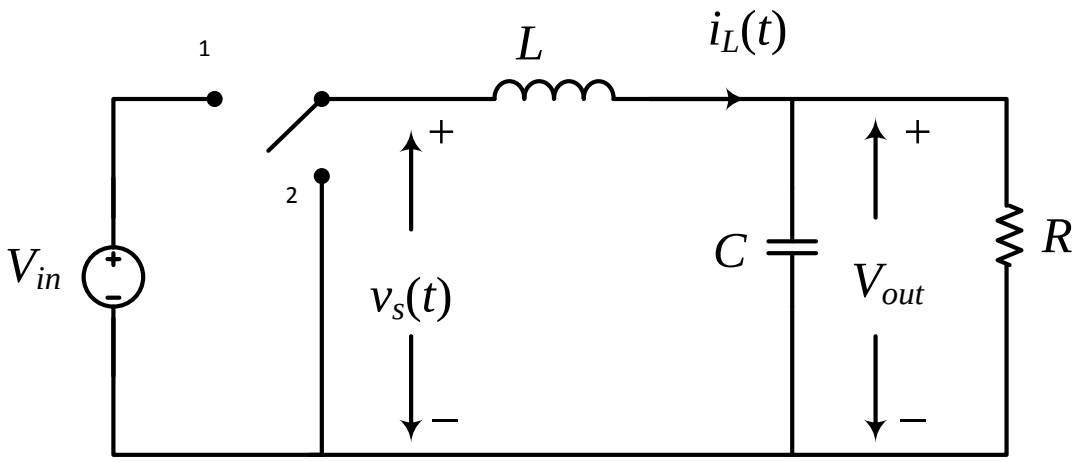
Inductor Voltage Swing and Current Ripple



$$\Delta i_L = \frac{V_{L\_on} D}{2Lf_{sw}} = \frac{V_{L\_off}(1-D)}{2Lf_{sw}}$$

- To reduce ripple (inductor) - high frequency of operation
- Reduction of voltage swing , i.e. DV_{L_on} and $D'V_{L\_off}$ values

Buck Converter Reduction of Inductor Volume



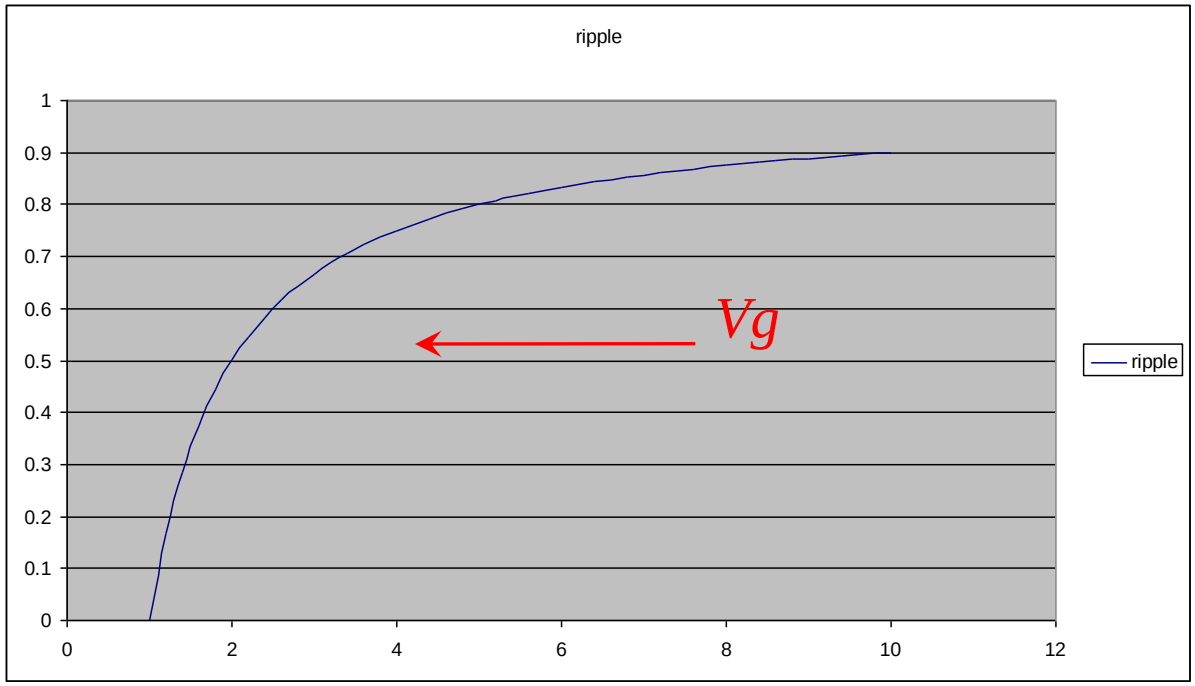
$$\Delta i_L = \frac{(V_g - V_{out}) \cdot DT_{sw}}{2 \cdot L}$$

$$\Rightarrow$$

$$L = \frac{(V_g - V_{out}) DT_{sw}}{2\Delta i_L}$$

Idea: to reduce the input voltage, i.e. bring it closer to the output voltage with a front-end capacitive stage

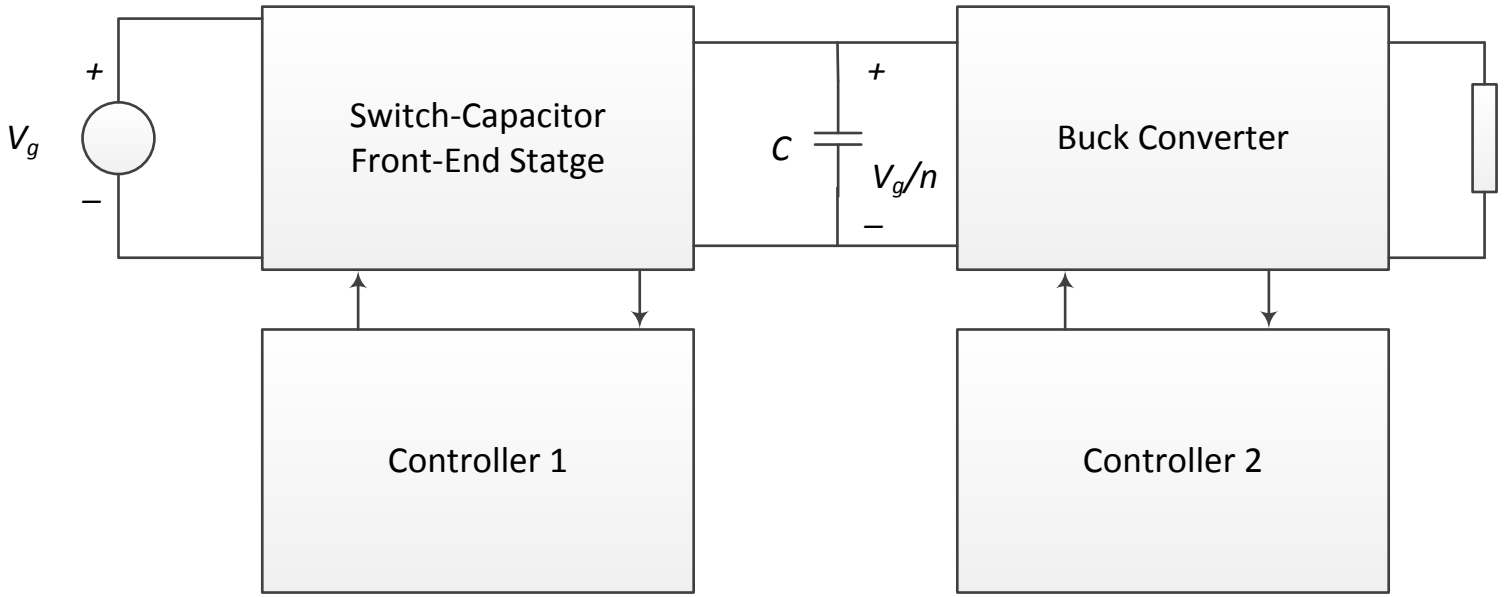
Volt Swing Reduction – Effect on Ripple (Value of L)



$$\Delta i_L = \frac{(V_g - V_{out}) \cdot DT_{sw}}{2 \cdot L}$$

Ripple changes of a 1 V converter for the input voltage variation from 10 V to 1 V. By reducing the voltage swing we can reduce the inductor value.

Conventional Approach: Serial Connection of a Switch Cap Converter And a Converter with Inductor

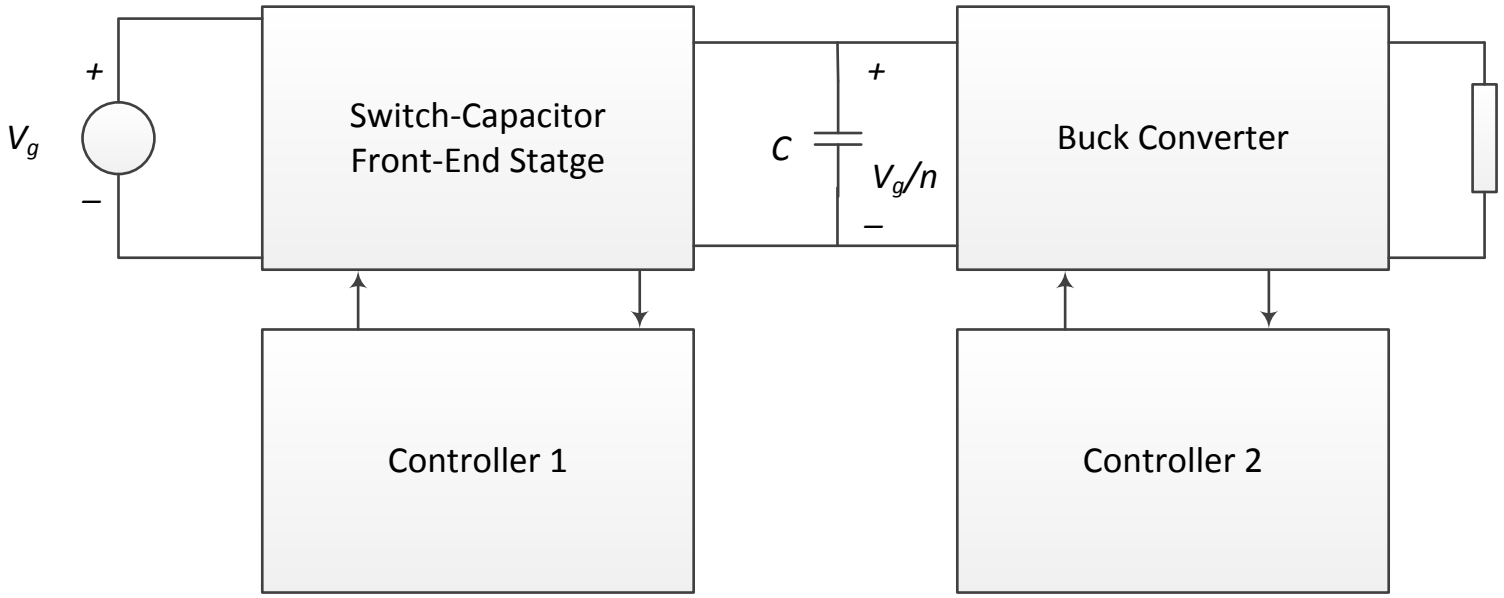


Front stage reduces the input voltage of the buck.

[1] R.C.N.Pilawa-Podgurski,D.M.Giuliano,andD.J.Perreault,"Merged two-stage power converter architecture with soft charging switched- capacitor energy transfer," in Proc. IEEE PESC, 2008.

[2] J. Sun, M. Xu, Y. Ying, and F. C. Lee, "High power density, high efficiency system two-stage power architecture for laptop computers," in Proc. IEEE PESC, Jun. 2006, pp. 1–7.

Common Approach: Serial Connection of a Switch Cap Converter And a Converter with Inductor



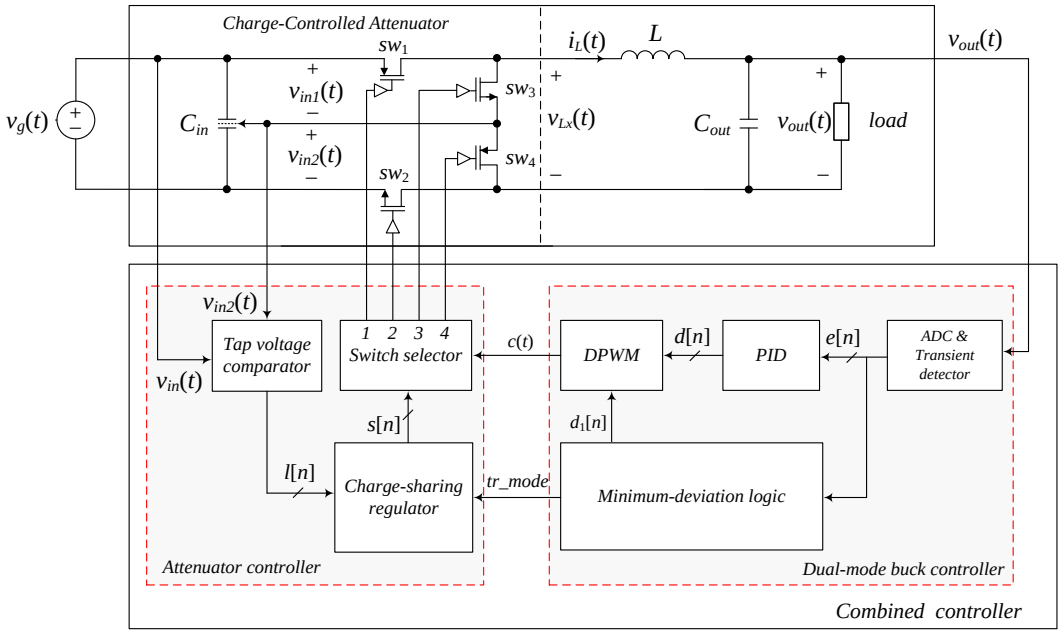
1. Drastic reduction of the output filter volume

1. Relatively large intermediate cap (still smaller favorable tradeoff)

2. Extra switches in conduction path (at least 4) and at least 6 switches total

Buck Converter with Merged Capacitive Attenuator (Hybrid Architecture)

Buck Converter with Merged Capacitive Attenuator



[1] A. Radić, A. Prodić, "Buck Converter With Merged Active Charge-Controlled Capacitive Attenuation," IEEE Transactions on Power Electronics, March 2012,Vol.27, Issue. 3, pp. 1049-1054

-All switches rated at ½ V_{max} of the conventional buck (no extra conduction losses)

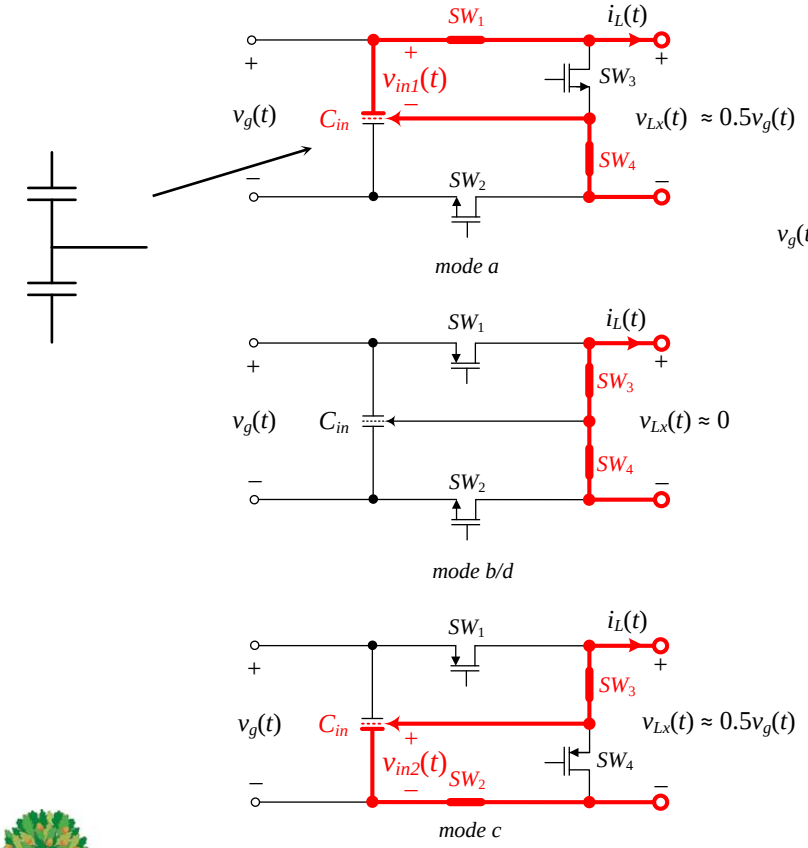
-Switches are shared between the cap stage and buck

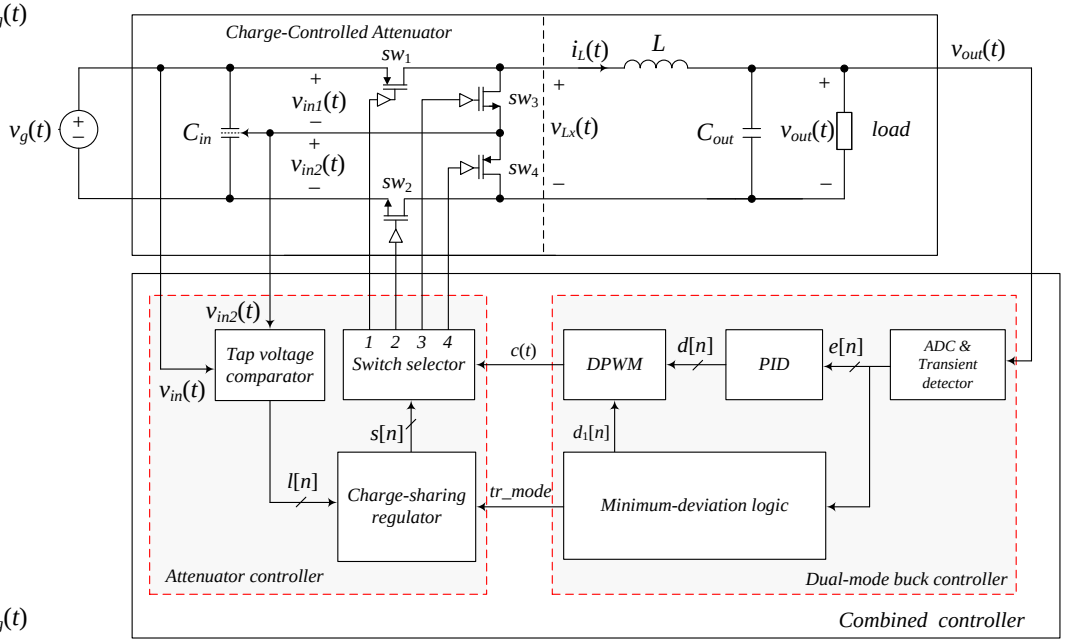
-Lower switching losses than of the conventional buck

-Centre tap voltage maintained constant with the help of buck inductor

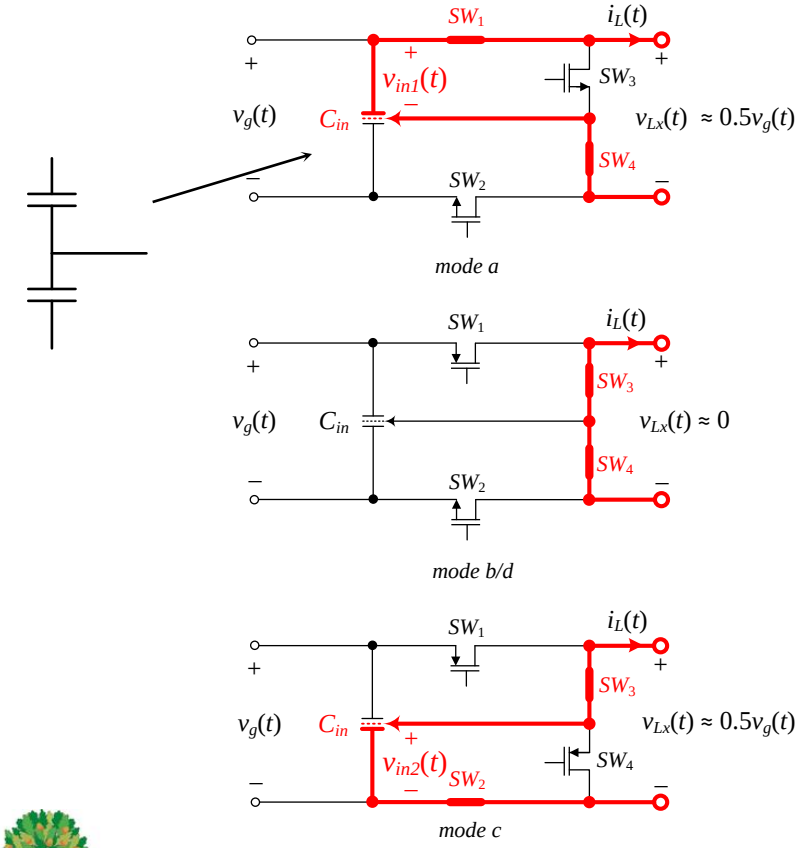
- Better transient response than the time-optimal buck

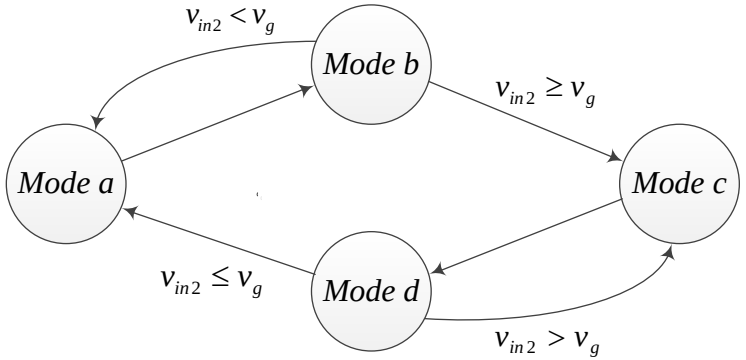
Modes of Operation, Ideal and Practical System





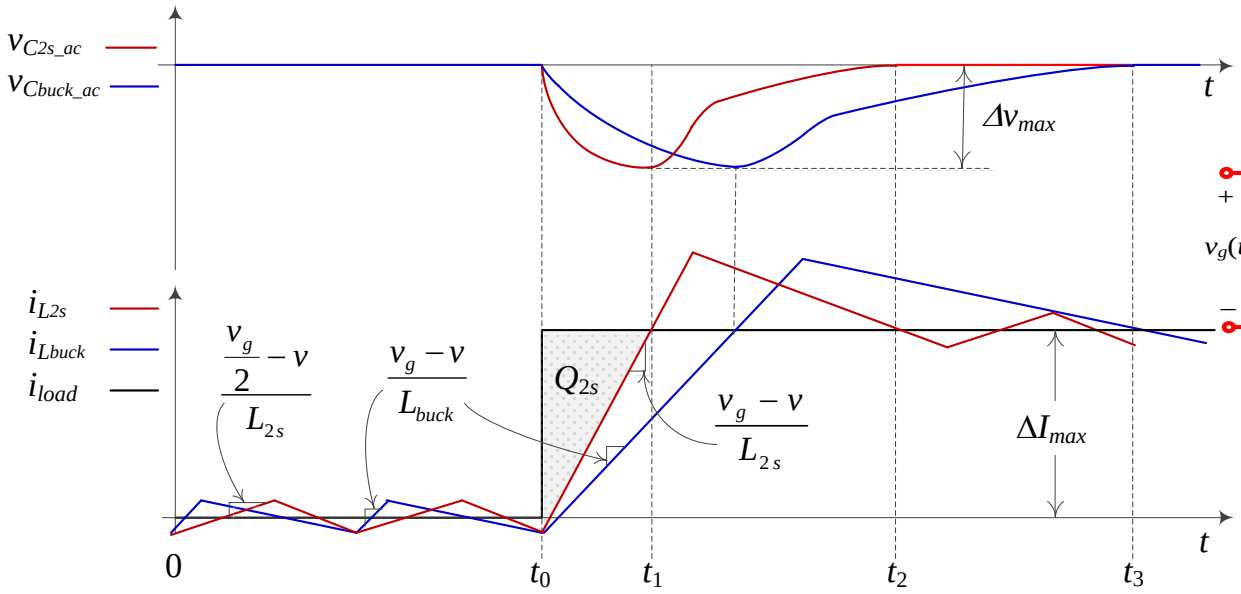
Modes of Operation, Ideal and Practical System

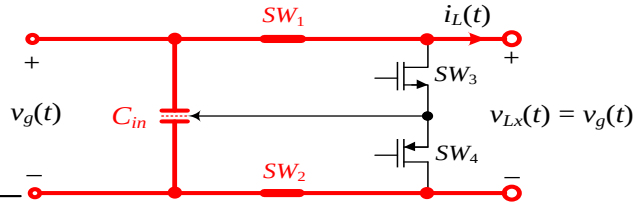




Centre-tap voltage controller operation. Skips regular sequence and takes the charge from the cap with larger voltage until balance is achieved.

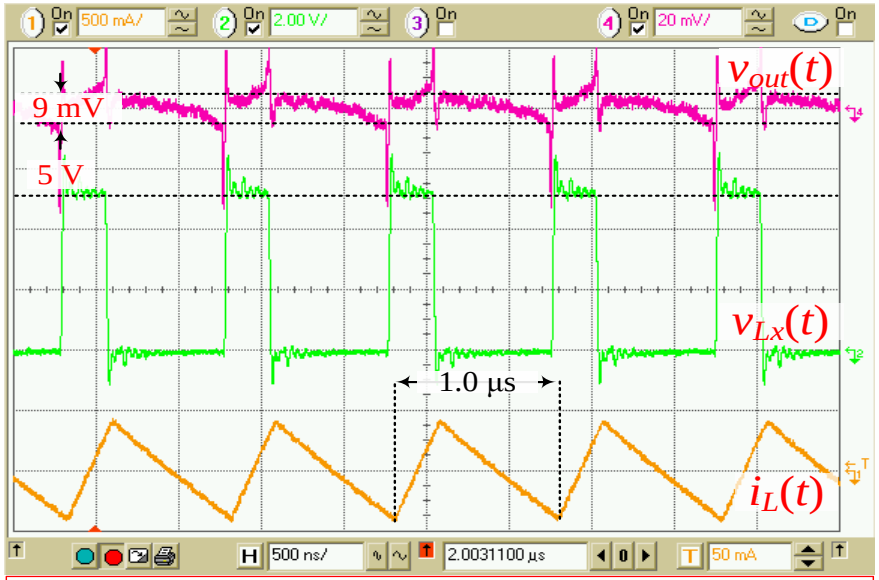
Transient Mode



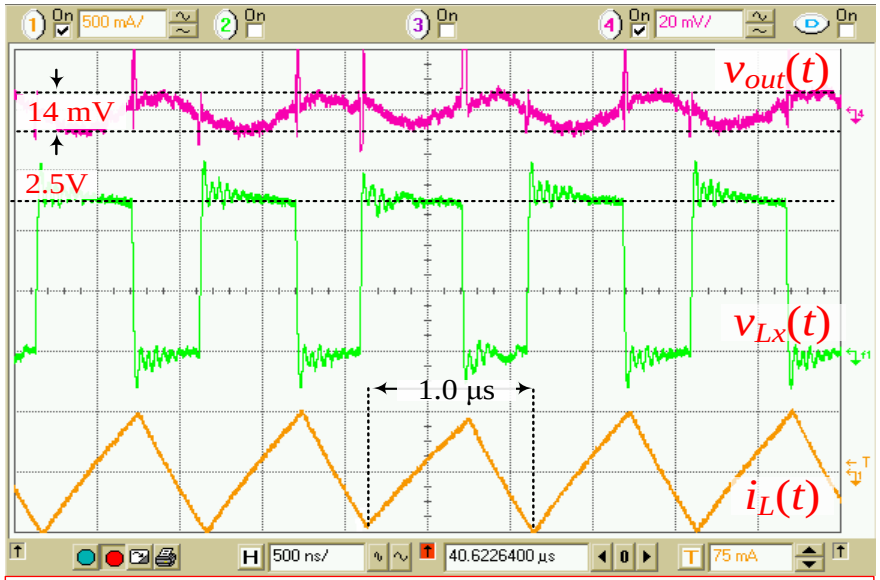


Comparison with a conventional buck

Experimental Results: Comparison with Conv. Buck



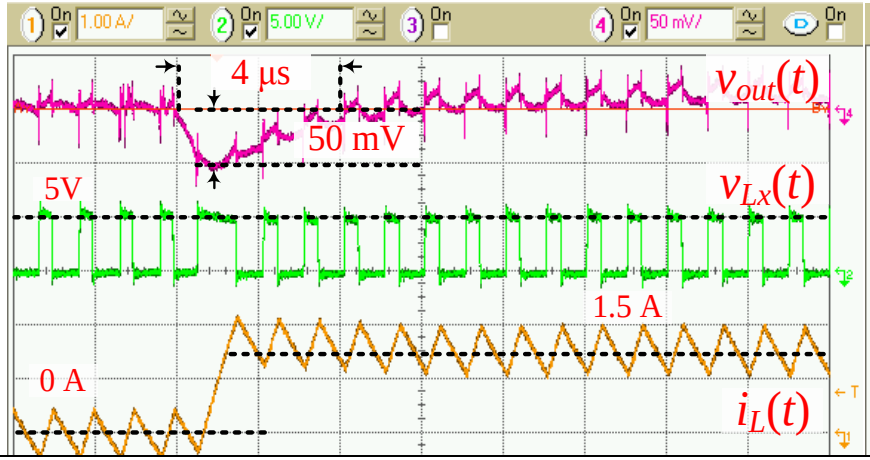
Conventional buck (L=1.0 µH, C=14 µF)

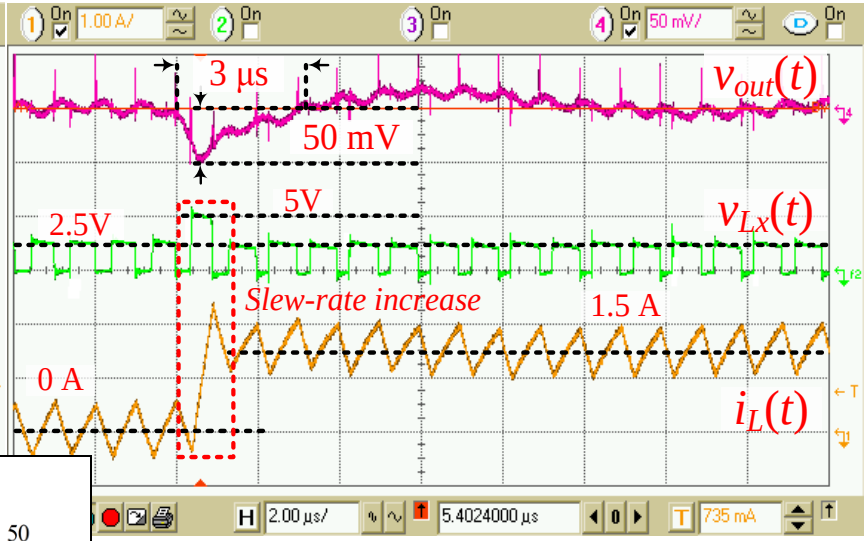


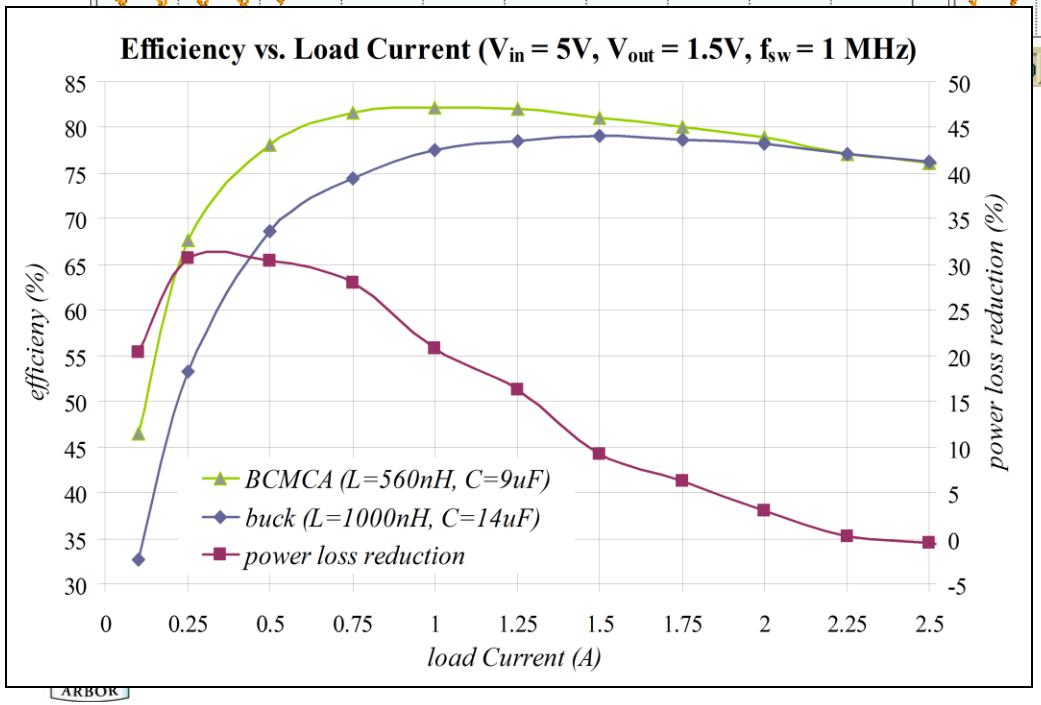
Buck with active charge attenuator (L=560 nH, C=9 µF)

For a 5V to 1 V buck 44% smaller inductor and 35% smaller output capacitor

Experimental Results: Comparison with Con. Buck



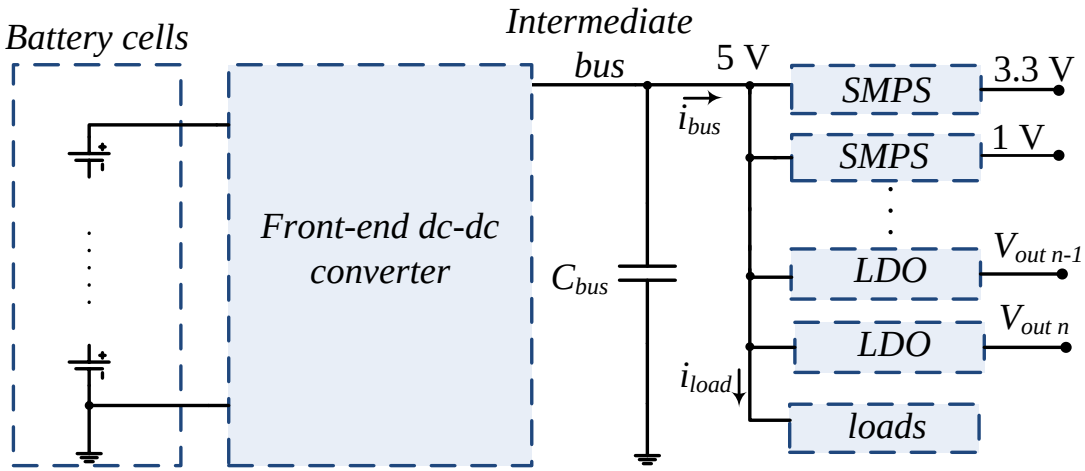




Both transient response and efficiency improved

Power Management System for Portable Applications

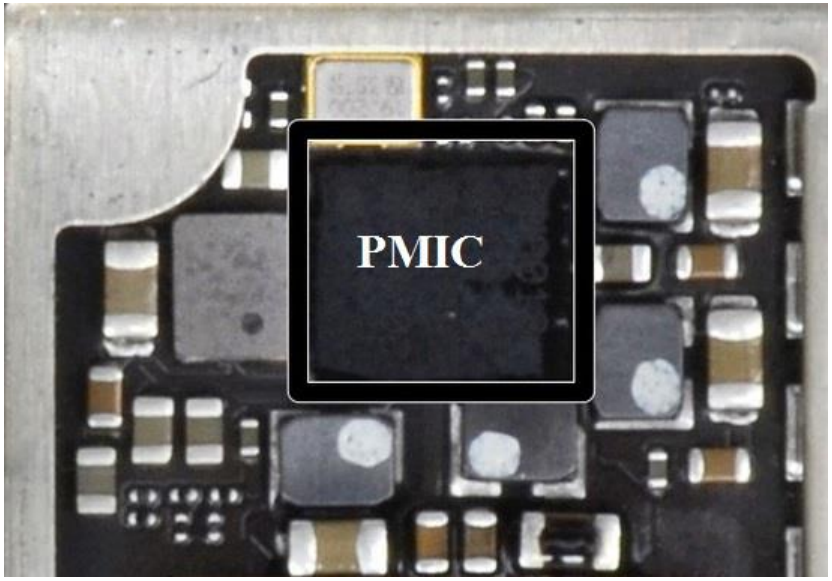
Typical Power Management System of a Portable Device



- Multiple outputs for various loads
- Front end dc-dc stage is bulky
- All SMPS downstream stage operate at a full swing

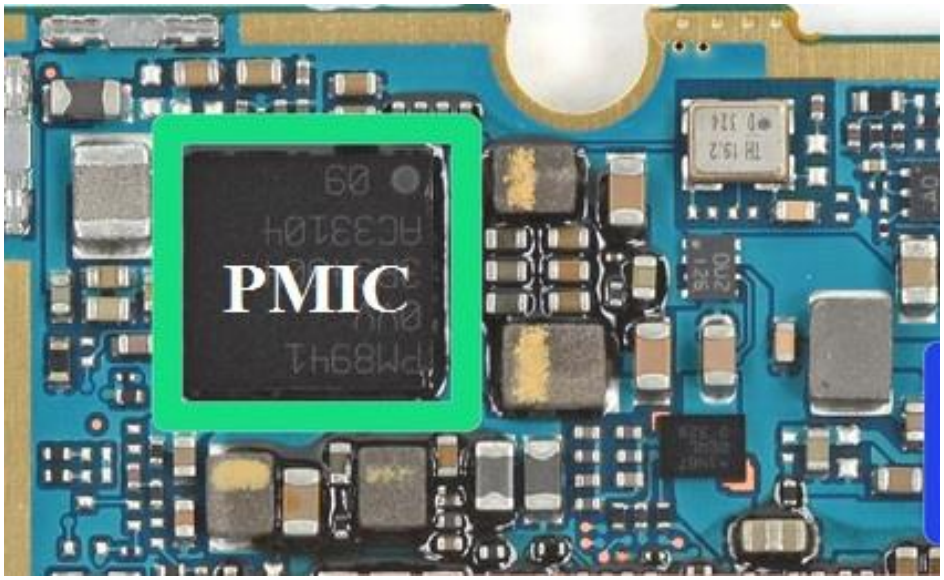
Conventional Power Management System (Goals)

- Inductors consume a large portion of volume of modern portable devices
- We would like to reduce the volume of the inductors



https://www.ifixit.com/Teardown/iPad+Air+Teardown/18907

iPAD Air Tablet

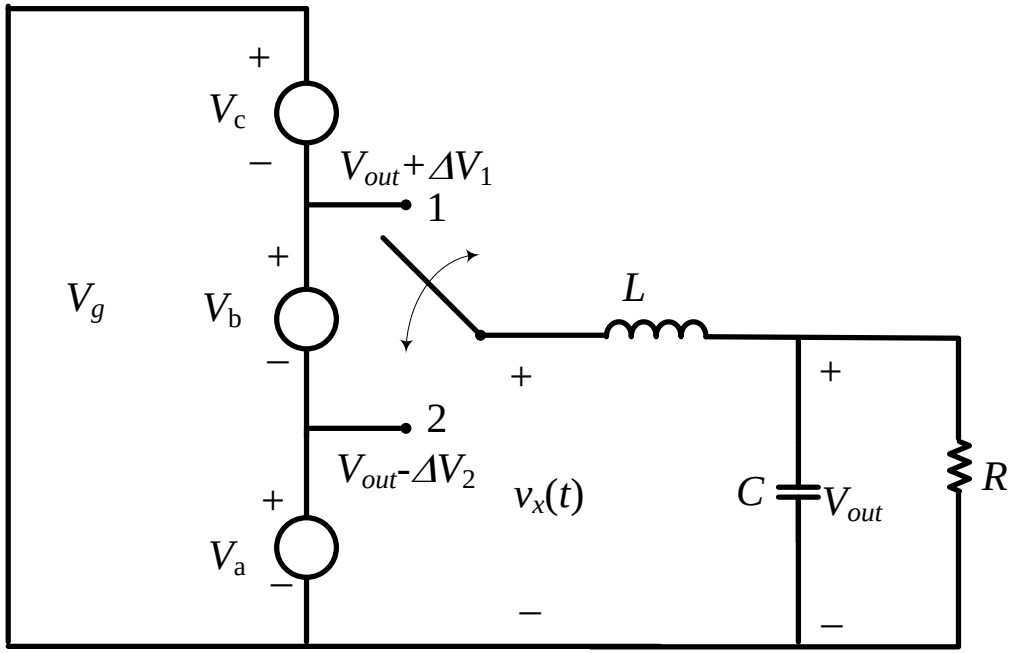


http://https://www.ifixit.com/Teardown/Nexus+5+Teardown/19016

Nexus 5 Smartphone

Revision of Voltage Swing Reduction Concept: General Case

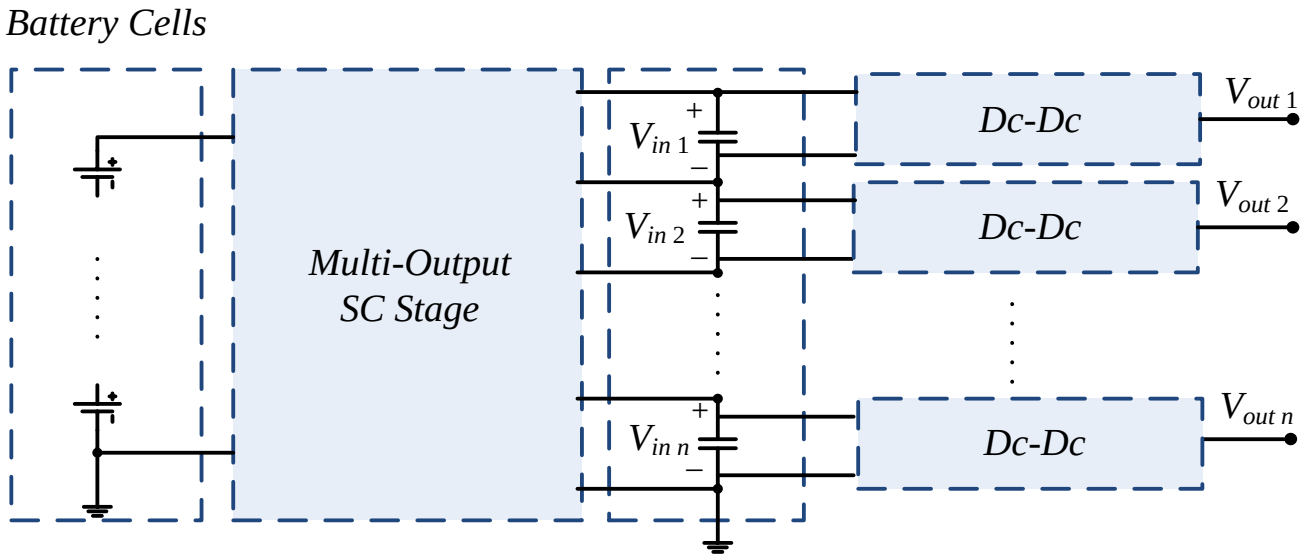
Voltage-Swing Reduction (Differential Buck)



$$\Delta i_L = \frac{V_{L\_1} \cdot D}{2 \cdot L \cdot f_{sw}} = \frac{V_{L\_2} \cdot (1-D)}{2 \cdot L \cdot f_{sw}}$$

Two values of the switch node voltage value can be set close to the output voltage value.

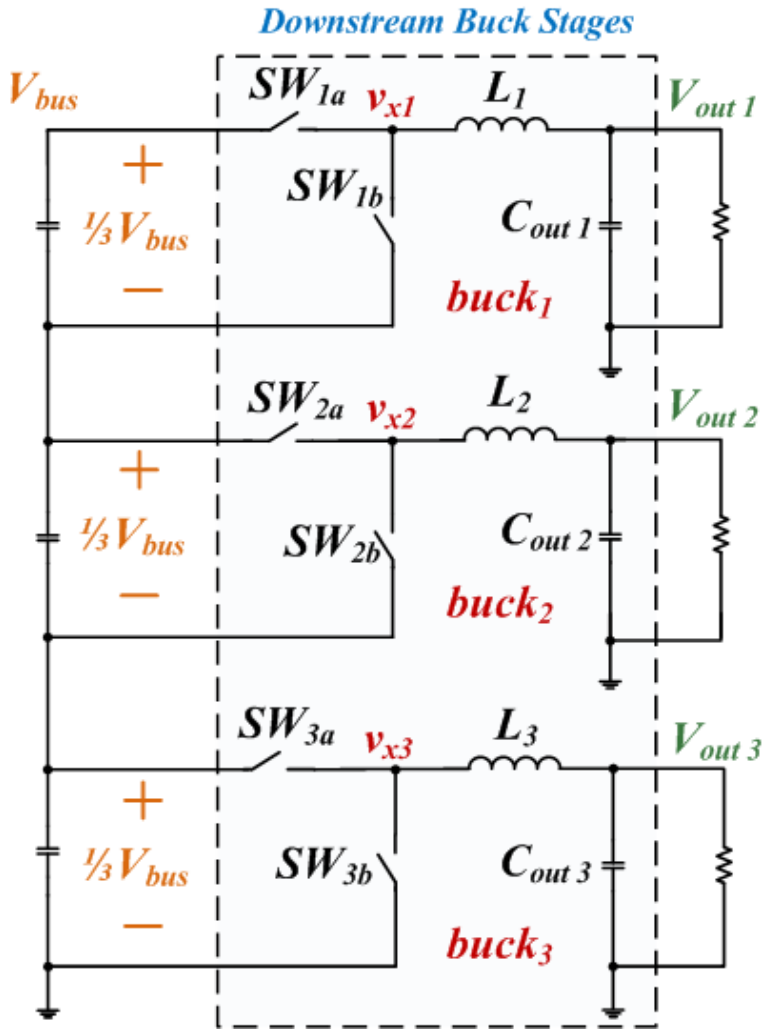
Hybrid SC Based Multi-Output Power Module



- Front end dc-dc stage is open loop SC converter (operating at high efficiency)
- All SMPS downstream stage operate at a swing equal to the corresponding tap capacitor voltage

Principle of Operation: Downstream Stage

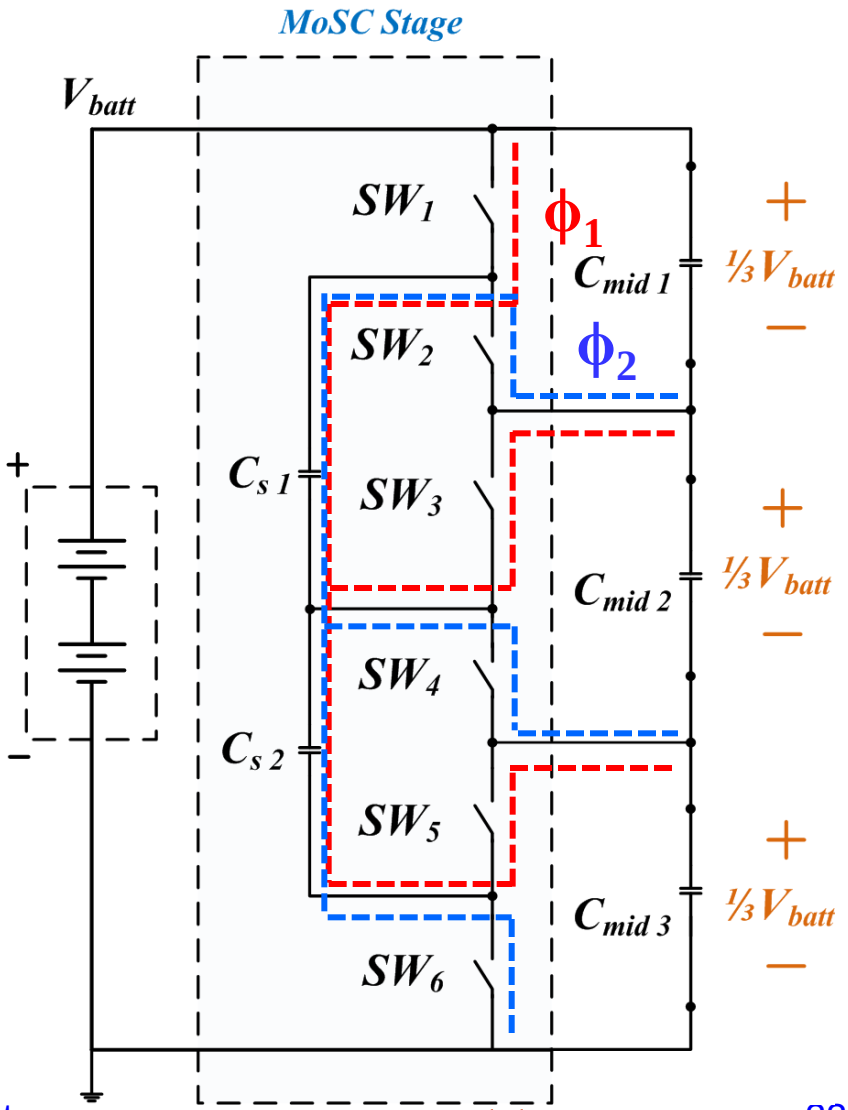
- Reduced voltage swings across inductors reduce the required inductor sizes for same ripple
- Differentially connected buck converters have increased efficiency due to reduced switching losses
- Operating at a higher switching frequency further reduces inductor sizes



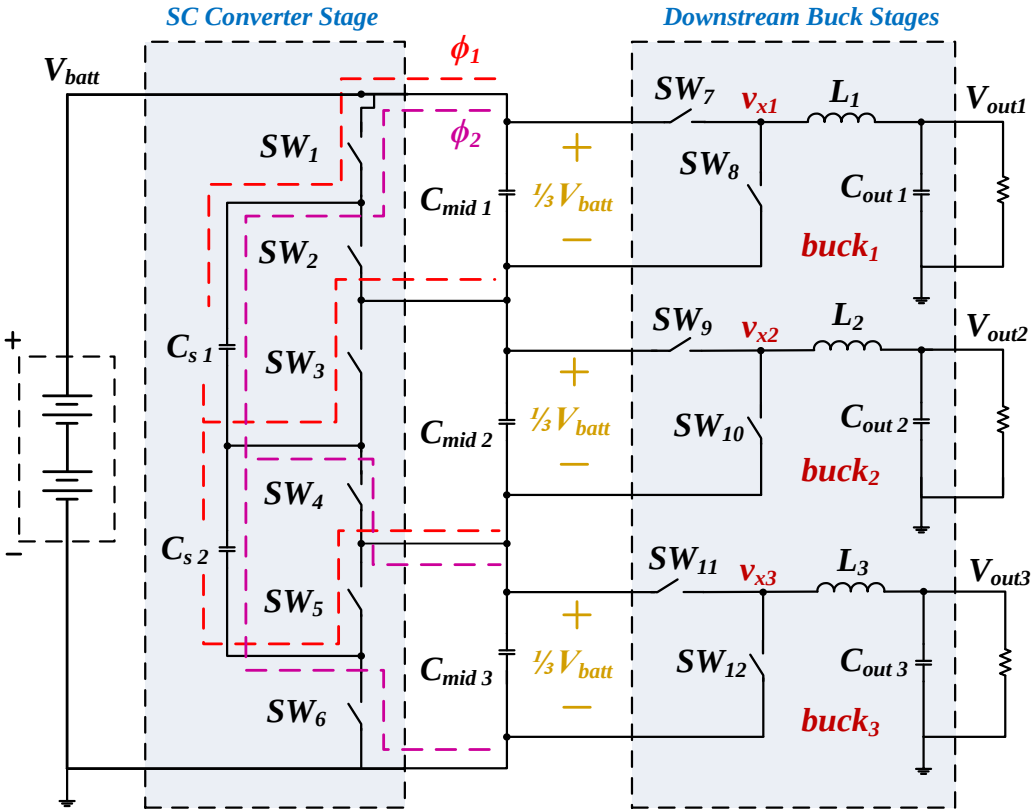
Practical Implementation

Multi-Output SC Front Stage

- Fixed-ratio switched capacitor circuits show high efficiency
- 2 flying capacitors (C_{s1} and C_{s2}) are used with 6 switches with 50% duty ratio
- Each intermediate capacitor (C_{mid1}, C_{mid2}, C_{mid3}) holds 1/3rd of the battery voltage



Hybrid SC Based Multi-Output Power Module

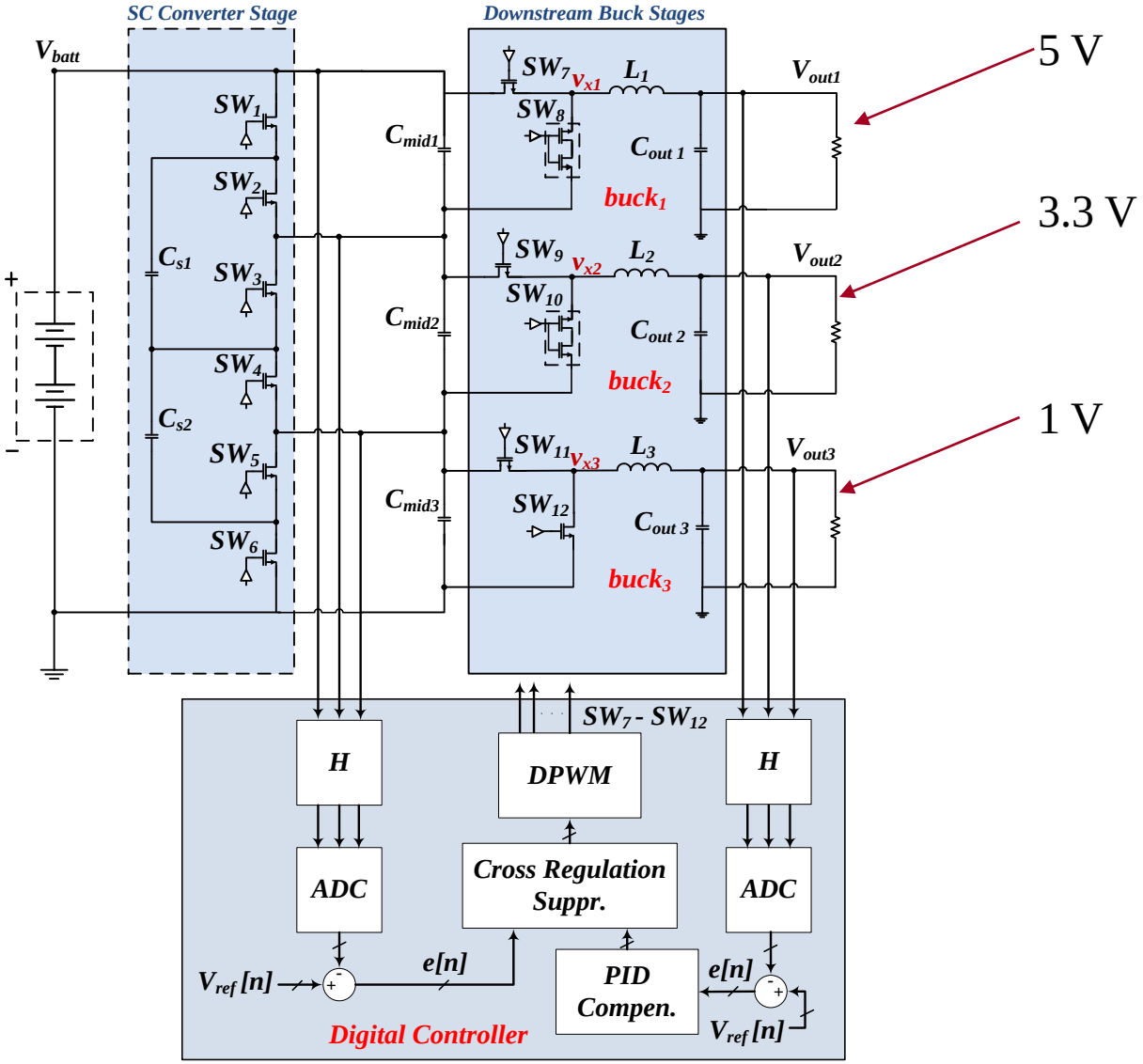


- Triple output front stage combined with differential buck converters

[1] S.M. Ahsanuzzaman, J. Blackman, T. Mcrea and A.Prodić, "A multi-output low-volume power management module for portable battery-powered applications," in Proc. IEEE Applied Power Electronics Conference (APEC), 2013

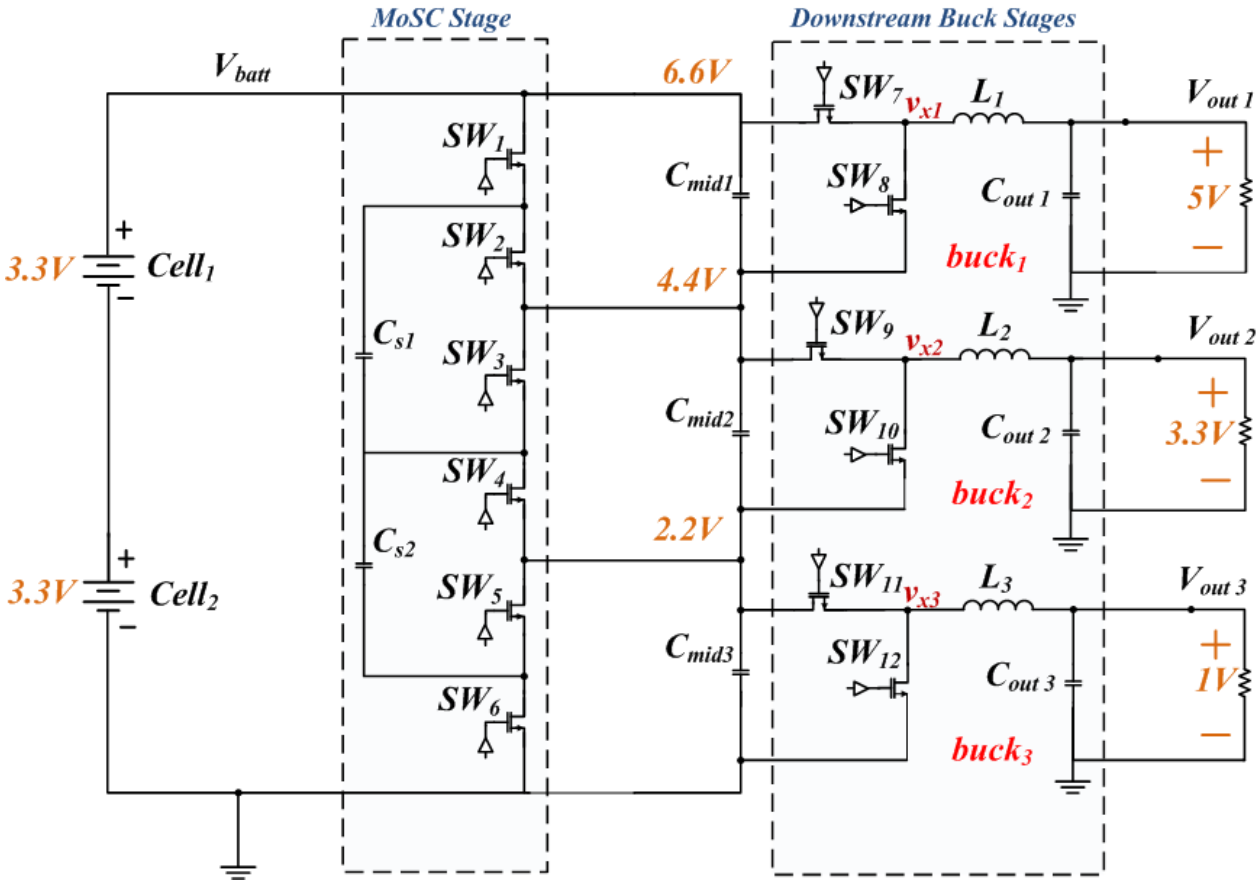
Implementation

2-cell battery pack
(5.4 V to 6.6 V)

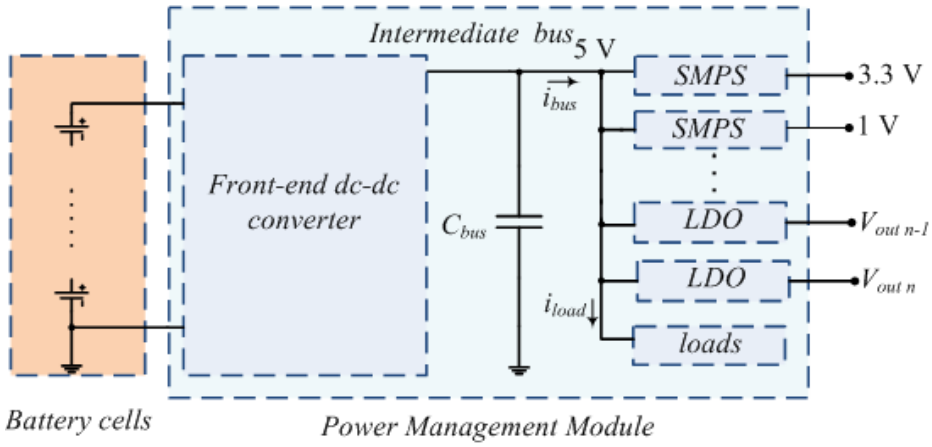


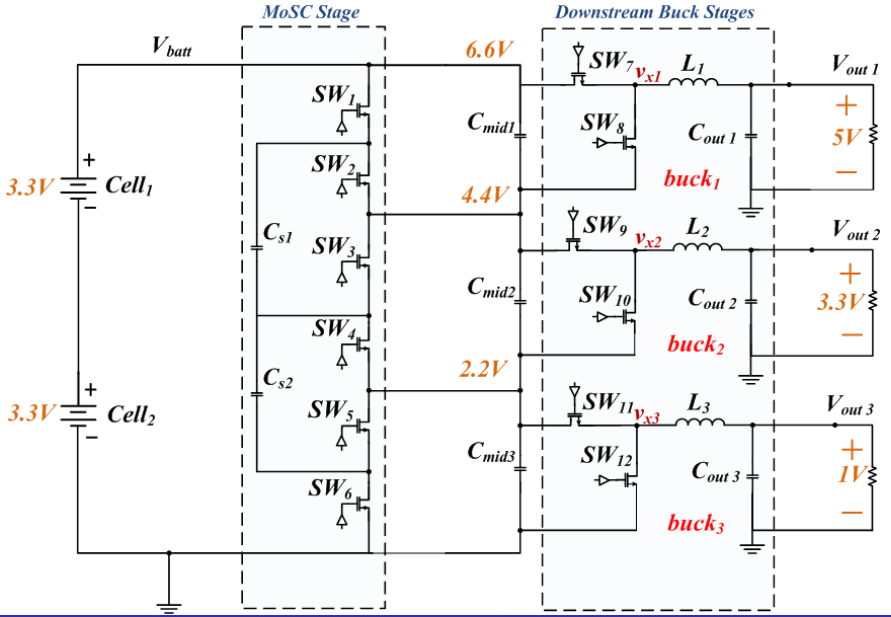
Typical Application

- 1 V output: Digital processors
- 3.3 V output: analog components (i.e. power amplifiers)
- 5 V output: USB ports and peripherals



Comparison Table (Inductor Volumes and Losses)

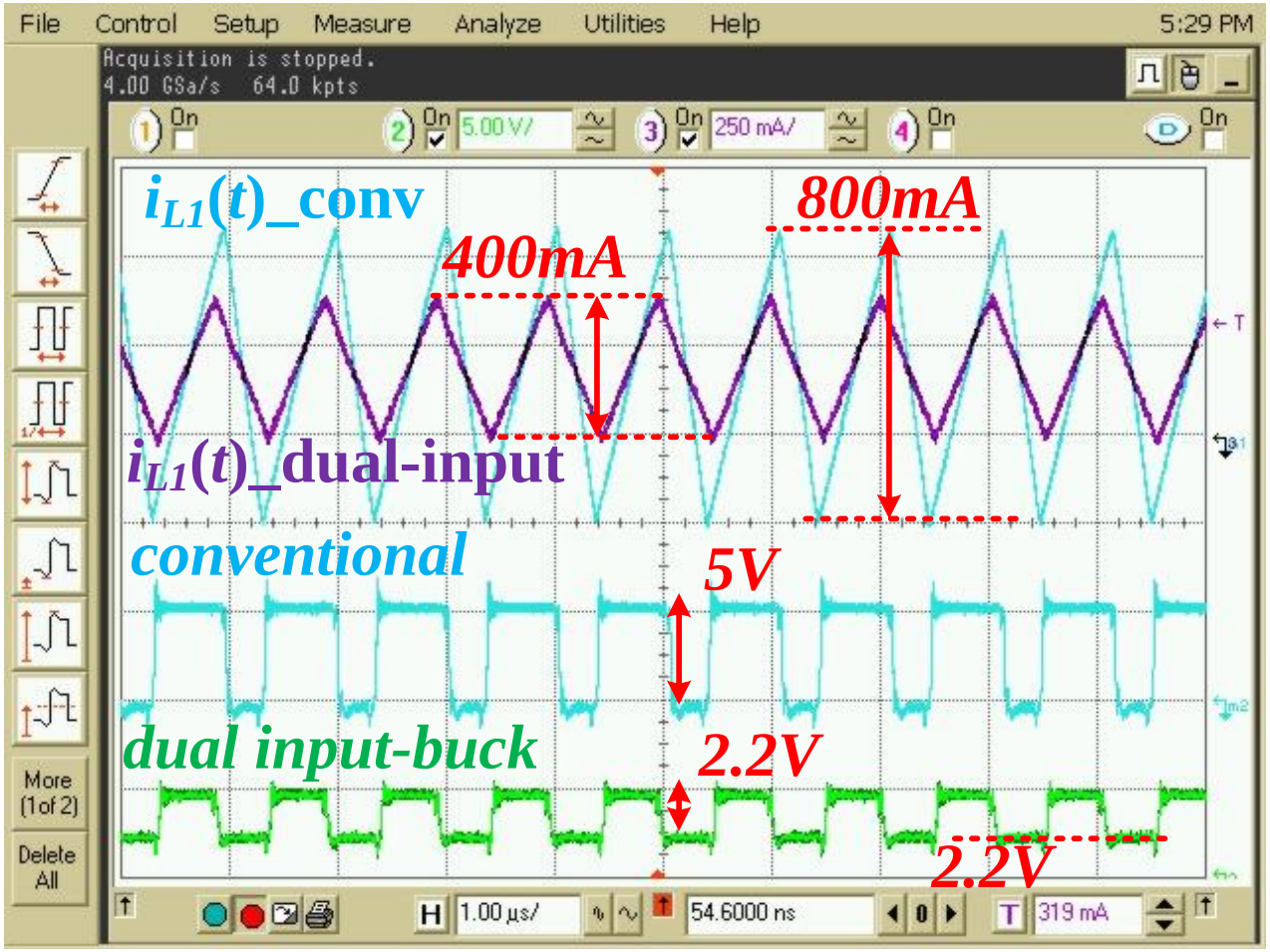




Values in the table are normalized with respect to the conventional architecture (left fig)

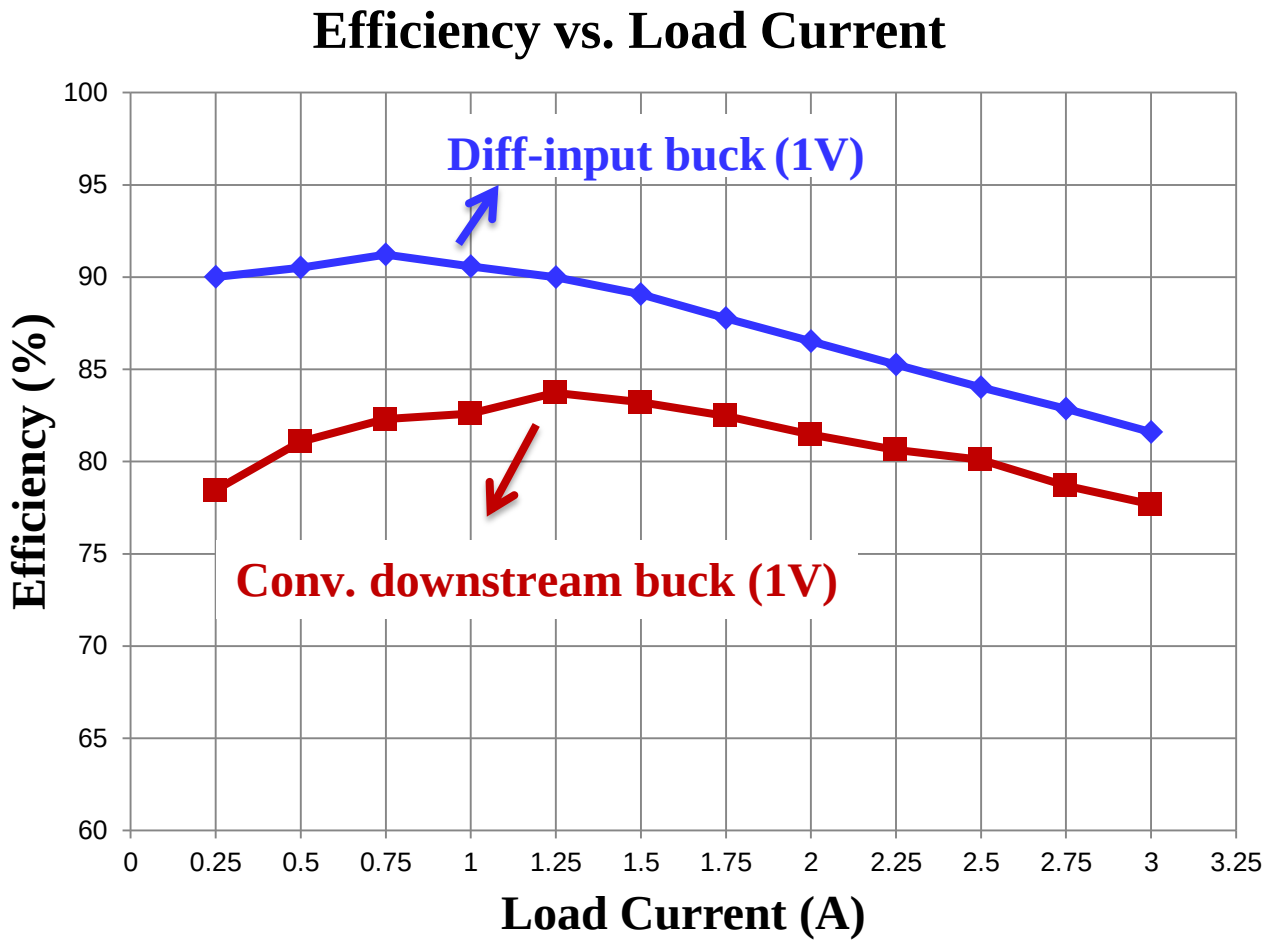
	V_{sw_norm}	$L_{\_norm}$	P_{sw_norm}	f_{sw_norm}
Diff-input buck 3.3 V	0.44	0.49	0.44	1
Diff-input buck 1 V	0.44	0.68	0.44	1
Diff-input buck 3.3 V (incr. f_{sw})	0.44	0.25	0.88	2
Diff-input buck 1 V (incr. f_{sw})	0.44	0.34	0.88	2

Volume Reduction



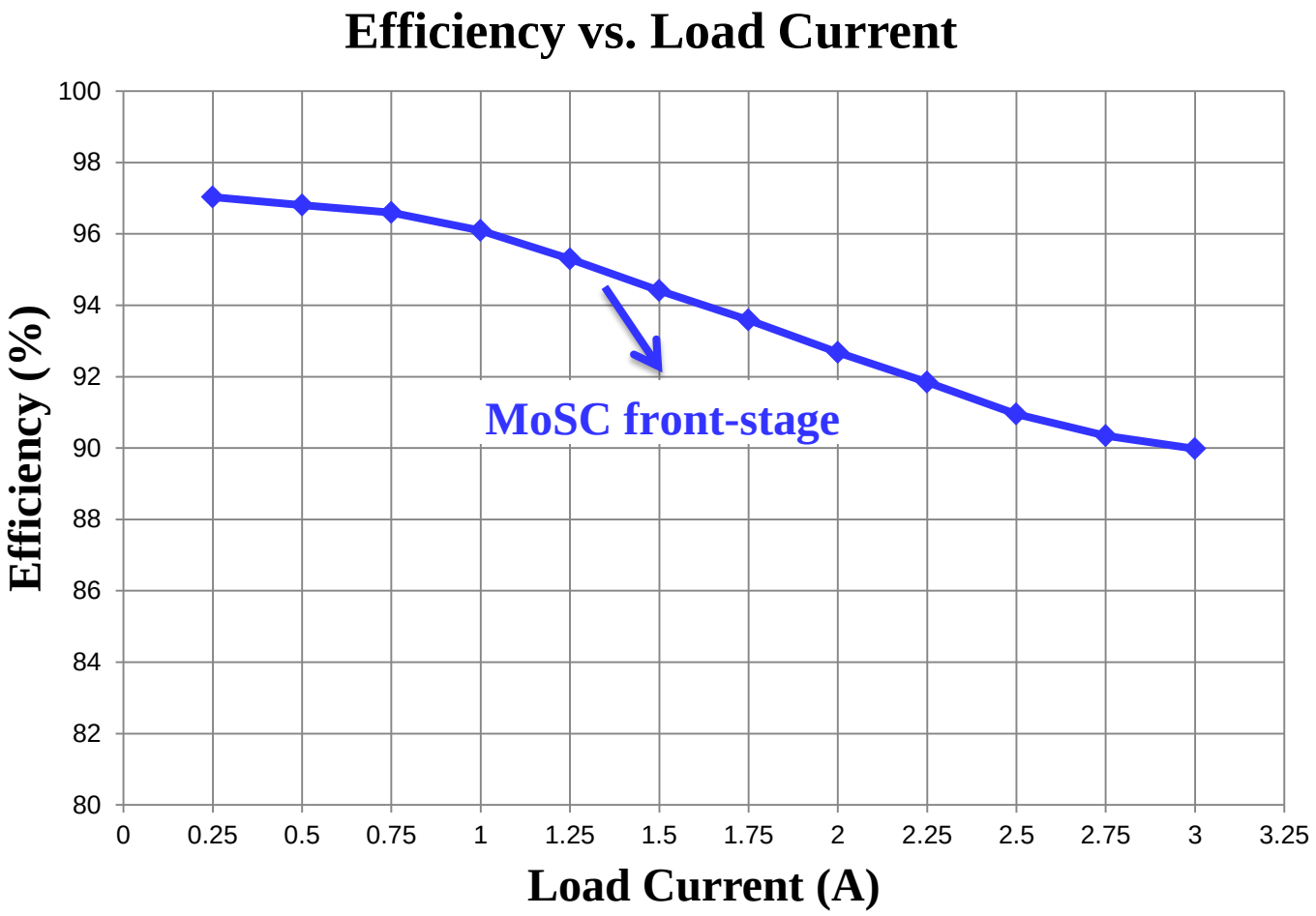
Measured Efficiency Comparison

- 1 V buck converter: 12% improvement at lighter loads



Measured System Efficiency

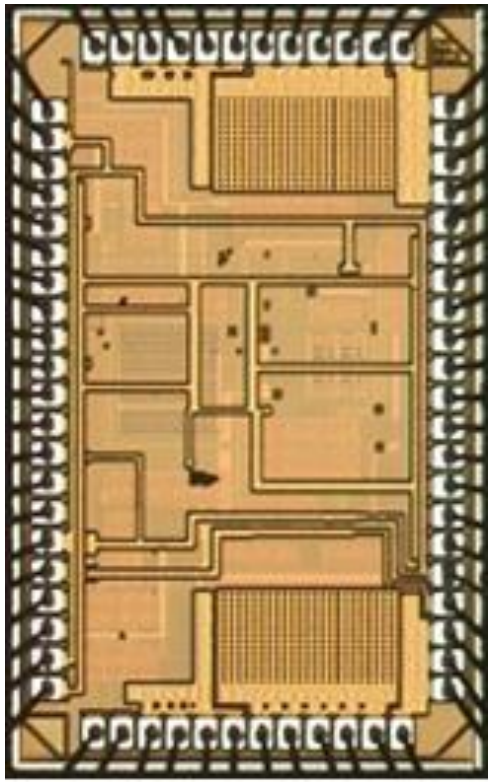
- MoSC front-end stage shows above 90% operating efficiency



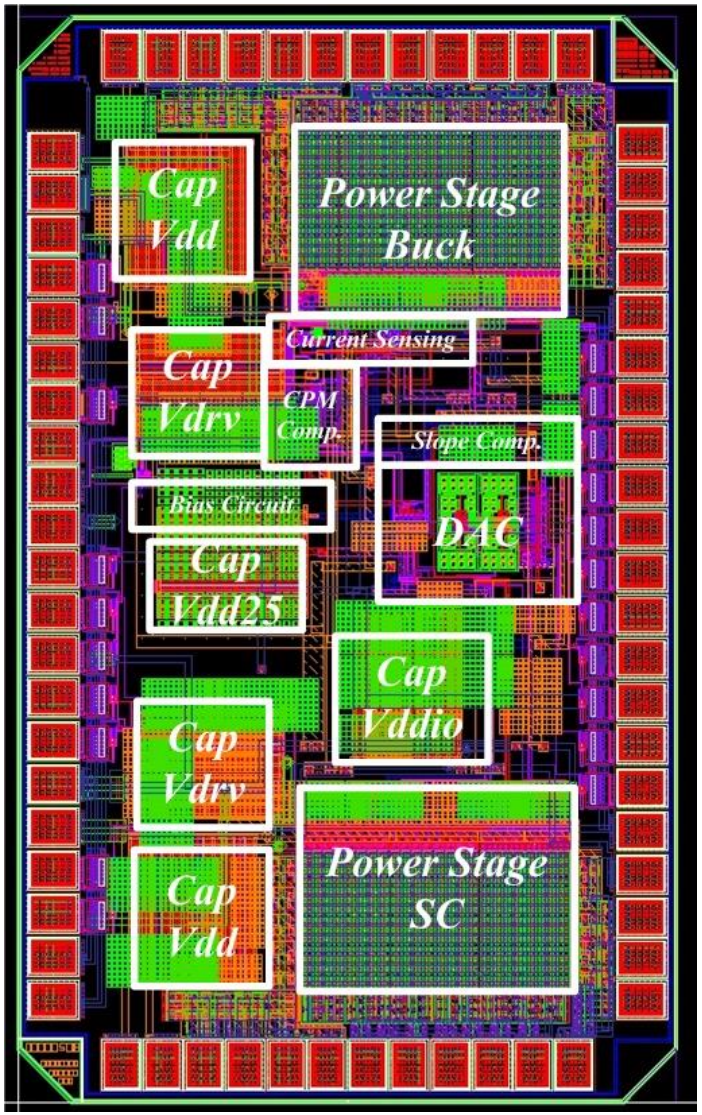
On-Chip Implementation Power Management IC Module

Test Chip (IC-SCB)

- Total Area: 1.5 mm X 2.5 mm



Die Photo

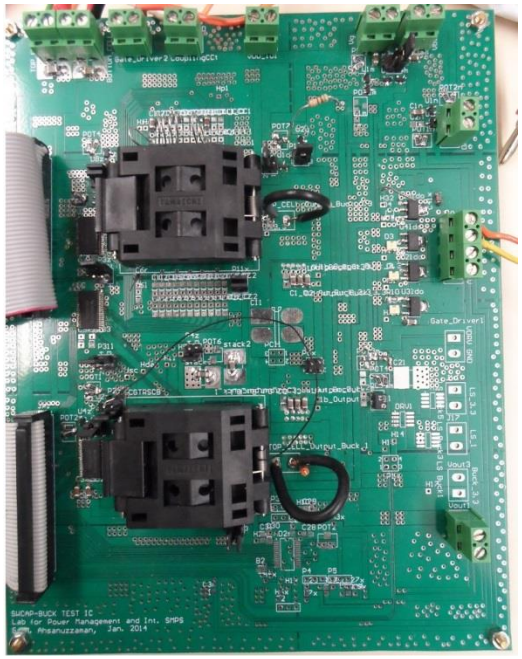


IC Layout

Experimental Setups

- 2 stacked IC-SCBs are tested for the proper system operation

Specifications	Value	Units
f_{sw_sc}	580	KHz
f_{sw_buck}	10	MHz
V_{in}	3	V
V_{out1}, V_{out2}	1, 2.5	V
Buck L,C	100, 10	nH, µF
R_{on} *Pmos, Nmos*	150, 125	mΩ



Test Board #1

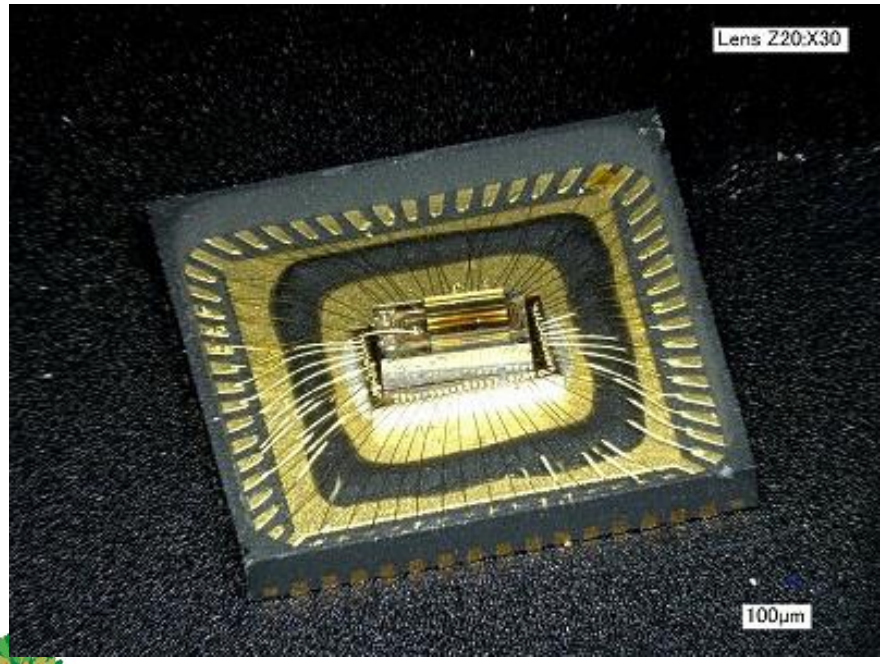
(discrete inductors)

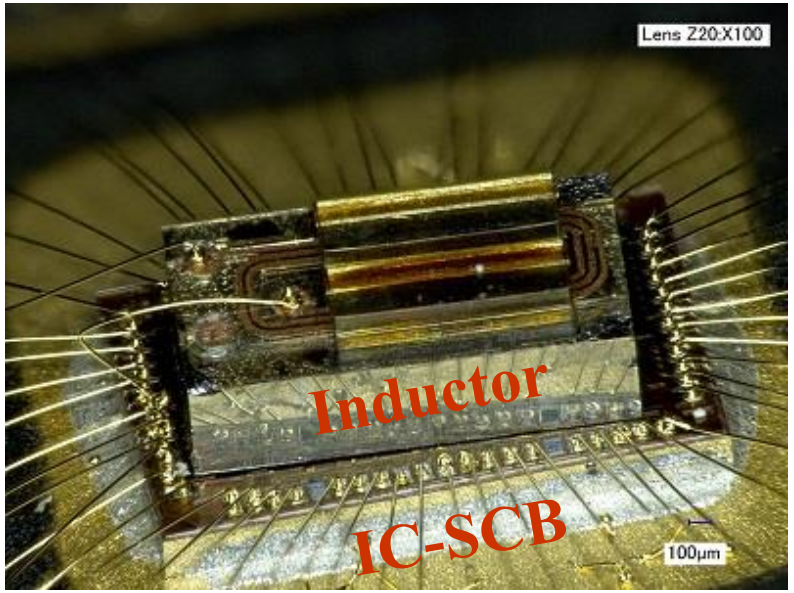
Test Board #2

(on-chip inductors)

IC Packaging with Inductors

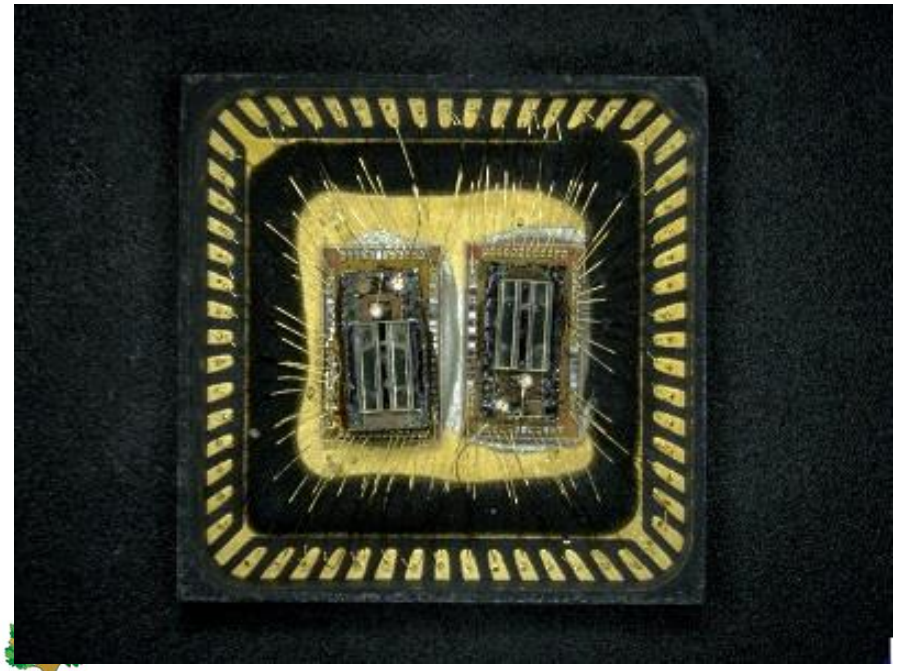
- Bonding picture: 1-IC
  - 60 QFN Package: 7mm X 7mm
  - Inductor (0603) is placed on top of the IC

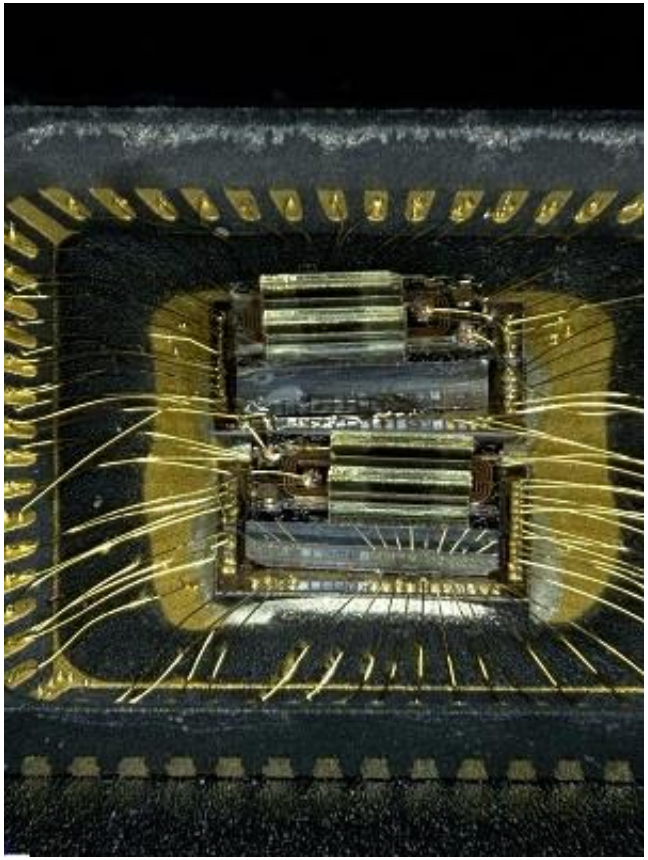




IC Packaging with Inductors

- Bonding picture: 2-ICs
  - 60 QFN Package: 7mm X 7mm
  - Inductors (0603) are placed on top of the ICs

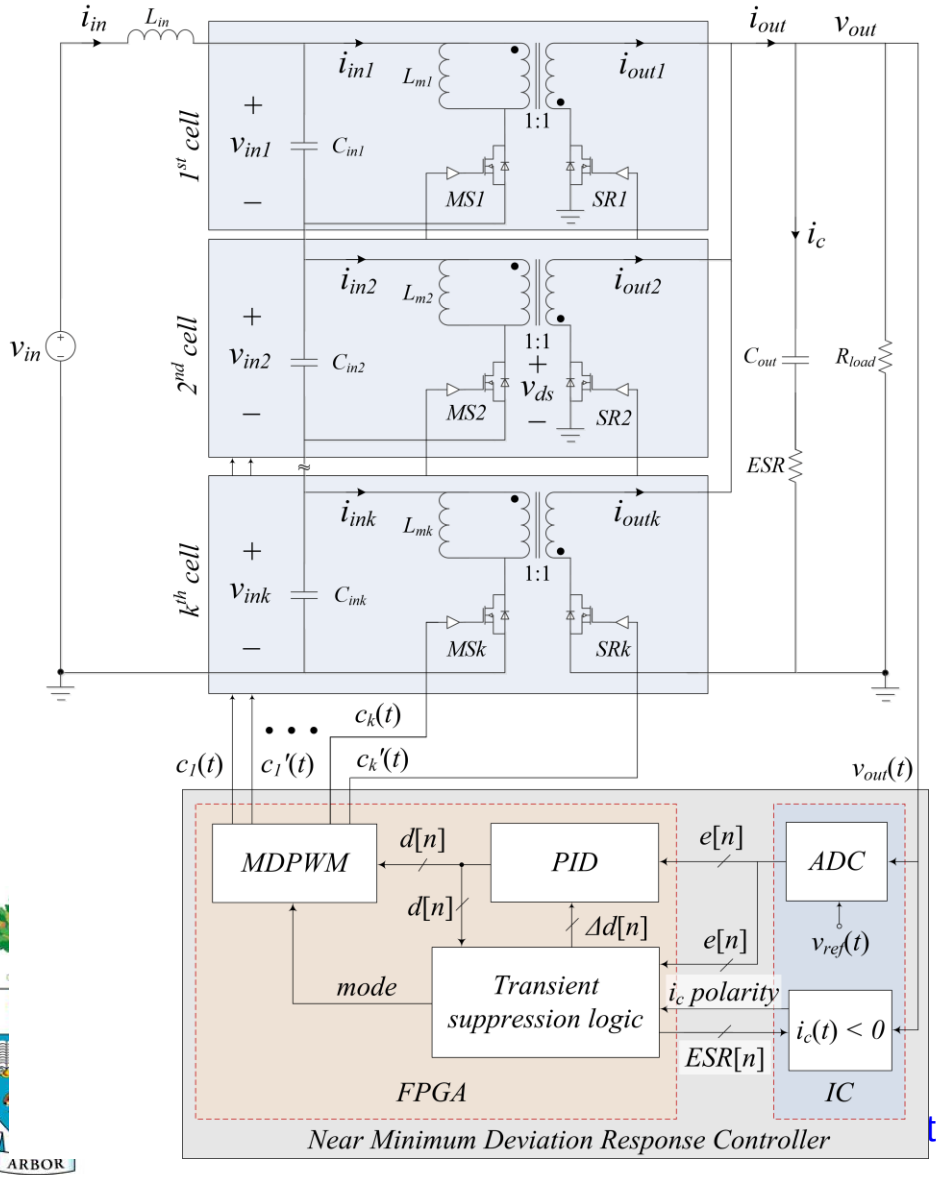




Zoomed

Design Example: Serial Input Parallel Output Flyback (Current Division + Swing Reduction + Optimal Control)

Serial Input Parallel Output Flyback



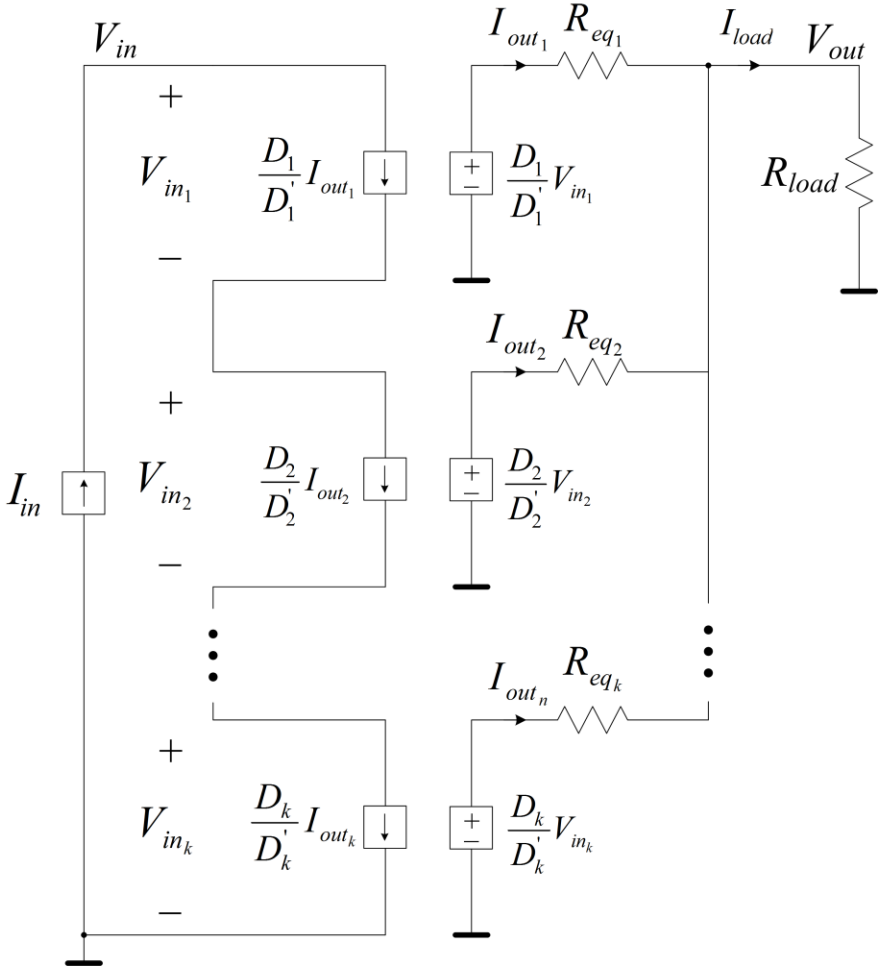
-Load current is shared between the phases

-Voltage swing of the inductors reduces with number of phases

-Near optimum deviation controller

[1] A. Radic, A. Straka, A. Prodic, "Low-volume stackable flyback with near-optimum controller," in Proc. IEEE APEC 2014.

Serial Input Parallel Output Flyback: Equivalent Circuit



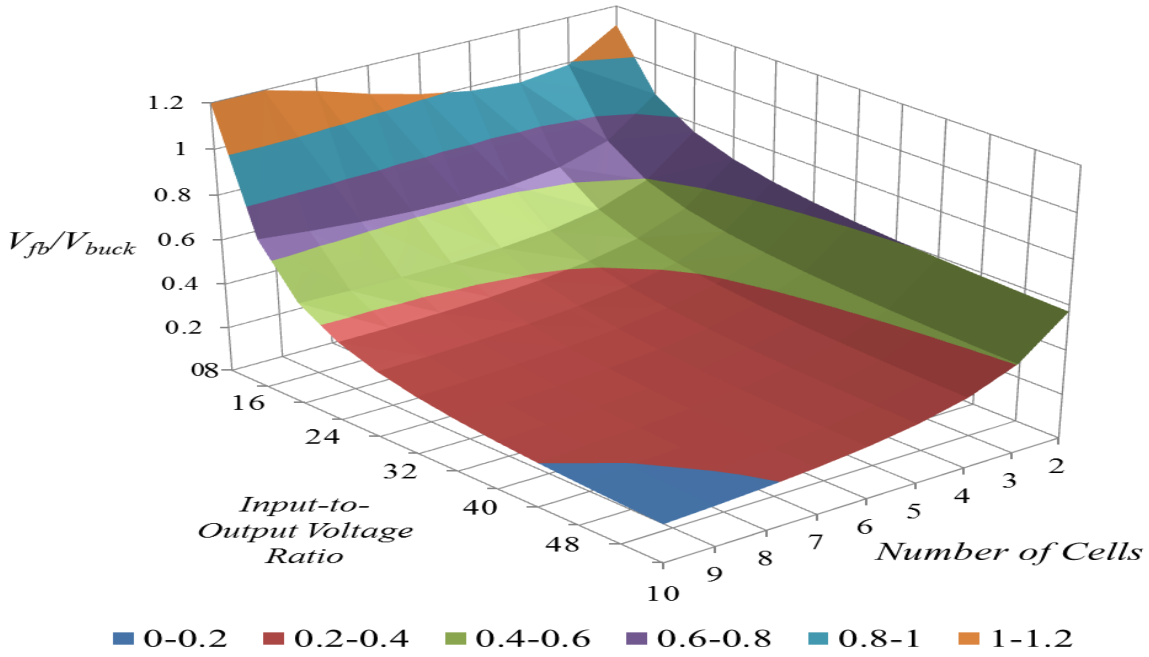
-This equivalent circuit shows that both current and voltage are shared between the phases

- $1/(k^2)$ reduction of power processing requirement per phase

- Inherent current sharing between phases (no need for extra hardware)

- Voltage balancing might be needed but that is less complex to implement

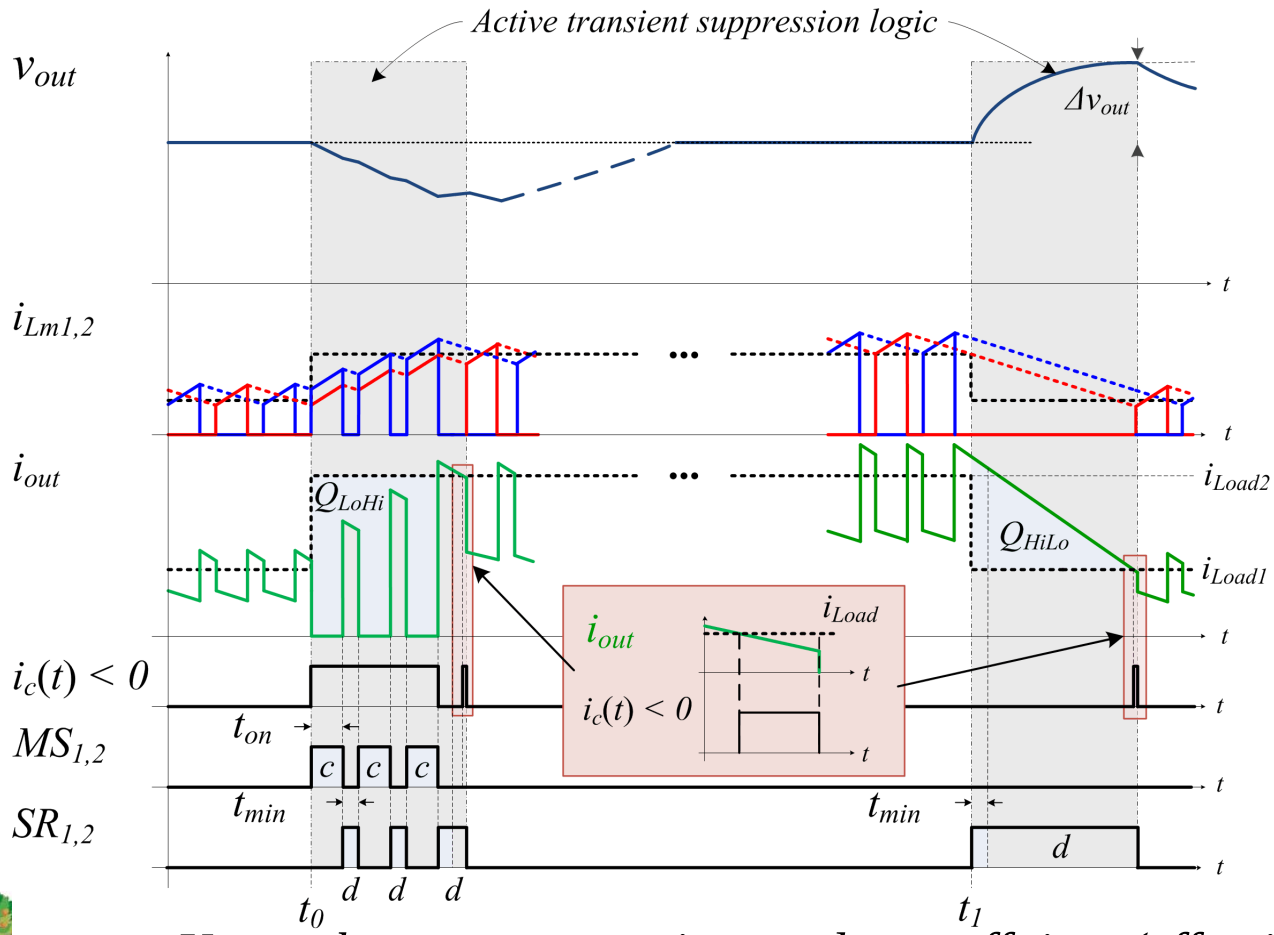
Volume Comparison vs. Interleaved Buck



-For step down ratios larger than 8 2-module flyback is already smaller than an equivalent interleaved buck. For large number of modules the advantage increases.

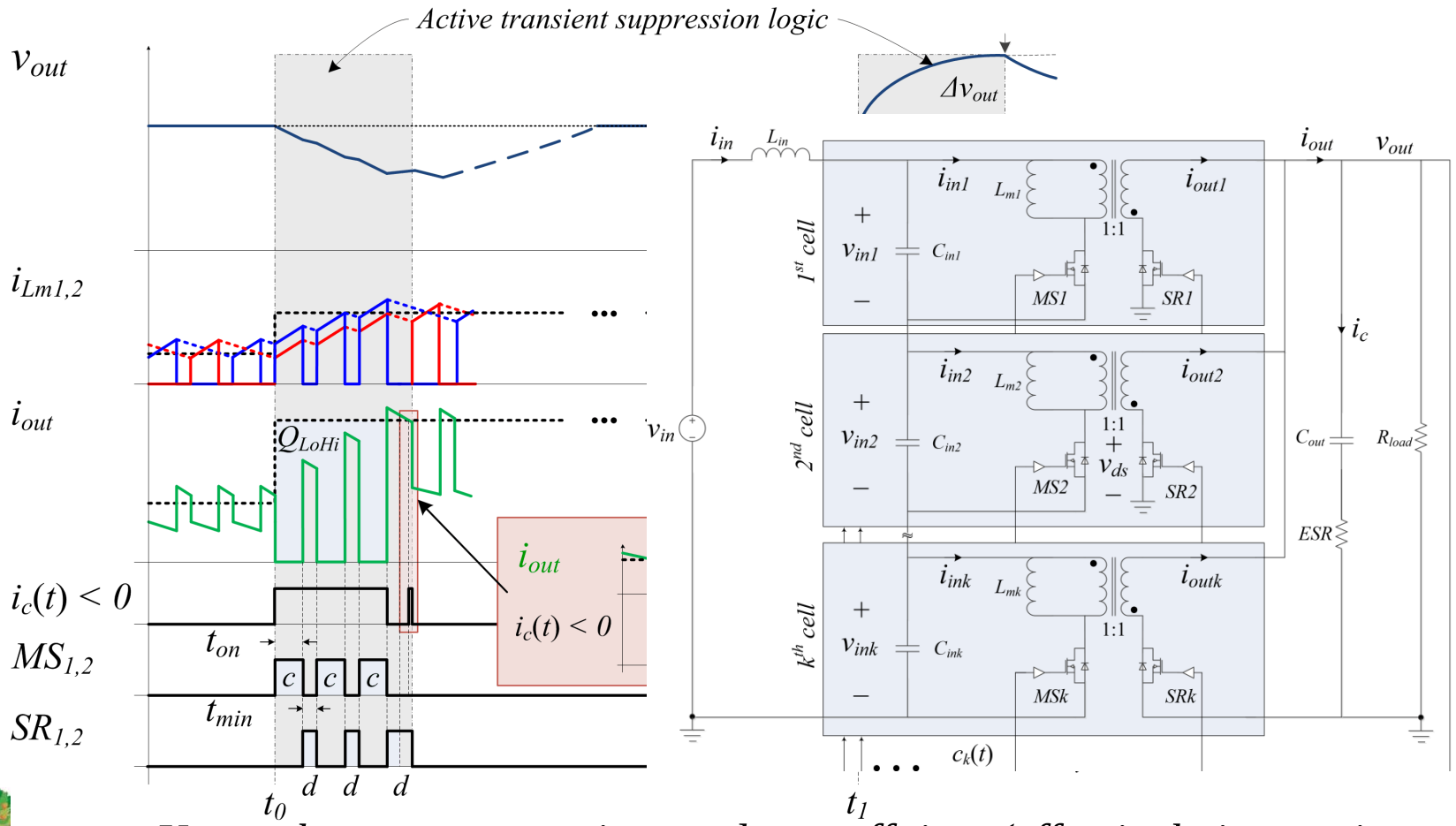
- Advantages recognized but the control is challenge, indirect energy transfer converter

Near Minimum Deviation Controller



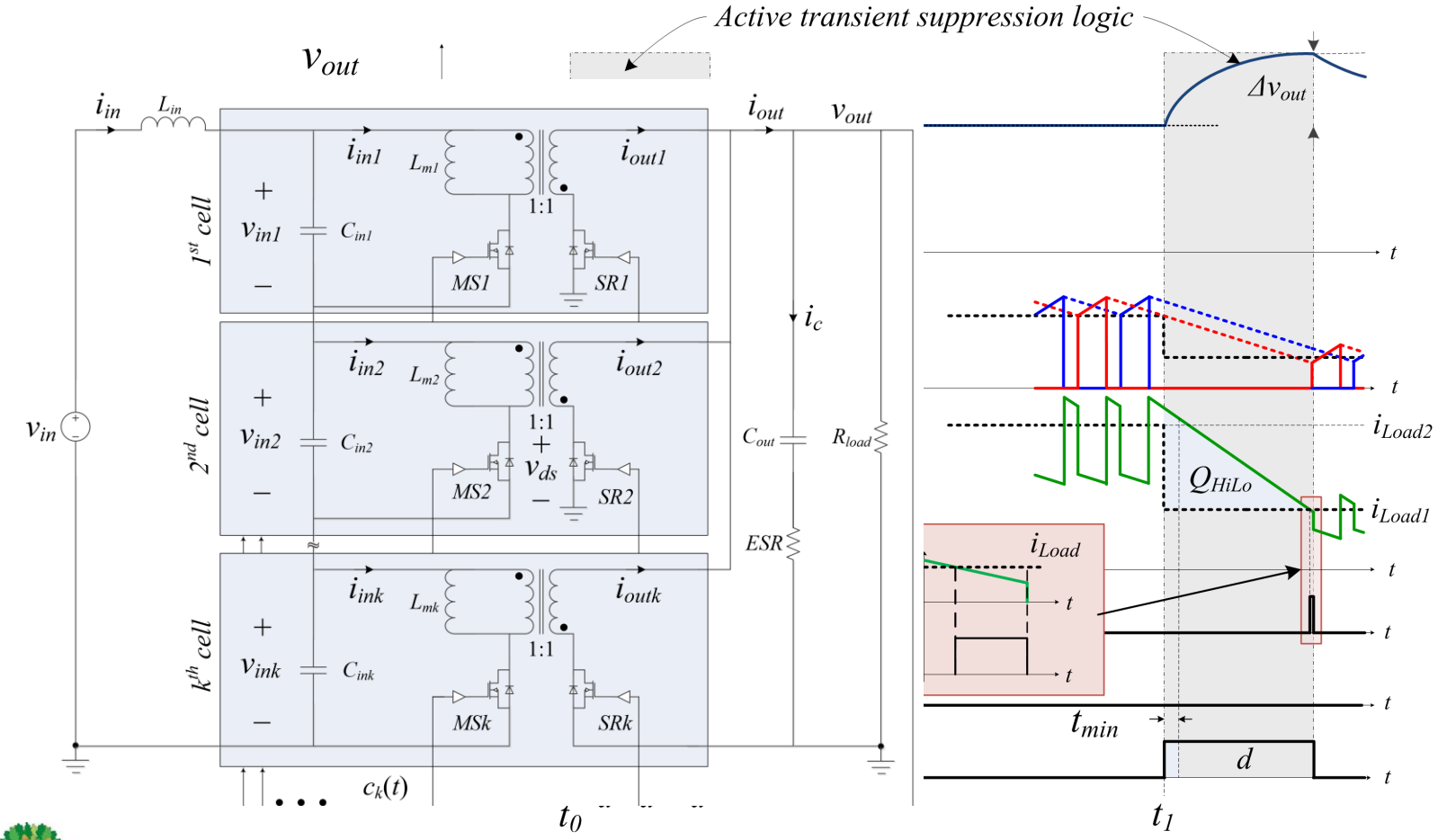
Keeps the constant on time, reduces off time (effectively increasing frequency, until the positive current of the flyback is detected)

Near Minimum Deviation Controller (Light to Heavy)



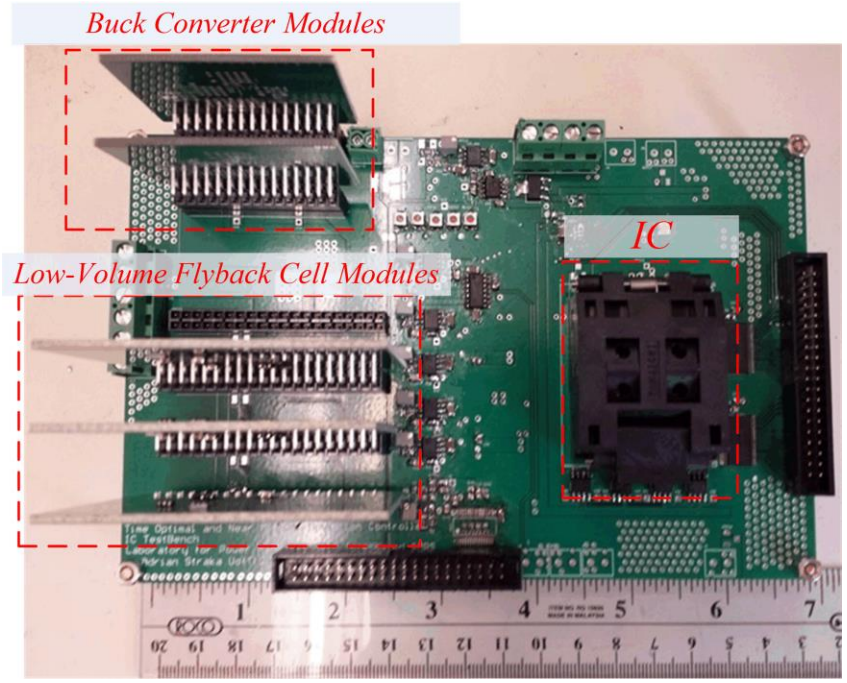
Keeps the constant on time, reduces off time (effectively increasing frequency, until the positive current of the flyback is detected)

Near Minimum Deviation Controller (Light to Heavy)

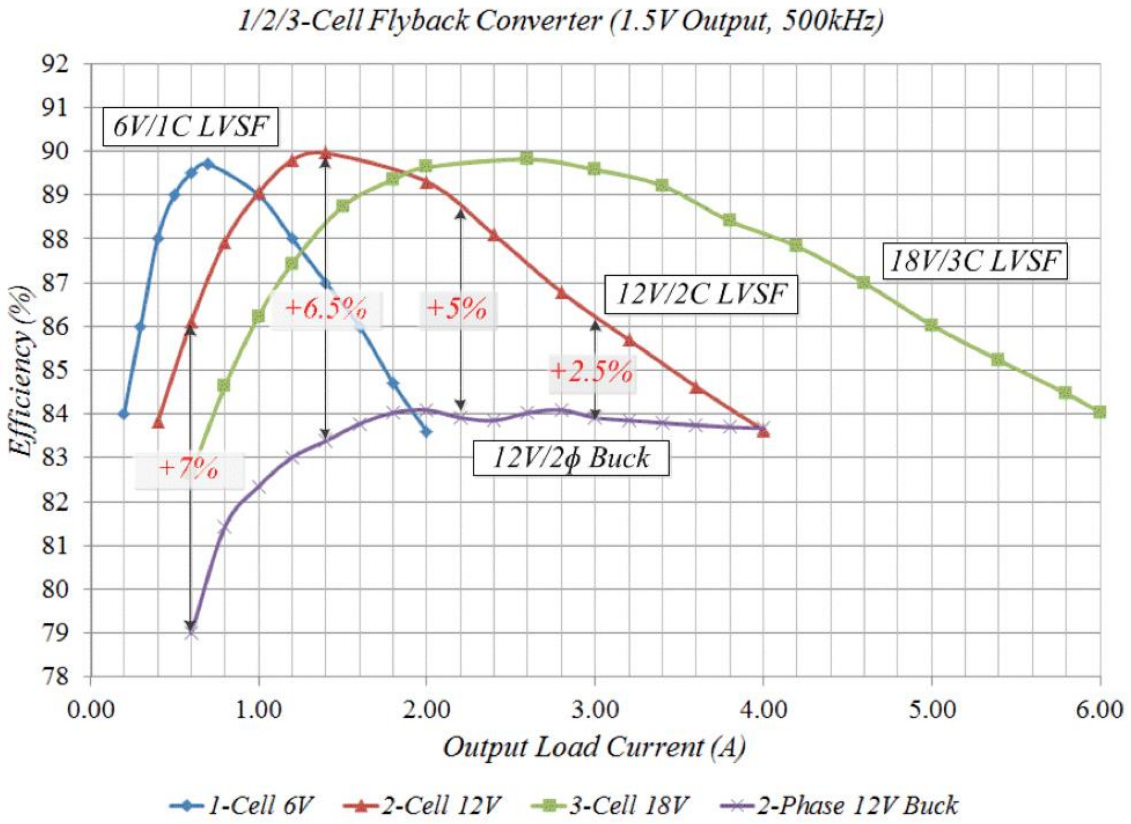


For heavy to light works almost as a conventional minimum deviation system

Experimental Implementation (board and IC)

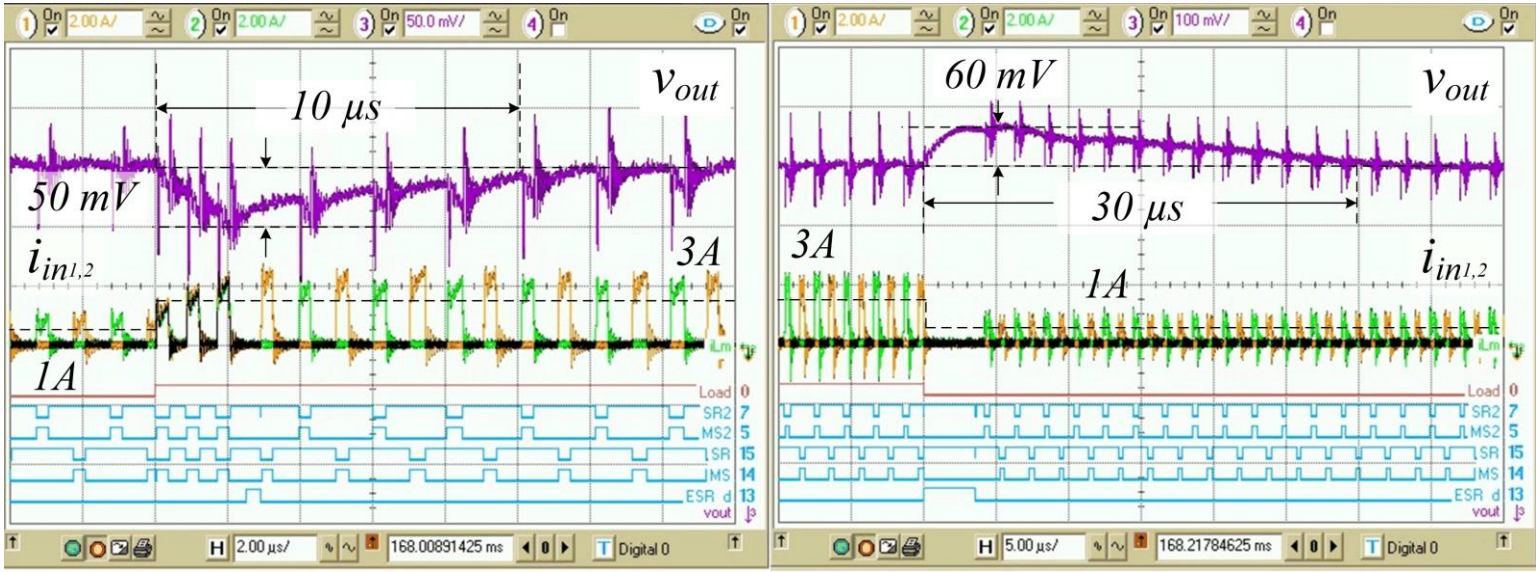


Efficiency Comparison



-Power processing efficiency is improved as well

Transient Performance



By utilizing voltage and current sharing we can reduce volume, improve efficiency while maintaining fast transient response.

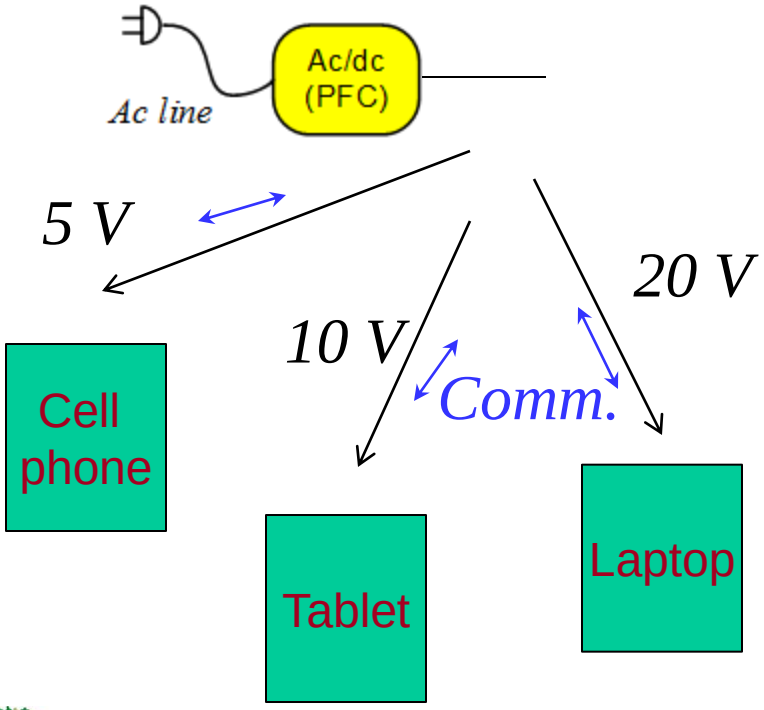
Part V

High Power Density Mixed-Signal Controlled Rectifiers with Power Factor Correction (Emerging Topologies)

Design Example: Application of Optimization Principles in Rectifiers with Power Factor Correction Applications

Programmable Output Adapter

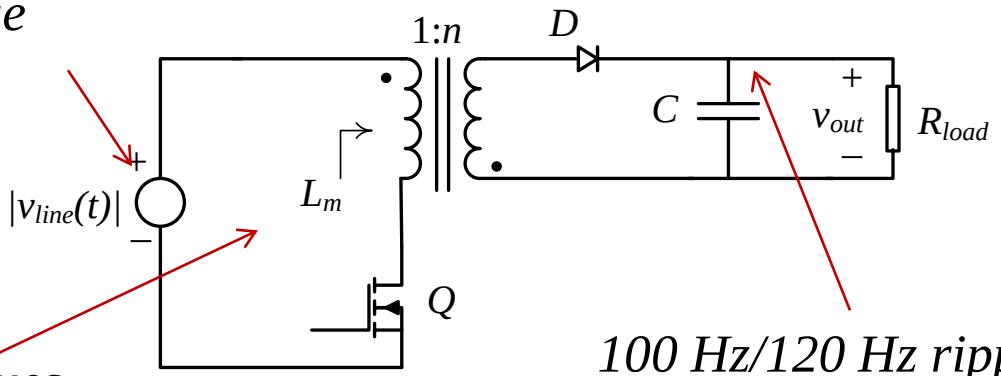
Requirements and Sizing For the Upcoming Adapters



- *The idea is to have one adapter (charger) that can work with any application*
- *Output voltage programmable between 5 V an 20, through USB communication* with the device
- *Problem with the capacitor volume*

DCM Flyback and Problem with Capacitor Sizing

Rectified line voltage

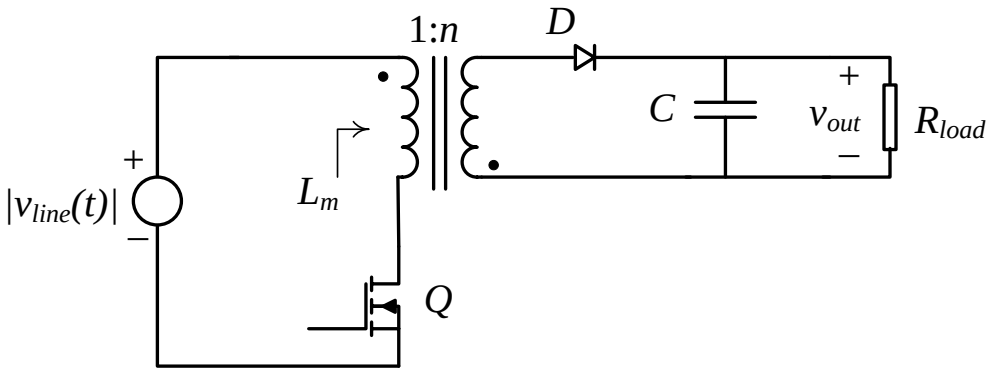


Averaged circuit behaves as a resistor

100 Hz/120 Hz ripple

- *In those applications Flyback converter operating in DCM is most often used*
- *Has a ripple at 120Hz (100 Hz) at the output capacitor*

DCM Flyback and Problem with Capacitor Sizing

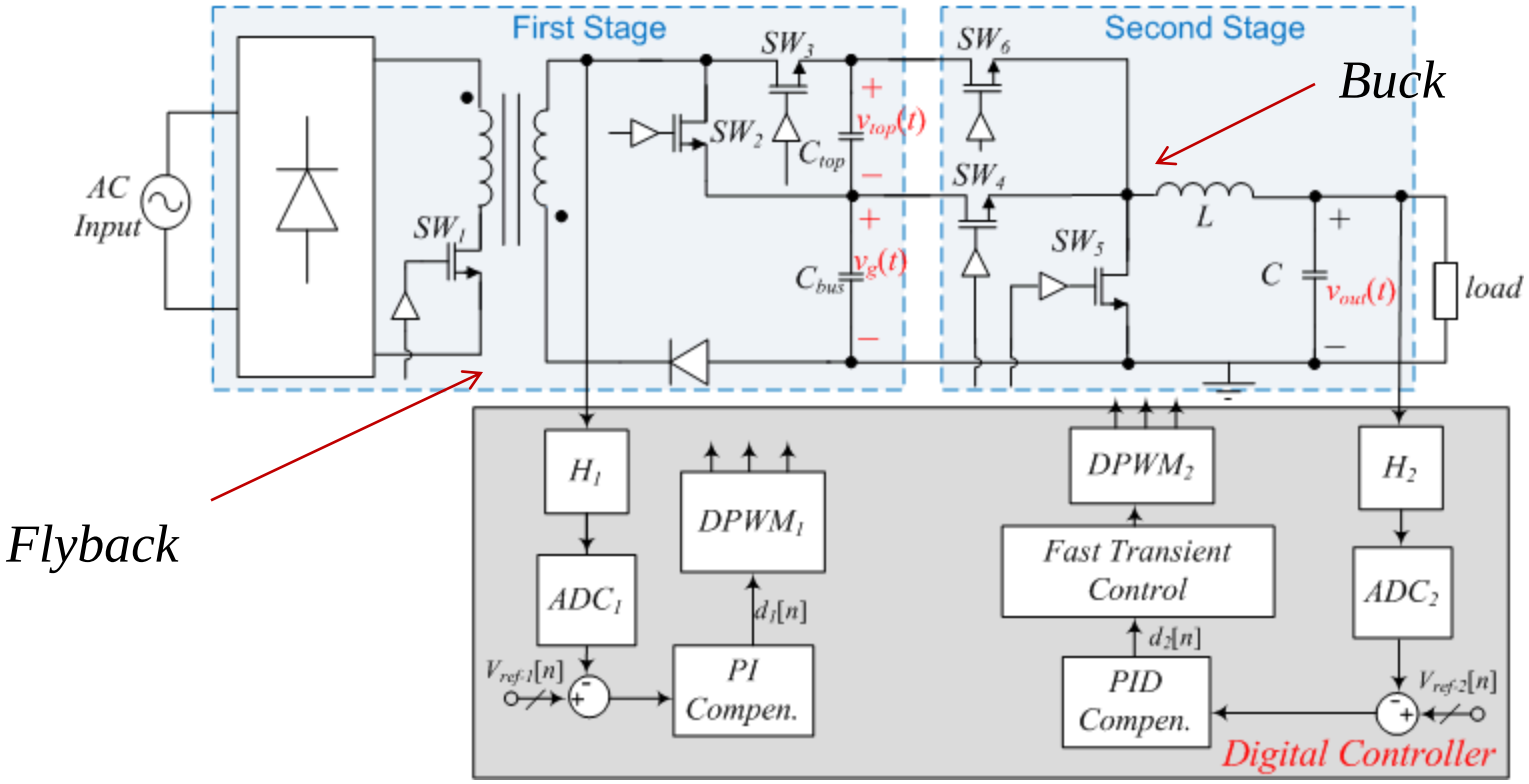


To eliminate the ripple the capacitor size can be defined as:

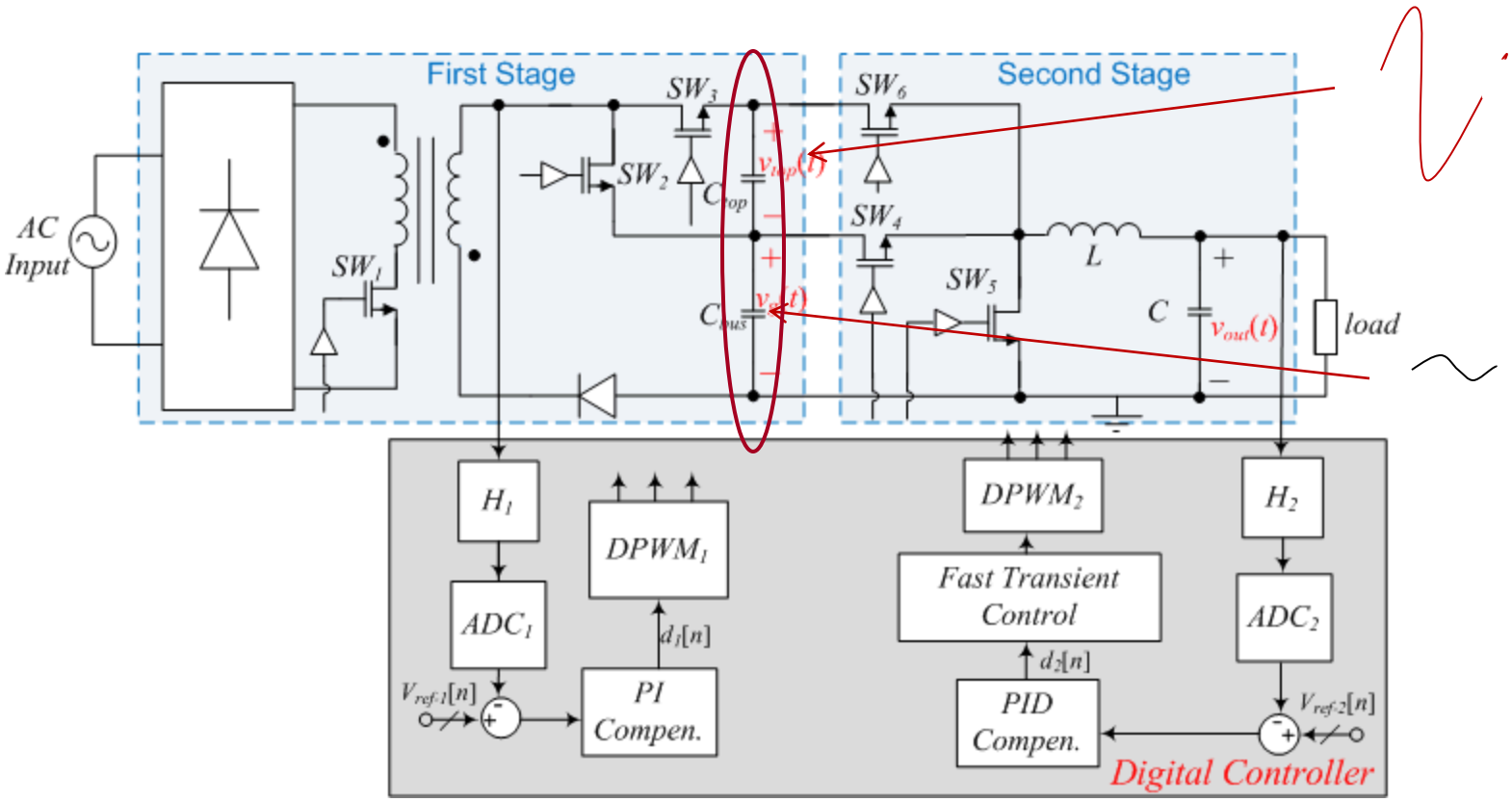
$$C \approx k \frac{P_{out}}{V_{out}^{\,2}} \left(\frac{V_{out}}{\Delta Vout} \right)$$

For 5 V, 20W output, and 1% regulation the size of the output capacitor is about 40 mF

Merged Two-Stage Solution with Energy Buffering Capacitor and On-Line Efficiency Optimization

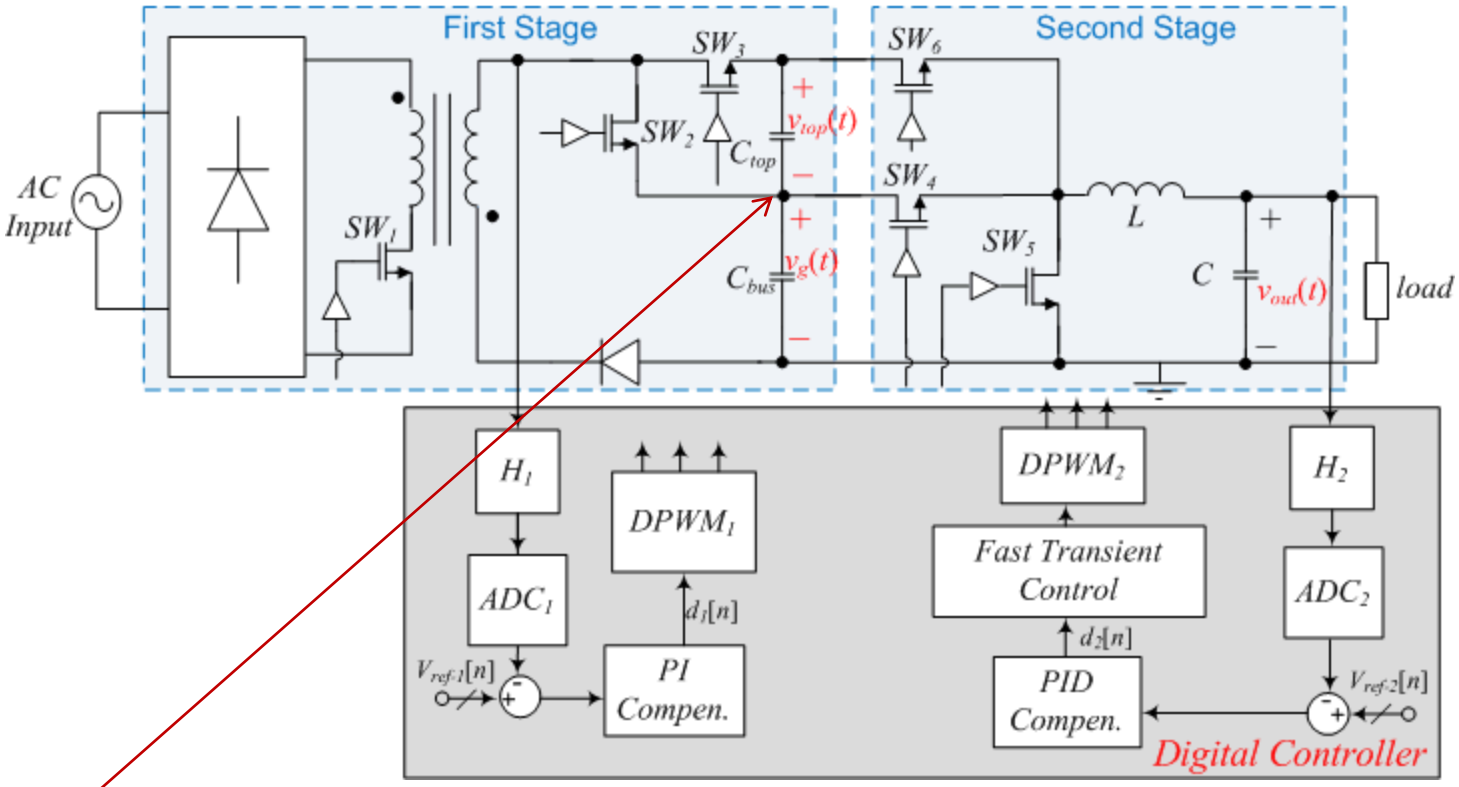


Merged Two-Stage Solution with Energy Buffering Capacitor and On-Line Efficiency Optimization



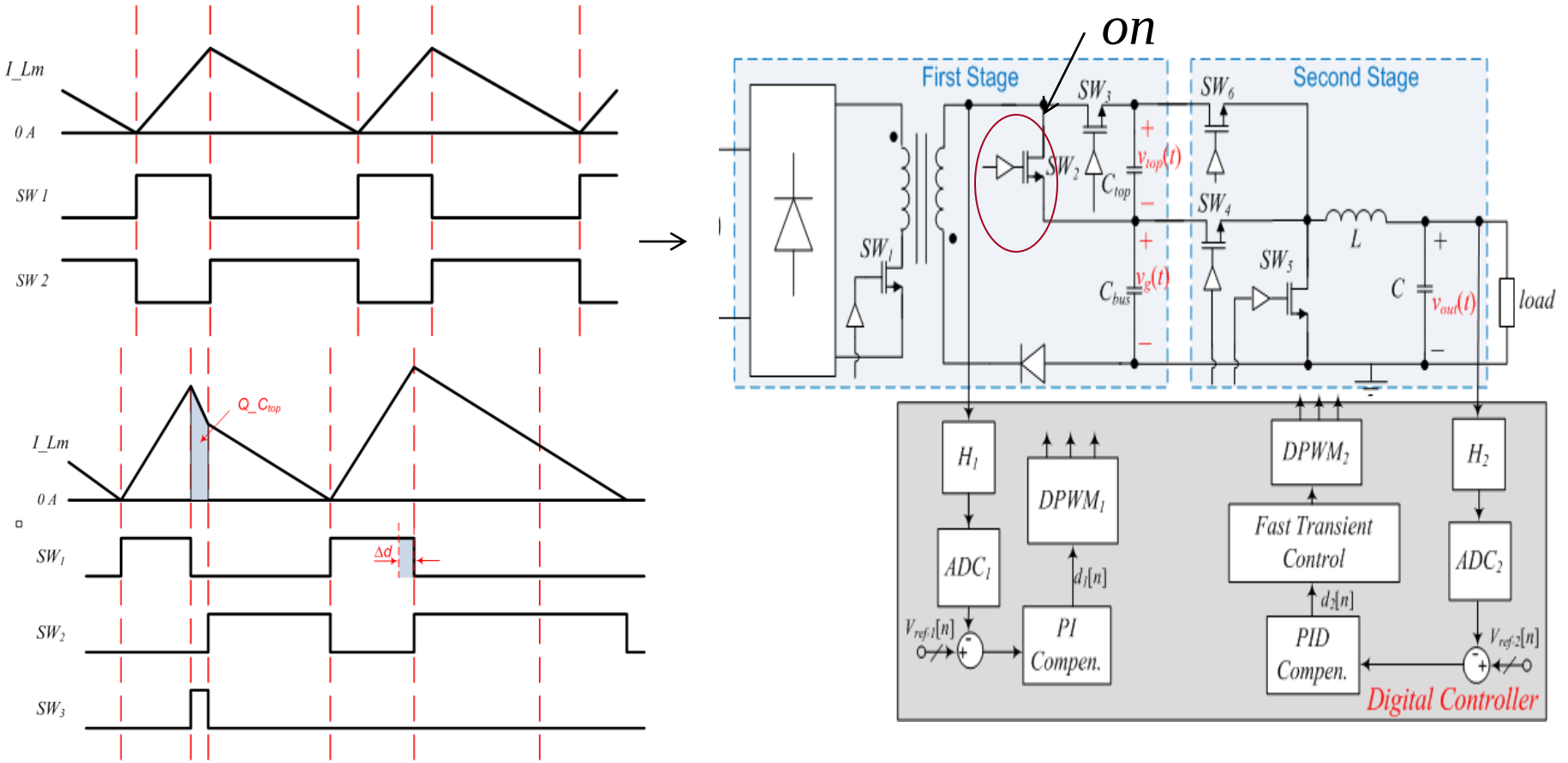
Top capacitor has much smaller value and handles larger voltage ripple (the input voltage of the buck is almost constant).

Merged Two-Stage Solution with Energy Buffering Capacitor and On-Line Efficiency Optimization



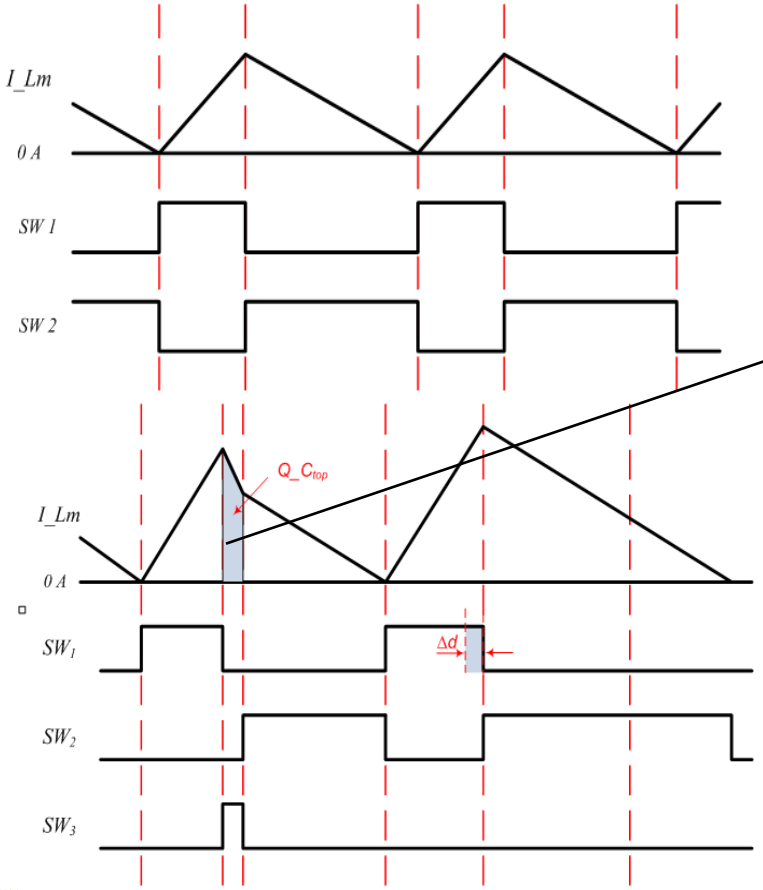
The bottom capacitor voltage is regulated such that it is just slightly larger than $v_{out}(t)$, resulting in a small output inductor.

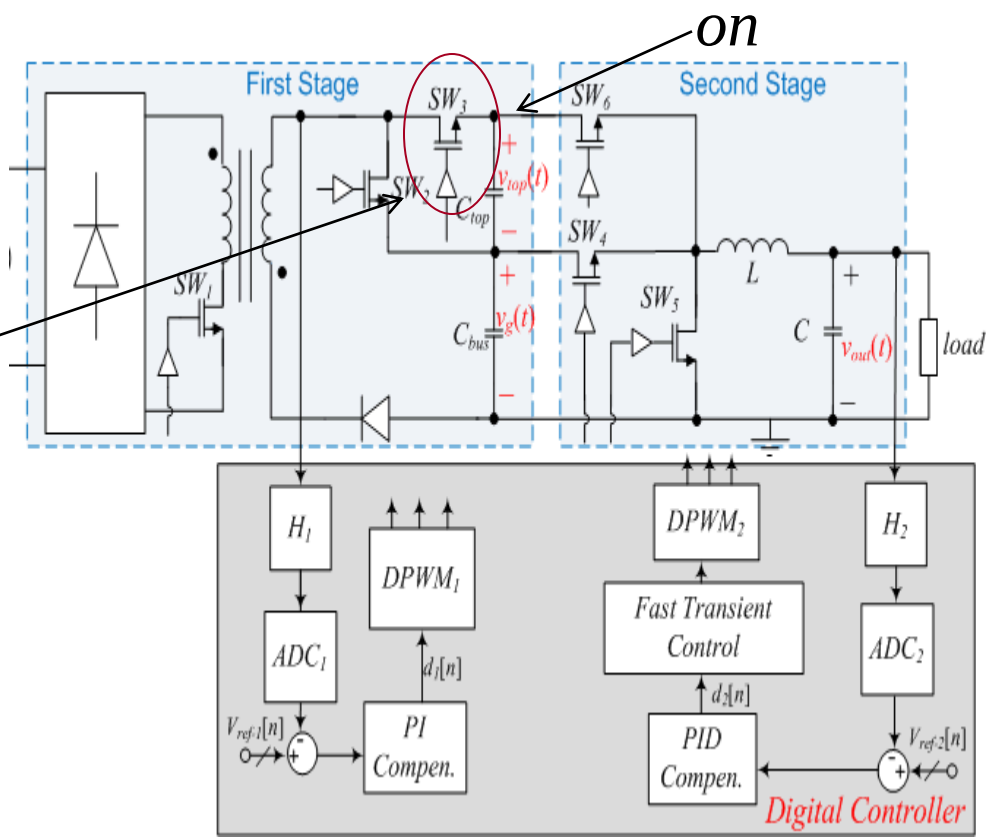
Balancing Capacitor Voltage (regulation of bottom capacitor voltage): Inductor Current Waveforms



Only once in many switching cycles, during a portion of one switching interval, changes operation from the regular mode (SW2-on) to balancing mode (SW3-on)

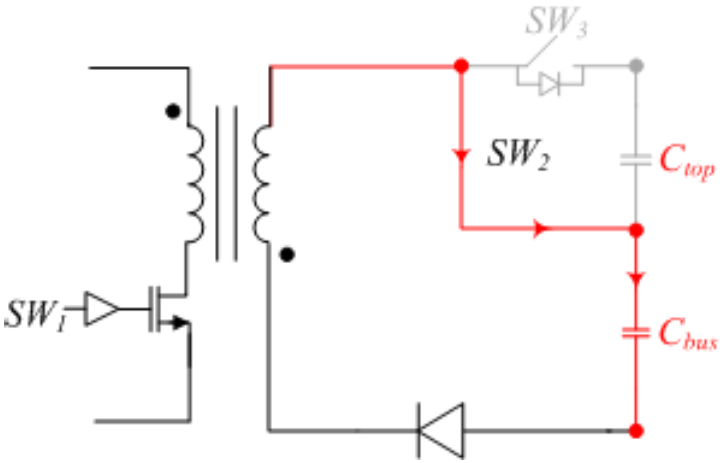
Balancing Capacitor Voltage (regulation of bottom capacitor voltage): Inductor Current Waveforms

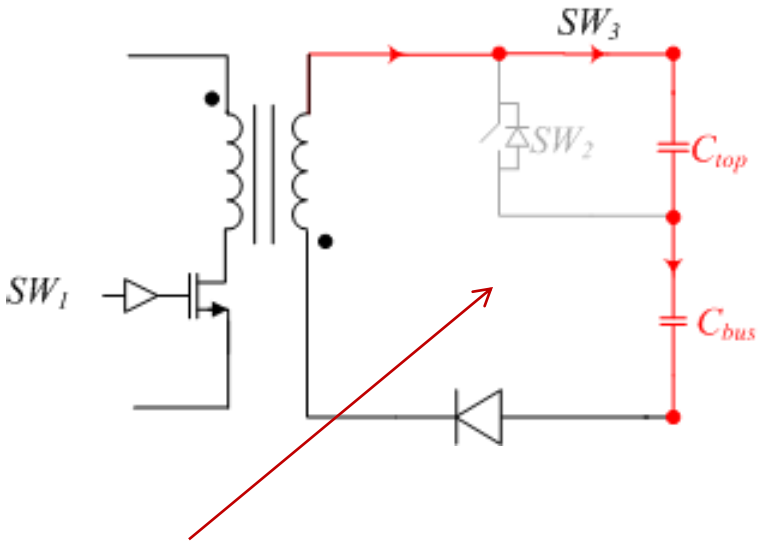




Only once in many switching cycles, during a portion of one switching interval, changes operation from the regular mode (SW2-on) to balancing mode (SW3-on)

Balancing of Capacitor Voltages

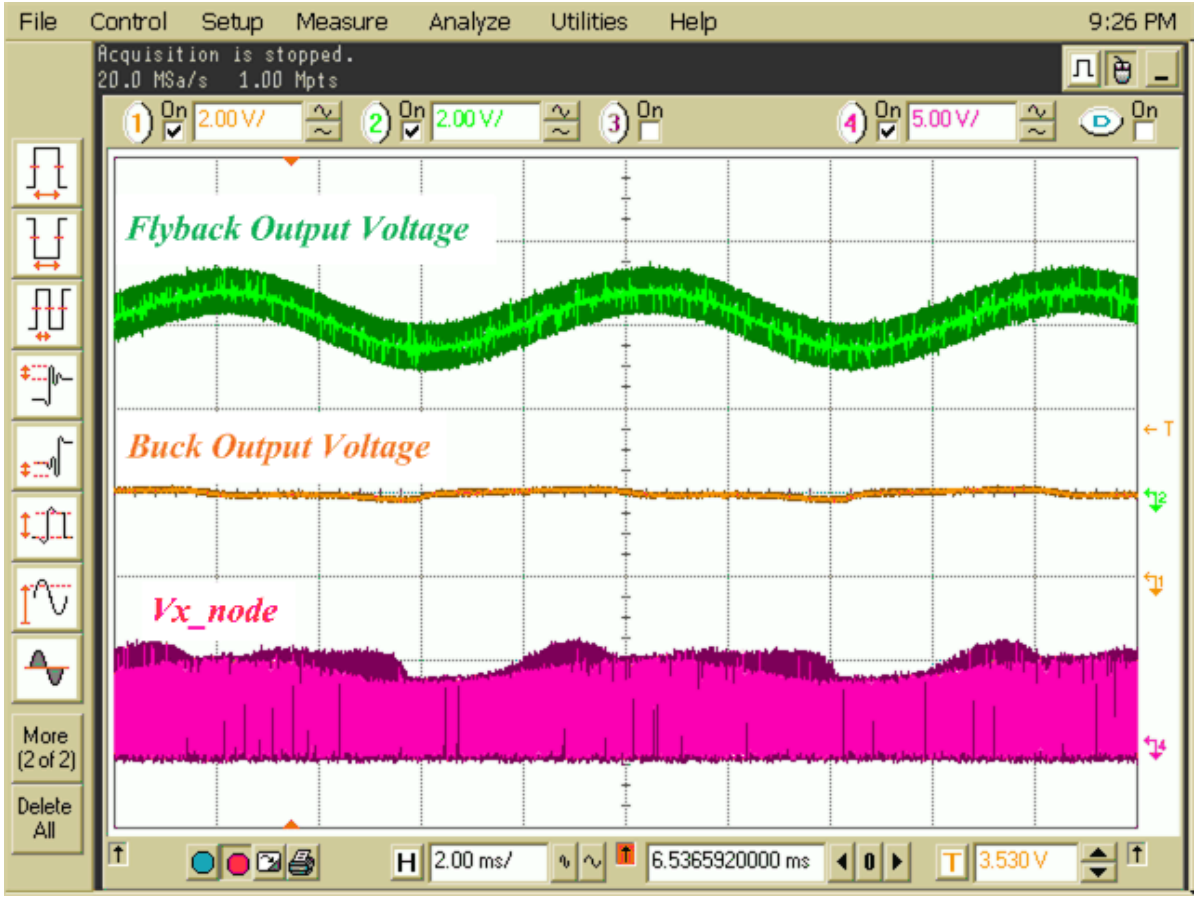




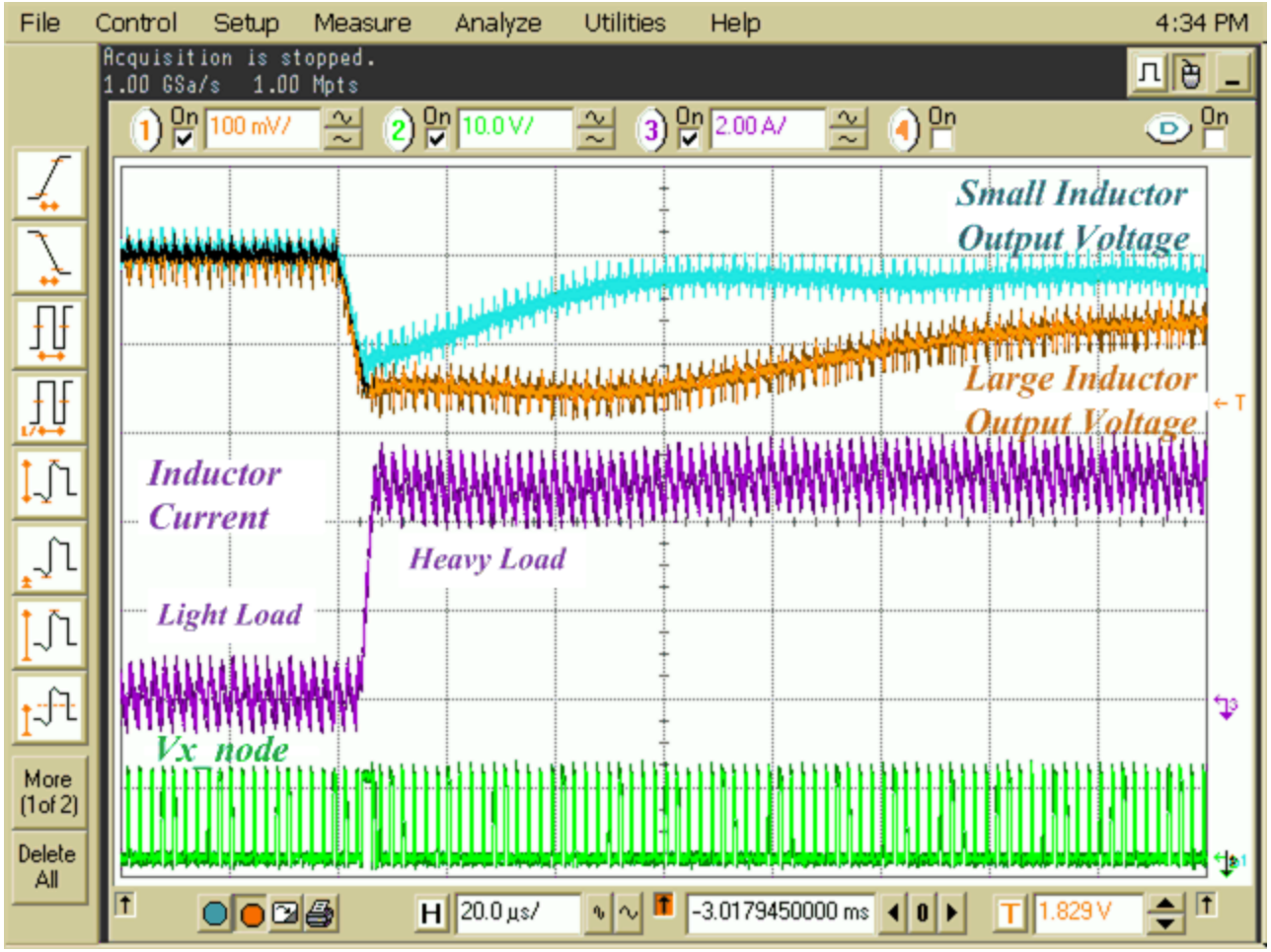
In this mode only top capacitor voltage is practically changed

Since the top cap is much smaller during the second portion of interval practically only its voltage is changed and we are achieveing independent regulation of two voltages

Experimental Results

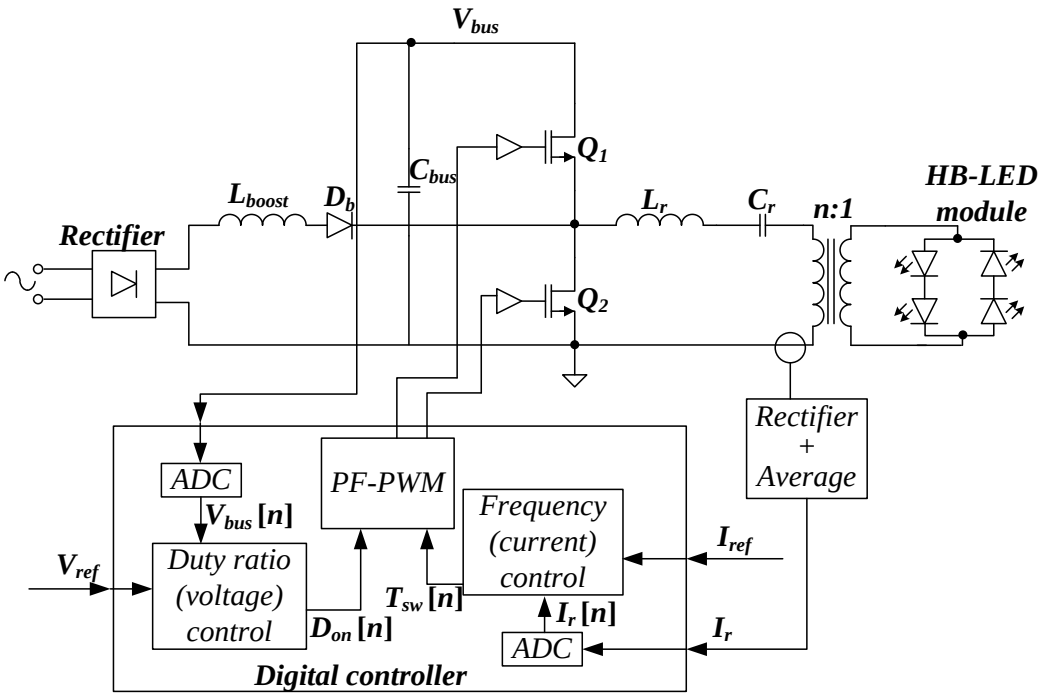


Transient Response



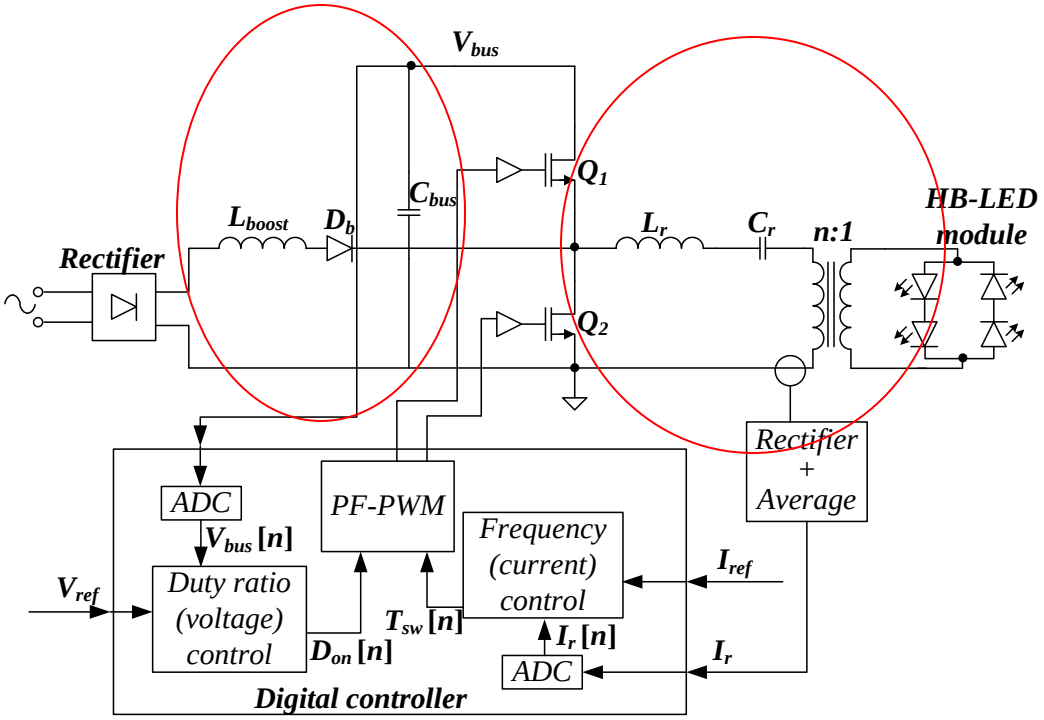
HB LED Supply Without Electrolytic Capacitor

Merged Boost PFC & Resonant Converter



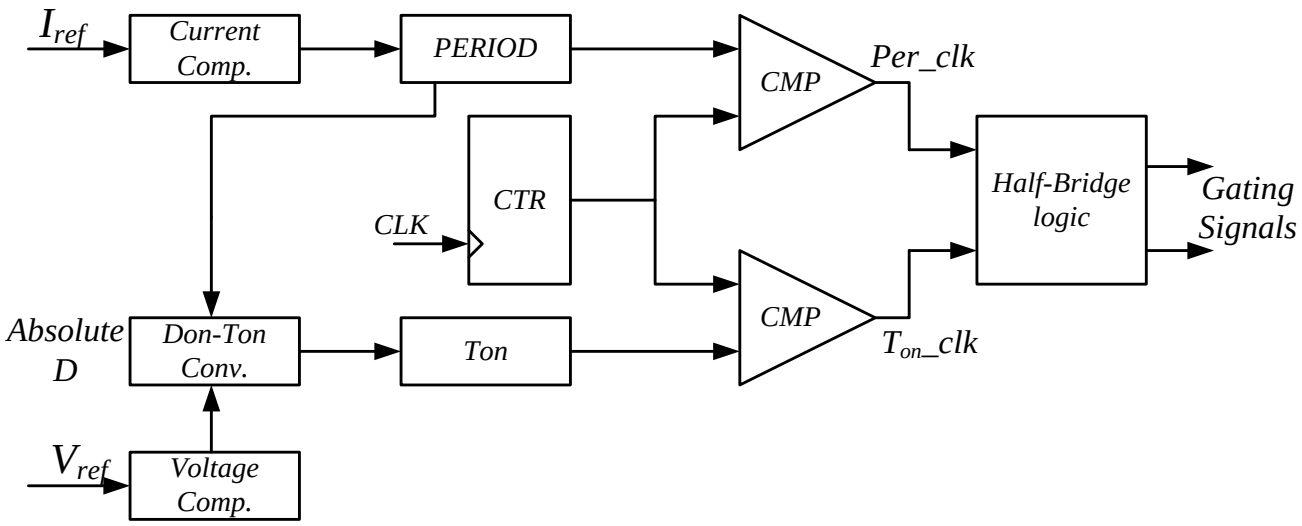
The ripple components is distributed between a small boost capacitor and resonant converter

Merged Boost PFC & Resonant Converter



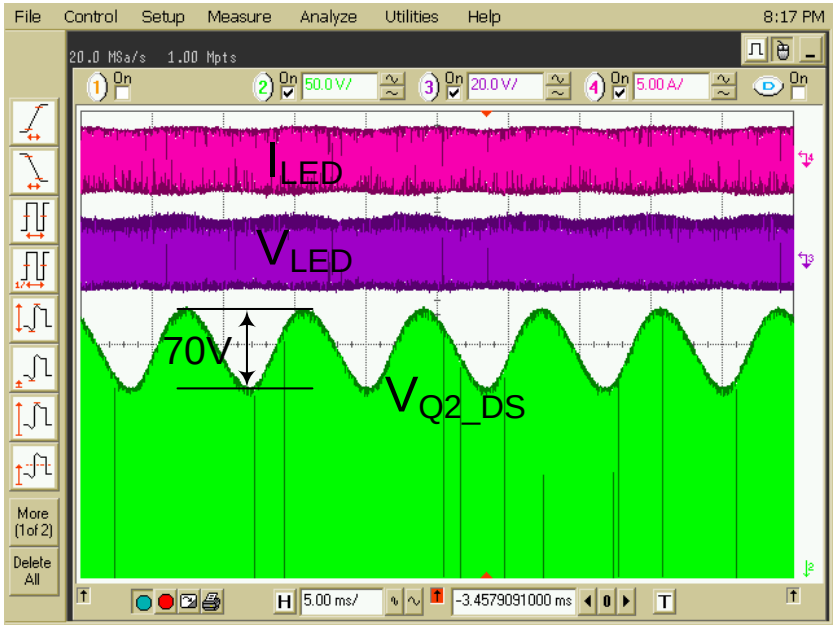
The ripple components is distributed between a small boost capacitor and resonant converter, no input voltage measurements, and shared components

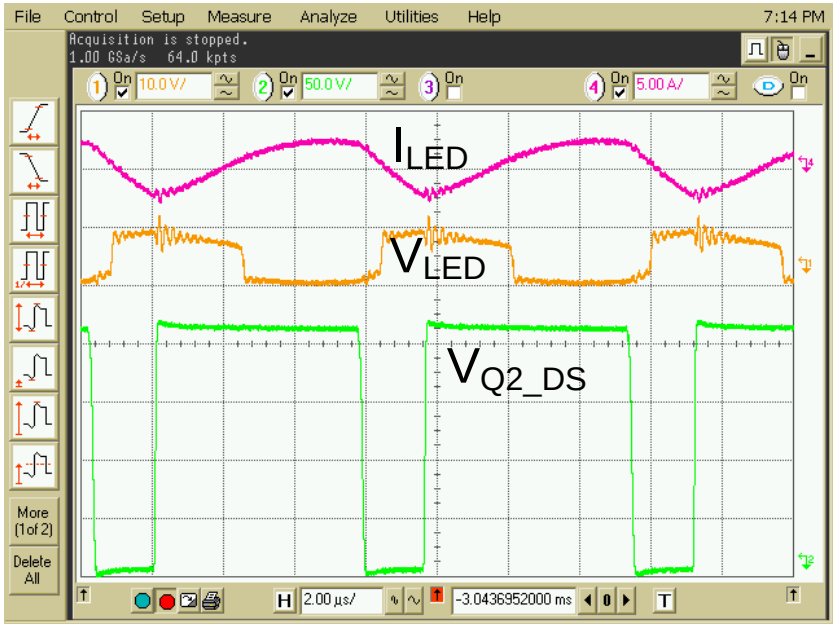
Integrated PFM and PWM Controller



Controller maintains desired duty ratio (for boost) while varying frequency to maintain ZVS of the converter (above resonance operation)

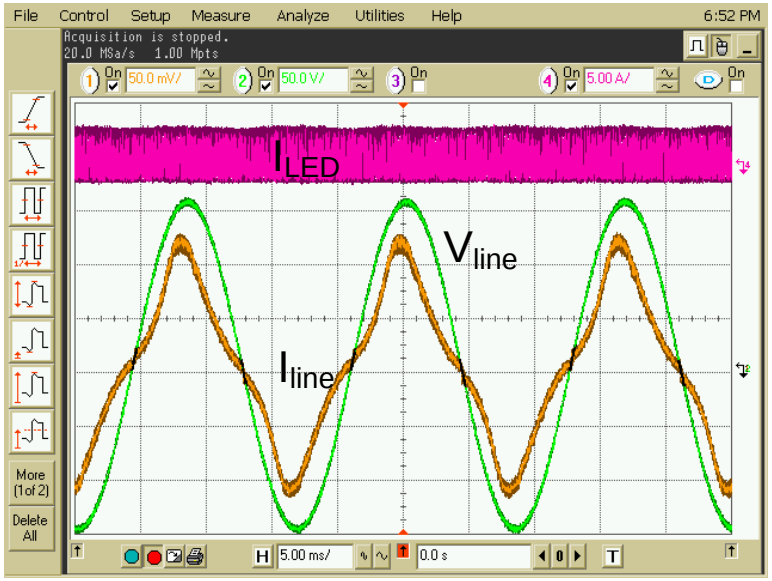
Experimental Waveforms

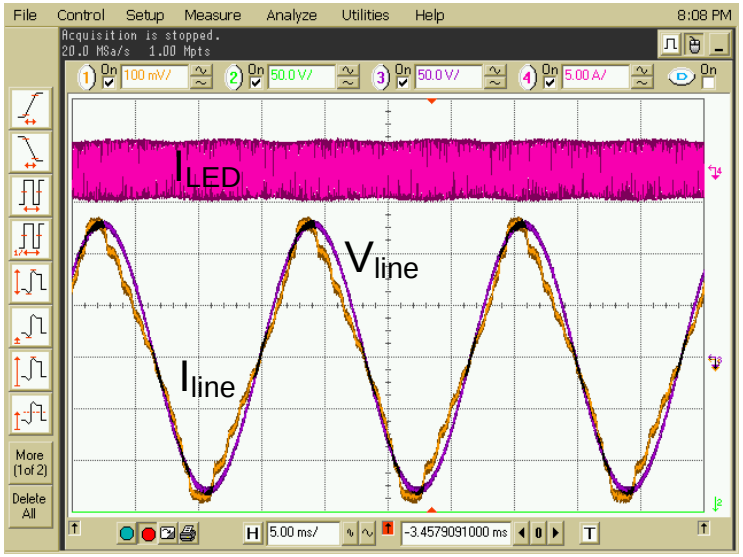




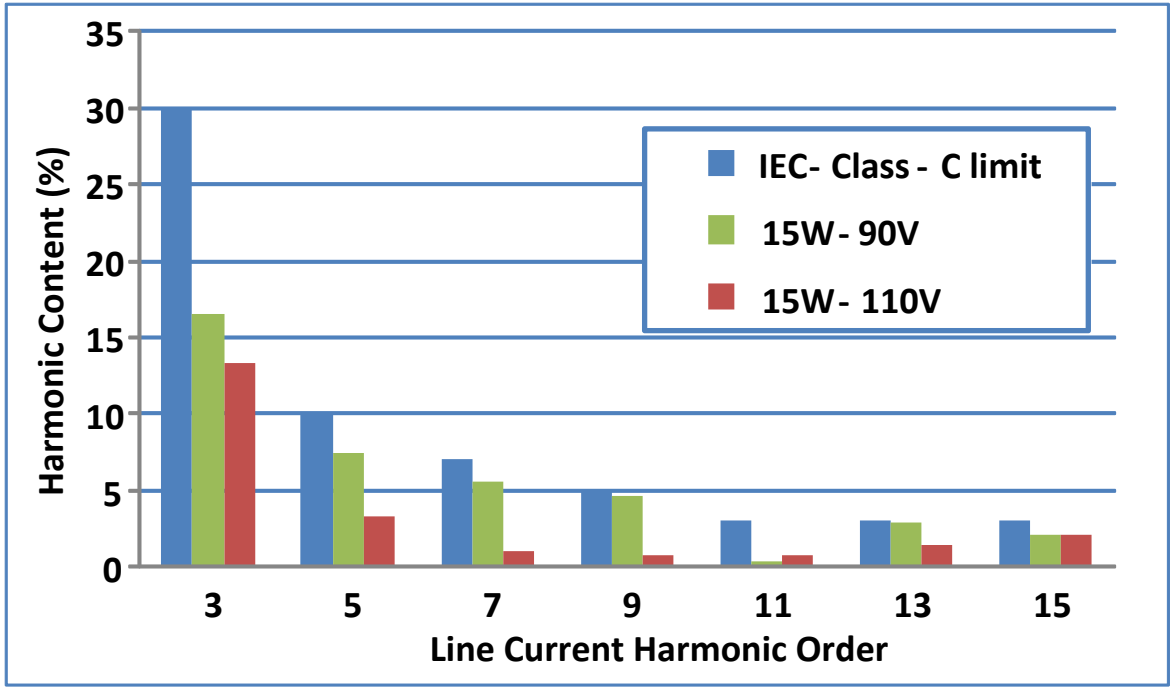
Large ripple allowed across boost ceramic capacitor

Input Current Waveforms



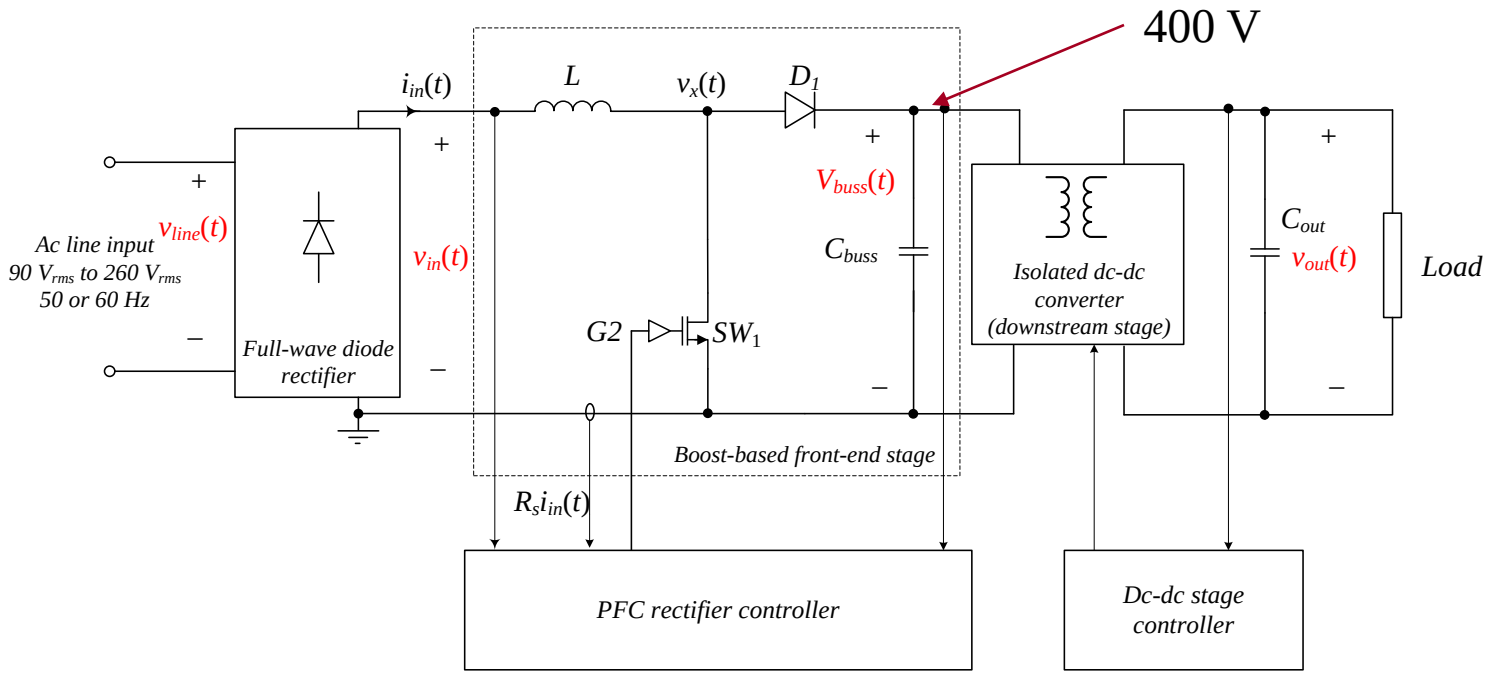


Harmonics


35
30
25
20
15
10
5
0
Harmonic Content (%)
IEC- Class - C limit
15W - 90V
15W - 110V
3
5
7
9
11
13
15
Line Current Harmonic Order

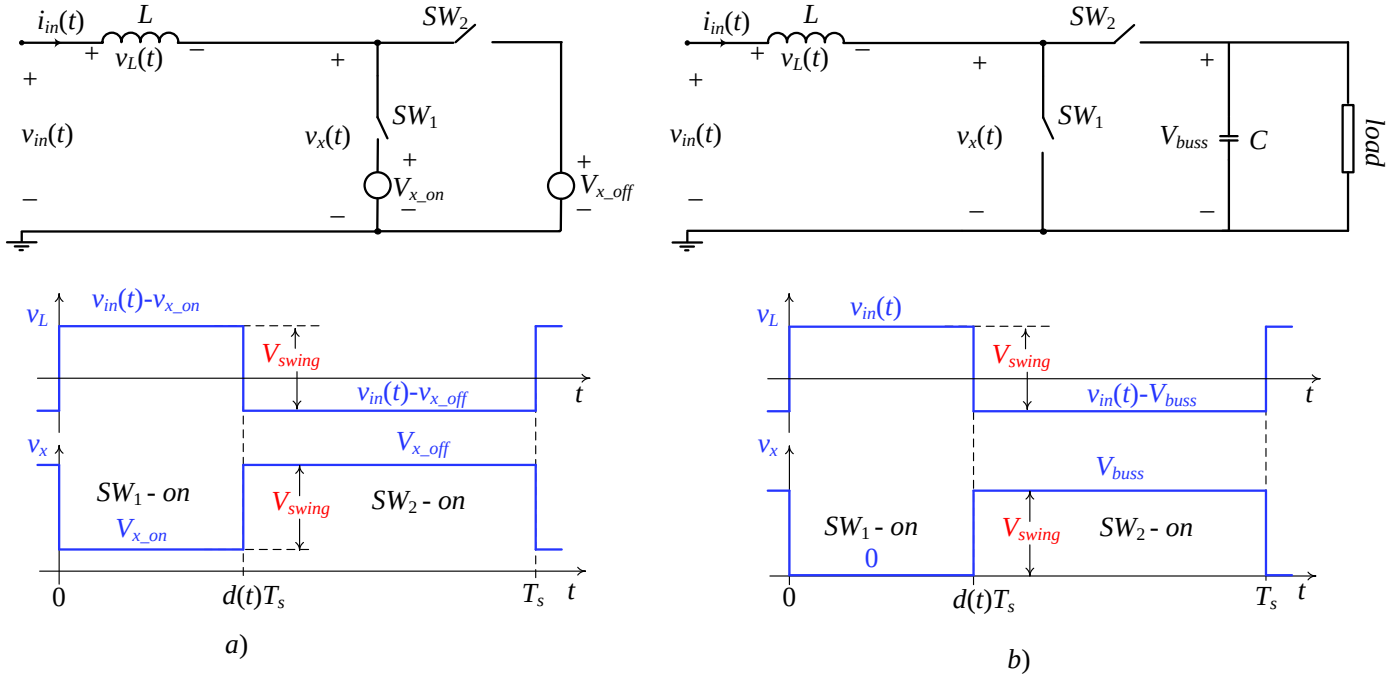
Low-Volume PFC Based on a Boost With Non-Symmetric Capacitive Divider

Conventional Boost Based PFC Rectifier + Downstream



- Very large boost inductor due to a large voltage swing (400 V)
- Bulky heat sink to cool down the switch (and diode) due to high switching losses

Inductor Voltage Swing in a Boost-Derived Converters



$$\Delta I_{ripple\_\max} = \frac{v_{L\_high}(t) - v_{L\_low}(t)}{8L} \times \frac{1}{f_{sw}} = \frac{V_{swing\_L}}{8L}\frac{1}{f_{sw}} = \frac{V_{swing\_x}}{8L}\frac{1}{f_{sw}}$$

Inductor voltage swing is equal to the switching node voltage swing.

General Principle

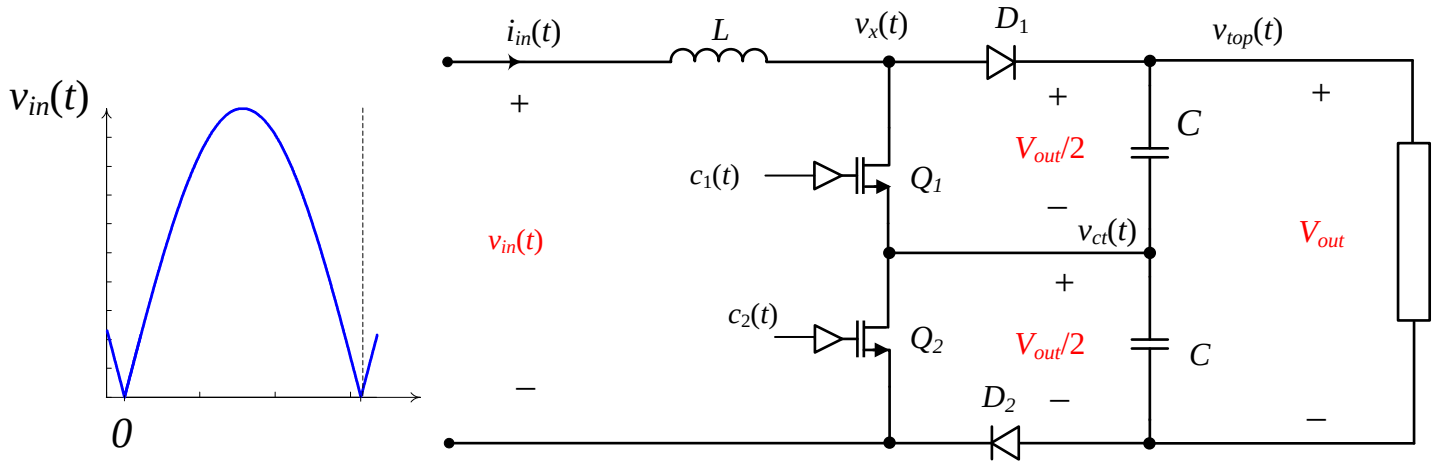
To reduce L and, consequently, C operation at high switching frequency is usually targeted, alternatively we can reduce the swing voltage.

$$\Delta I_{ripple} \approx \frac{v_{L\_on}(D)}{2Lf_{sw}} = \frac{v_{L\_off}(1-D)}{2Lf_{sw}}$$

Here, to minimize the L, we can reduce the inductor voltage swing , ideally making it 0

Load-Source Inversion and Boost Based Architectures (Original Architectures)

3-Level Boost



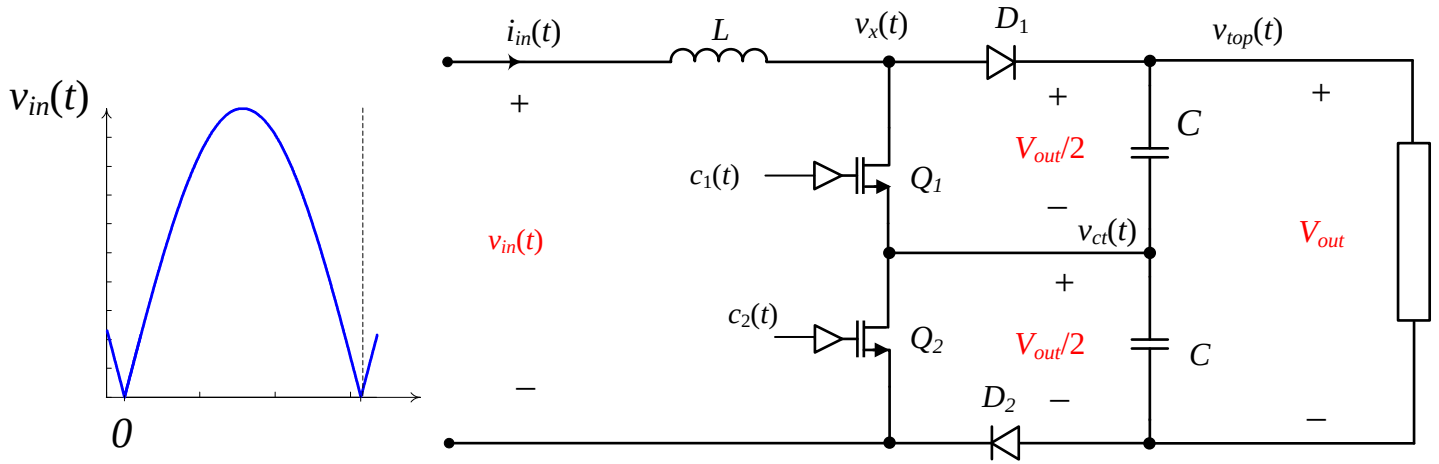
[1] T.A. Meynard, H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in Proc. IEEE PESC '92, pp.397-403 vol.1.

[2] L. Balogh, R. Redl, "Power-factor correction with interleaved boost converters in continuous-inductorcurrent mode," in Proc. IEEE APEC '93. pp.168-174.

[3] M.T. Zhang, Y. Jiang, F.C. Lee, M.M Jovanovic, "Single-phase three-level boost power factor correction converter ," in Proc. IEEE APEC '95, pp.434-439 vol.1.

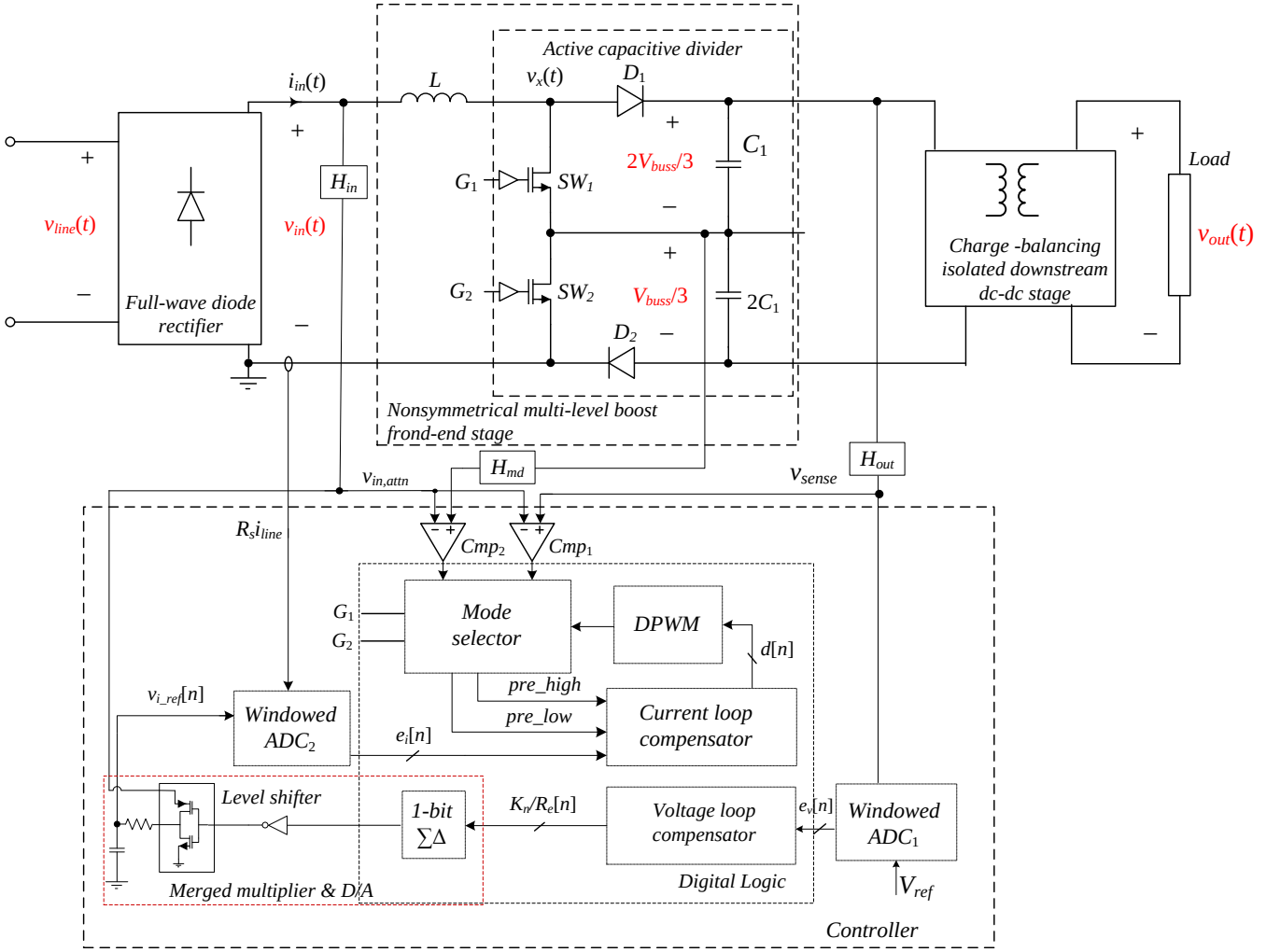
[4] J. Salmon, A. Knight, J. Ewanchuk, N. Noor, "Multi-level single phase boost rectifiers using coupled inductors," in Proc. IEEE PESC 2008, pp.3156-3163.

3-Level Boost



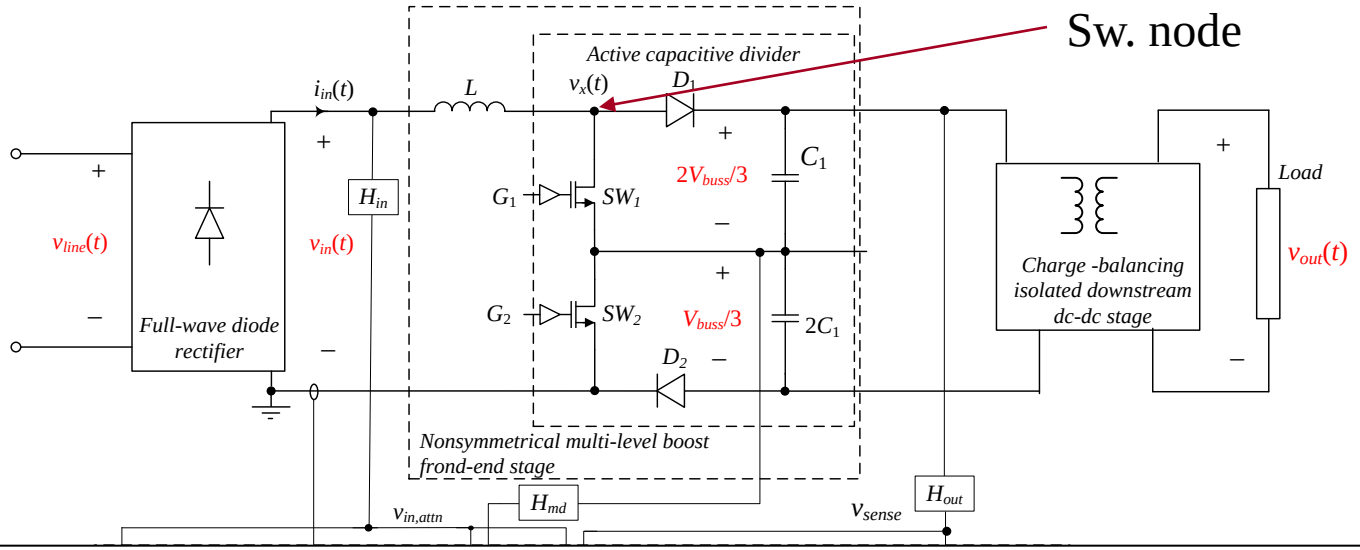
- The switching sequence is changed depending on the input voltage level, such that the voltage swing is reduced (+)
- The inductor volume is reduced by 50% compared to conventional(+)
- Lower Switching losses (+)
- Direct extension to a larger number of levels results in exponent increase in the switching components count (-)

Non-symmetric Multi-Level Boost PFC + Downstream



[1] B. Mahdavikhah, R. DiCecco, and A.Prodić, "Low-volume PFC rectifier based on non-symmetric multi-level boost converter," in Proc. IEEE Applied Power Electronics Conference (APEC), 2013

Non-symmetric Multi-Level Boost PFC + Downstream

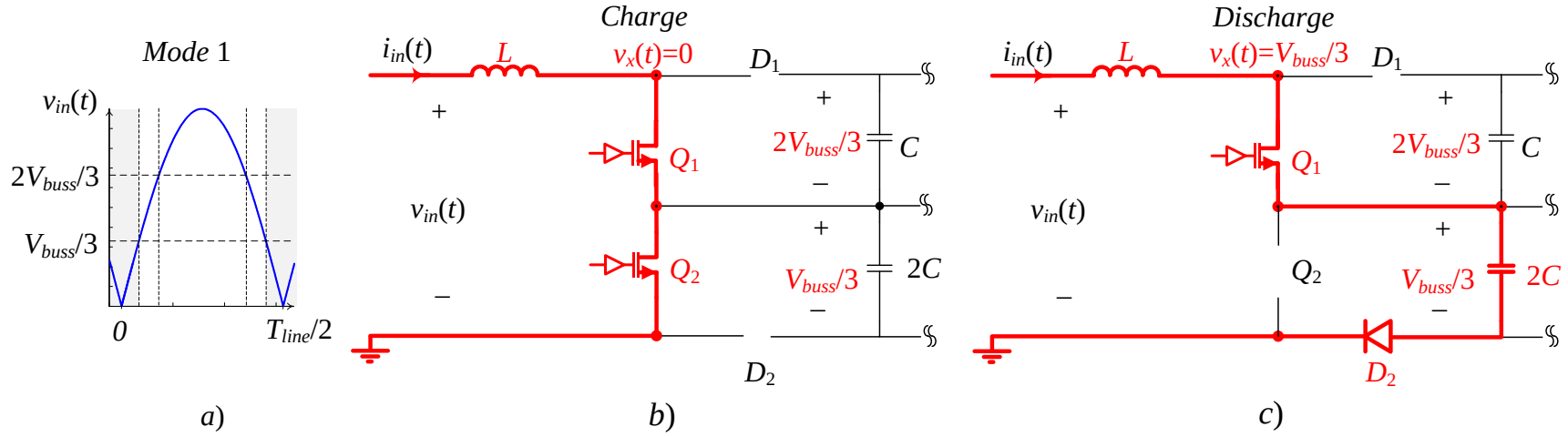


- The output capacitor replaced with non-symmetric divider, the middle tap is held at Vbus/3 (not Vbus/2)
- The structure of the circuit changes with the input voltage
- We can produce four node voltages 0, Vbus, Vbus/3, and 2Vbuss/3
- Inductor reduced by 3 times
- Switching losses reduced as well (lower switching losses)

Modes of Operation: Mode 1 ($V_{in}<V_{bus}/3$)

Mode of operation changes, depending on the input voltage level.

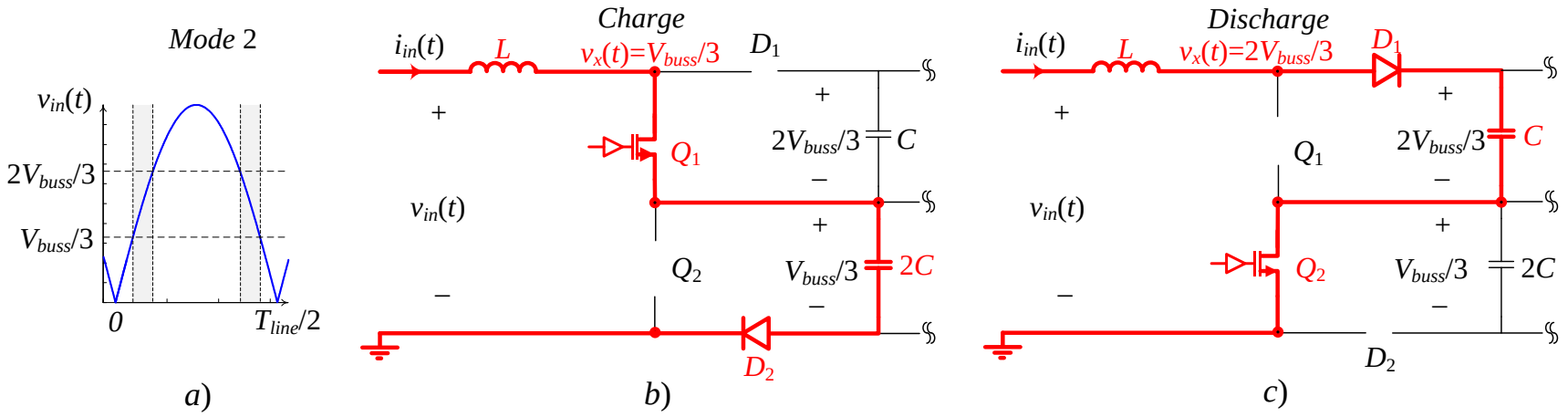
1



$$V_{swing} = V_{bus}/3,\ V_{bl\_Q1}=2V_{bus}/3,\ V_{bl\_Q2}=V_{bus}/3\ V_{bl\_D2}=V_{bus}/3,\ V_{bl\_D1}=2V_{bus}/3$$

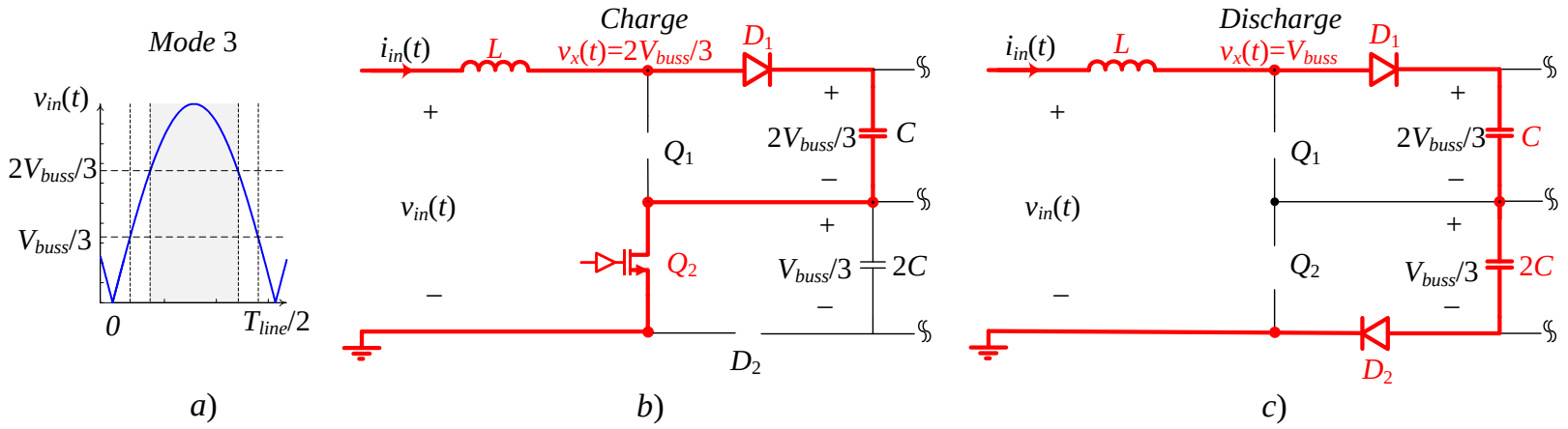
Modes of Operation: Mode 2 ($V_{bus}/3<V_{in}<2V_{bus}/3$)

2



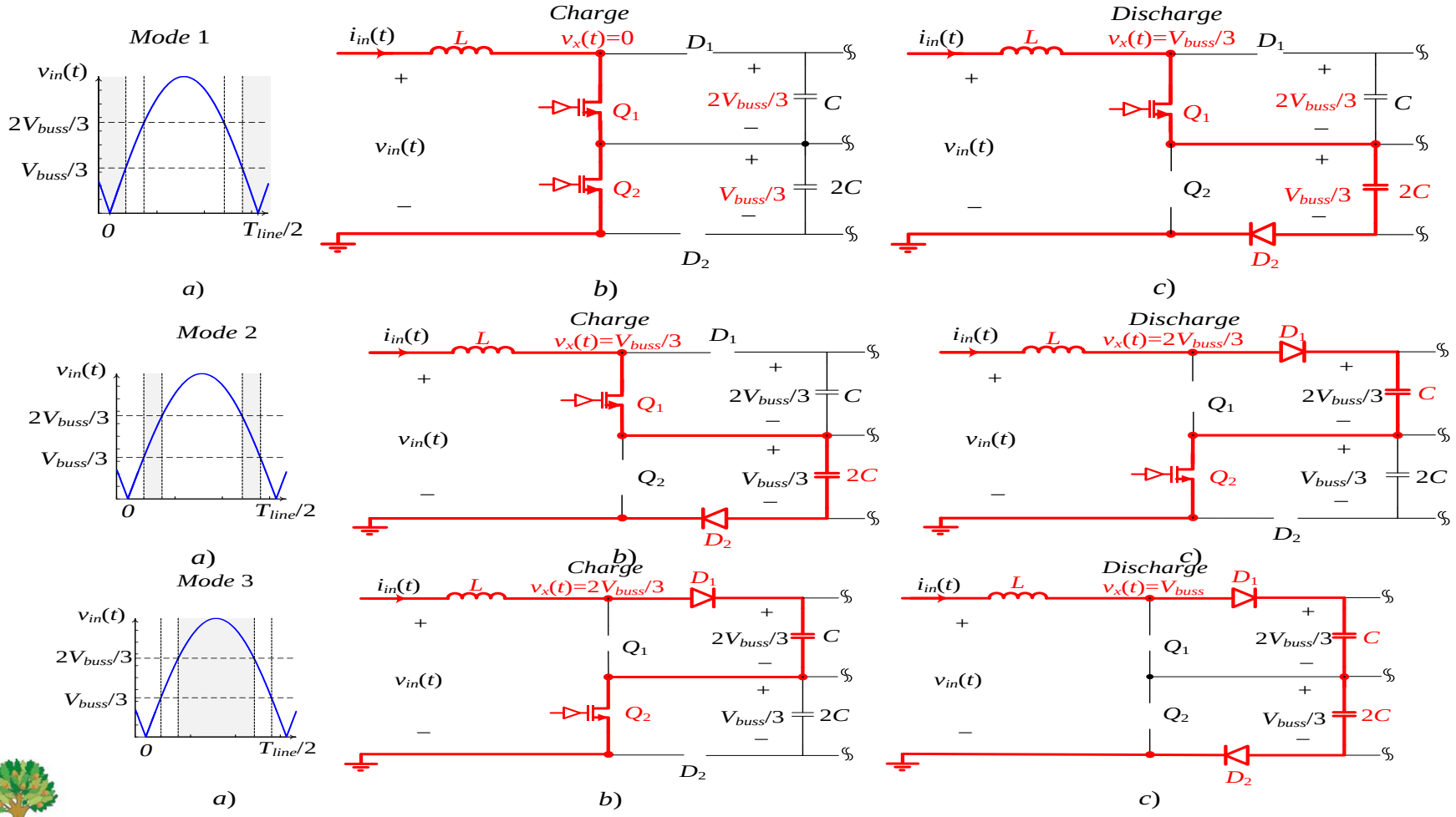
$$V_{swing} = V_{bus}/3,\ V_{bl\_Q1}=2V_{bus}/3,\ V_{bl\_Q2}=V_{bus}/3\ V_{bl\_D2}=V_{bus}/3,\ V_{bl\_D1}=2V_{bus}/3$$

Modes of Operation: Mode 3 ($2V_{bus}/3<V_{in}$)



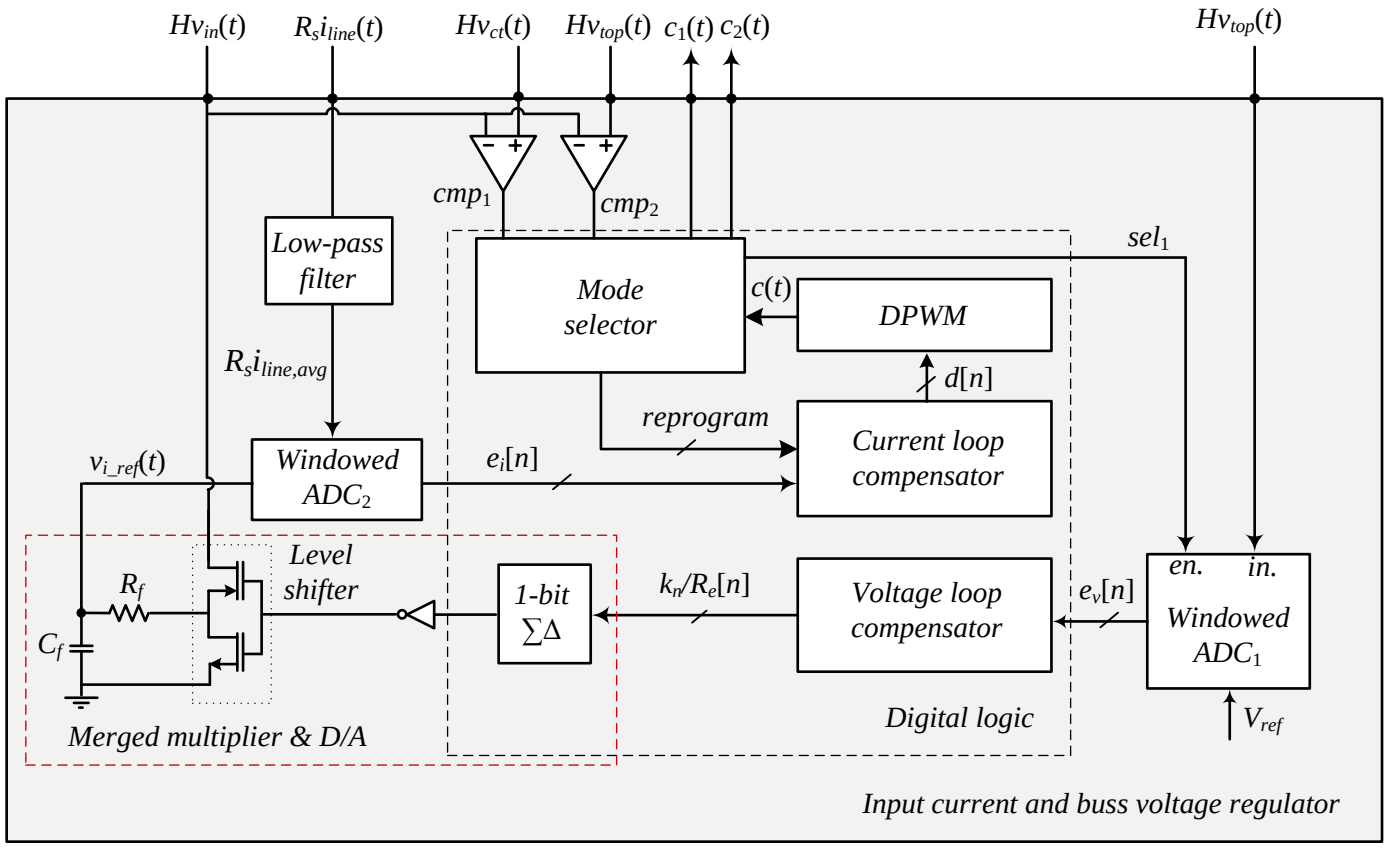
$$V_{swing} = V_{bus}/3,\ V_{bl\_Q1}=2V_{bus}/3,\ V_{bl\_Q2}=V_{bus}/3\ V_{bl\_D2}=V_{bus}/3,\ V_{bl\_D1}=2V_{bus}/3$$

4-Level Converter (Looks like a 3 level)

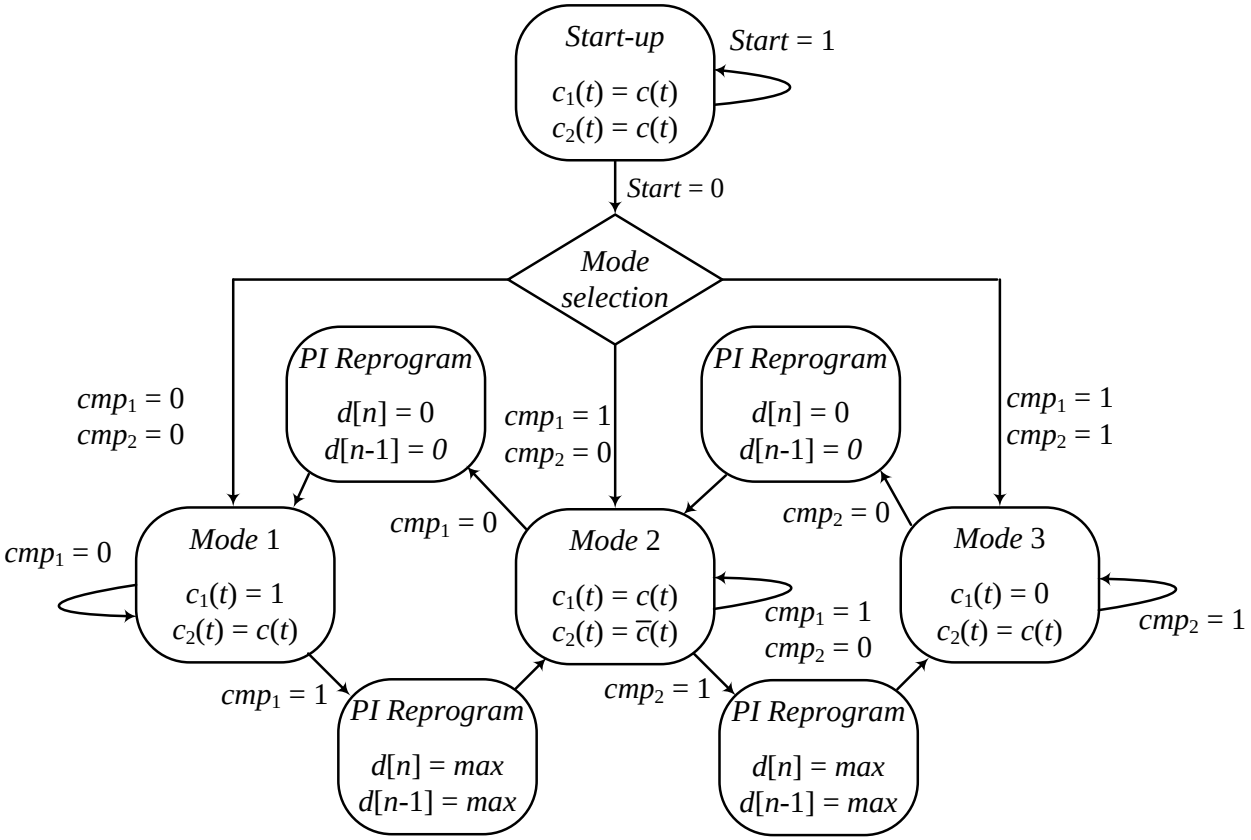


The switching node can have 4 different voltage levels, therefore, the converter behaves as a 4-level converter using 3-level hardware.

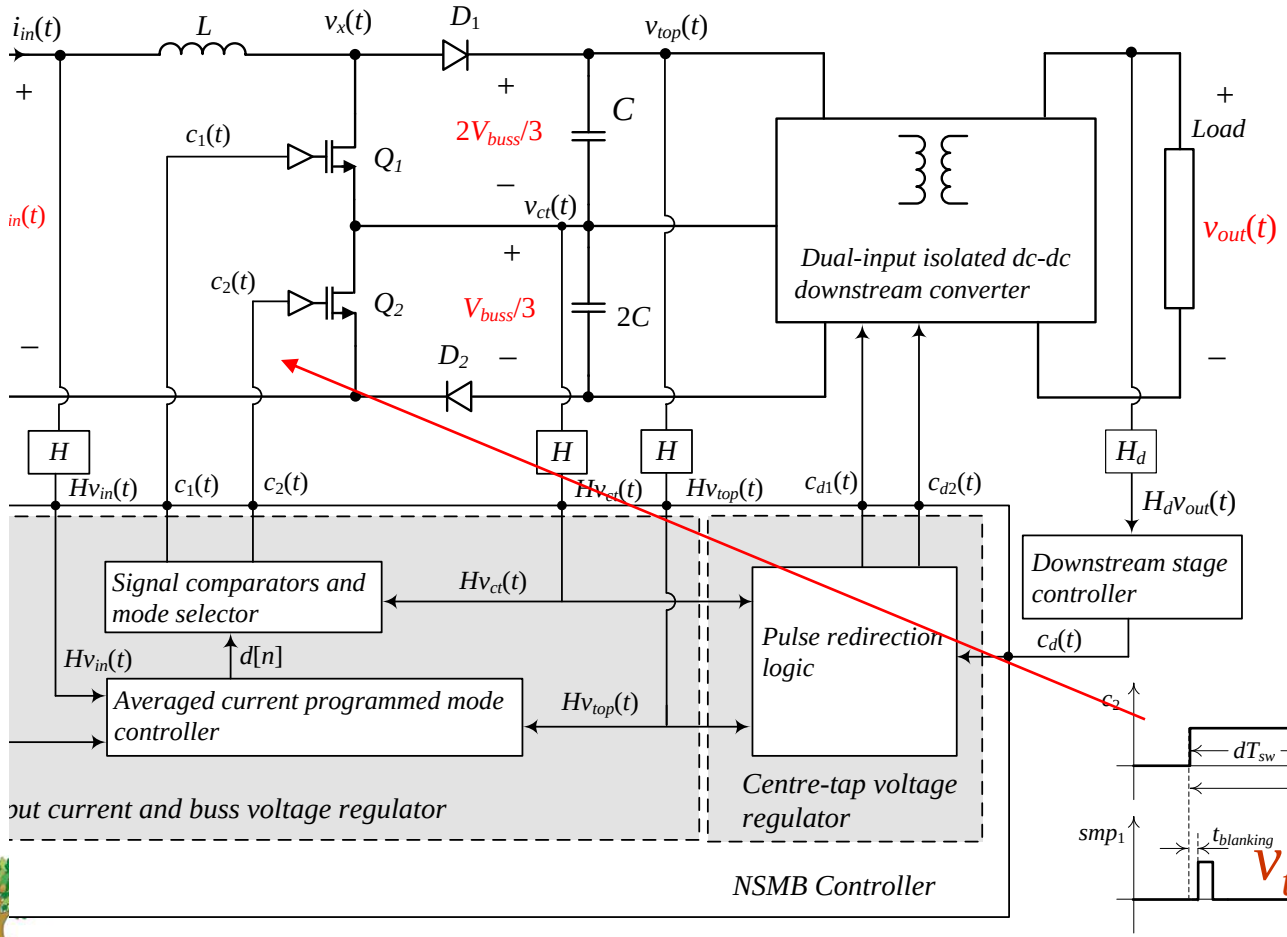
Practical Controller Implementation

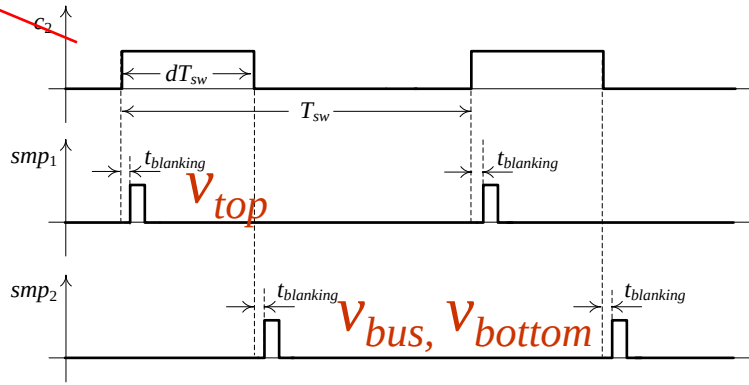


Mode Selection Logic and Bump-less Mode Transitions

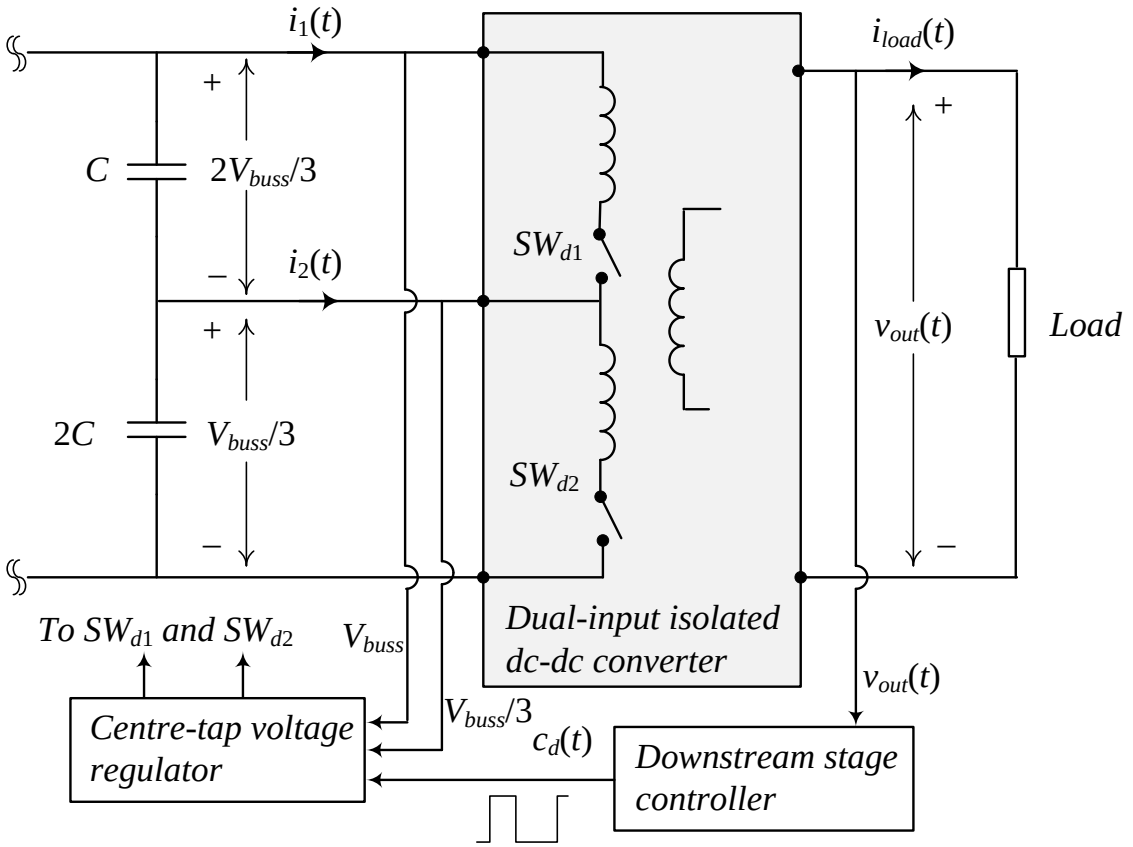


Sampling Logic



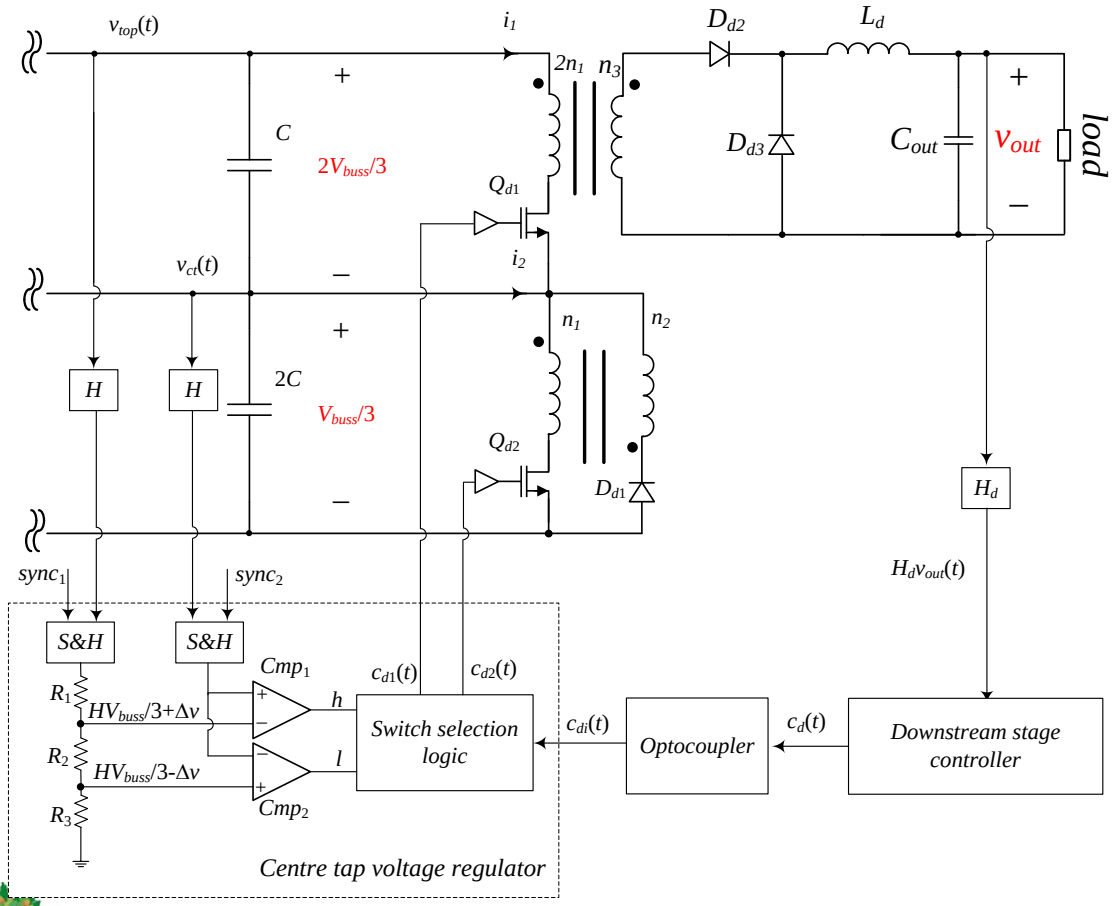


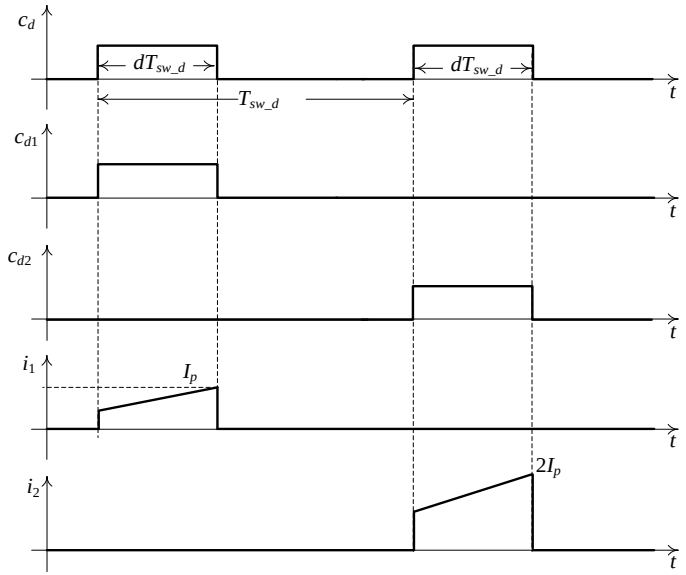
Centre Tap Voltage Balancing



Balancing is performed with the two currents of the downstream stage.

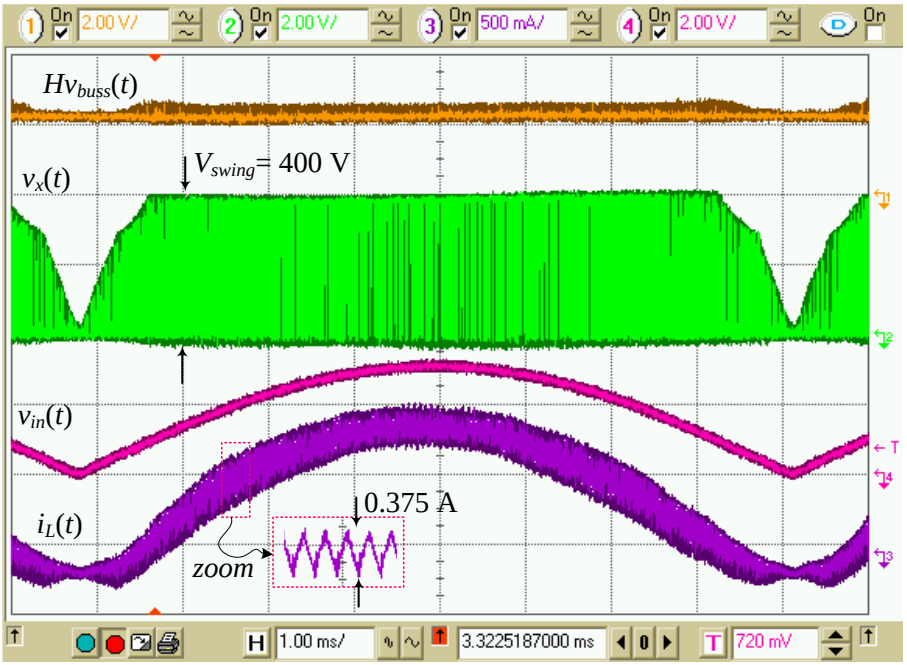
Practical Implementation

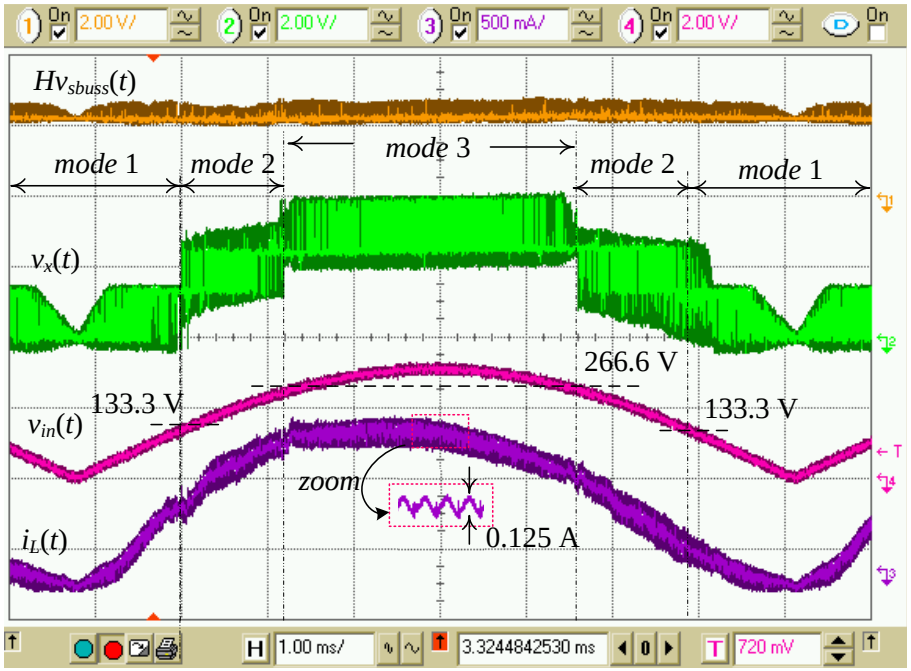




Conventional two-input forward and flyback also possible

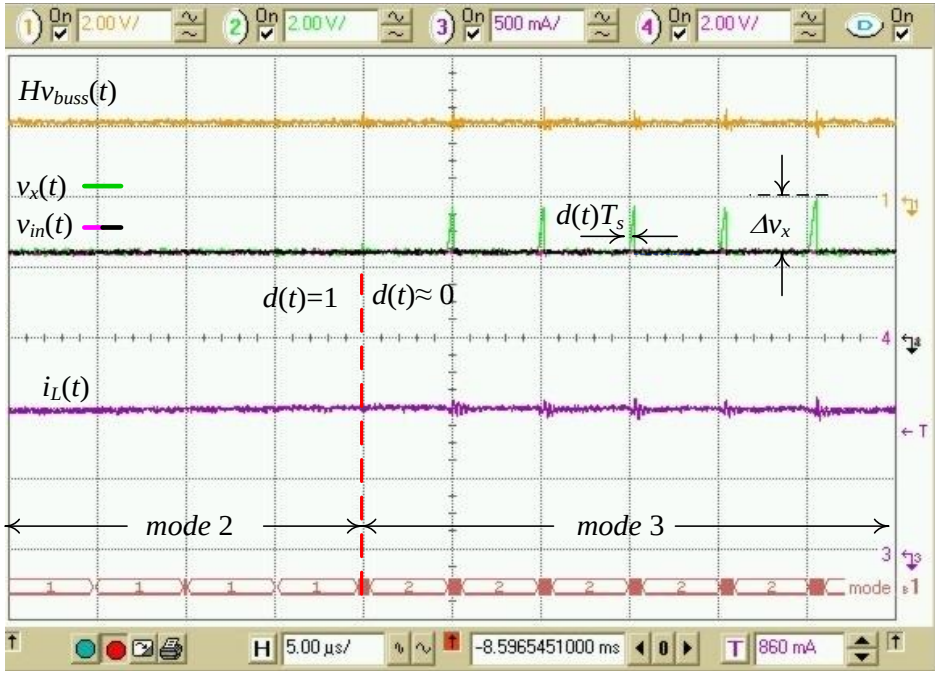
Experimental Waveforms – Comparison with Conventional PFC

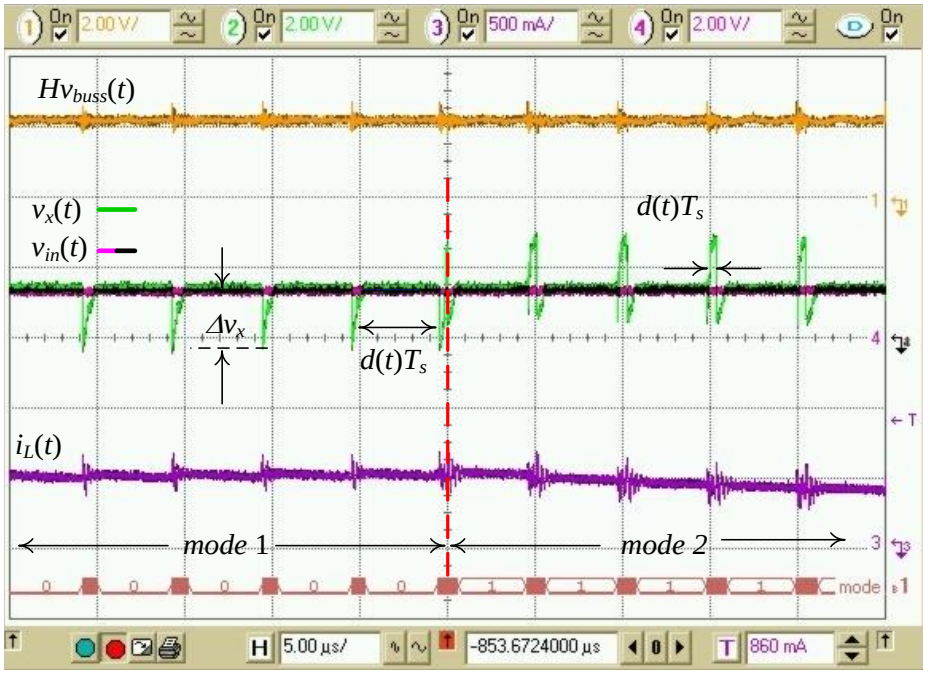




Only for this measurement the same inductors of 670 μH were used – 3 times smaller ripple of Non-Symmetric Boost PFC (allows for 3 x smaller inductor)

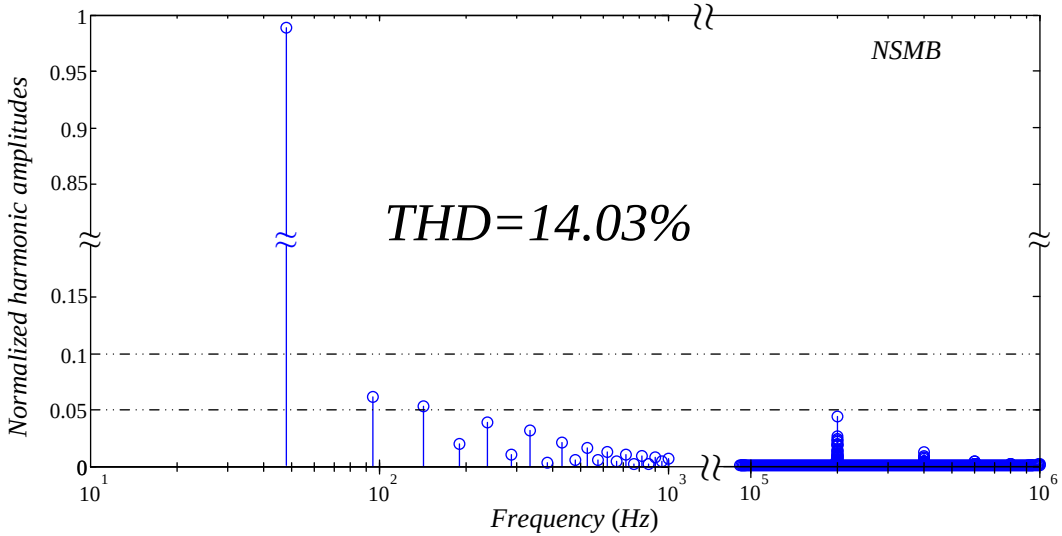
Mode Transitions and Voltage Swing

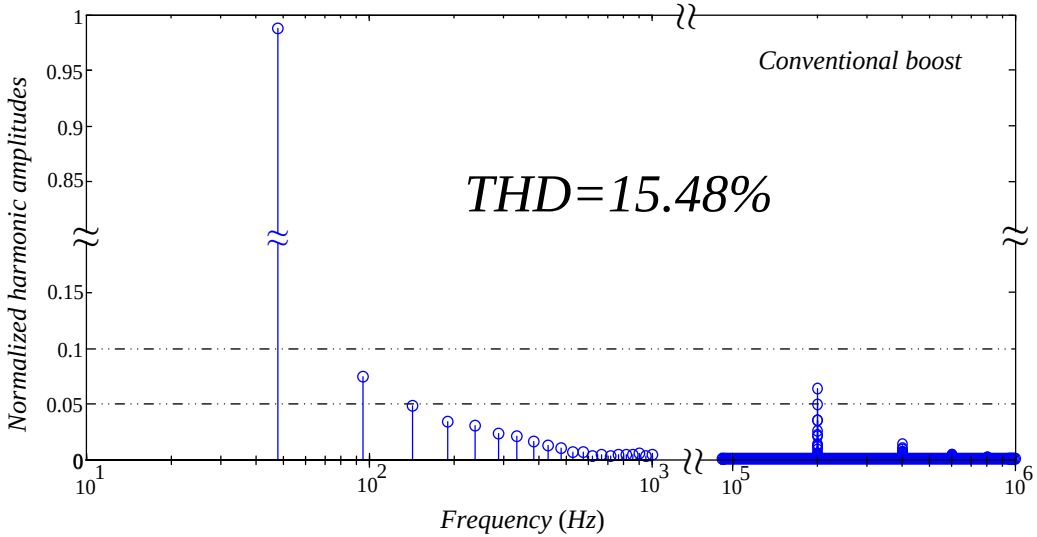




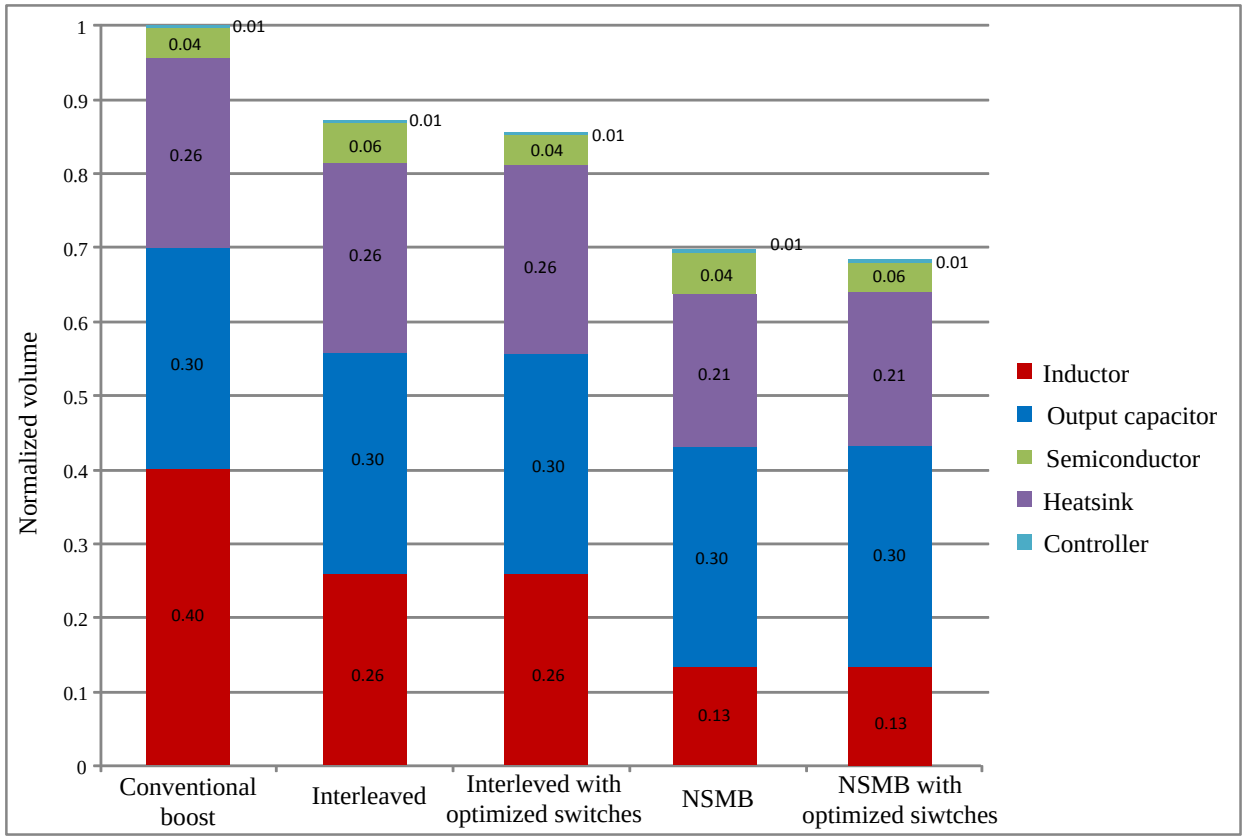
Smooth mode transitions and voltage swing reduced to 1/3 of previous value

Harmonics

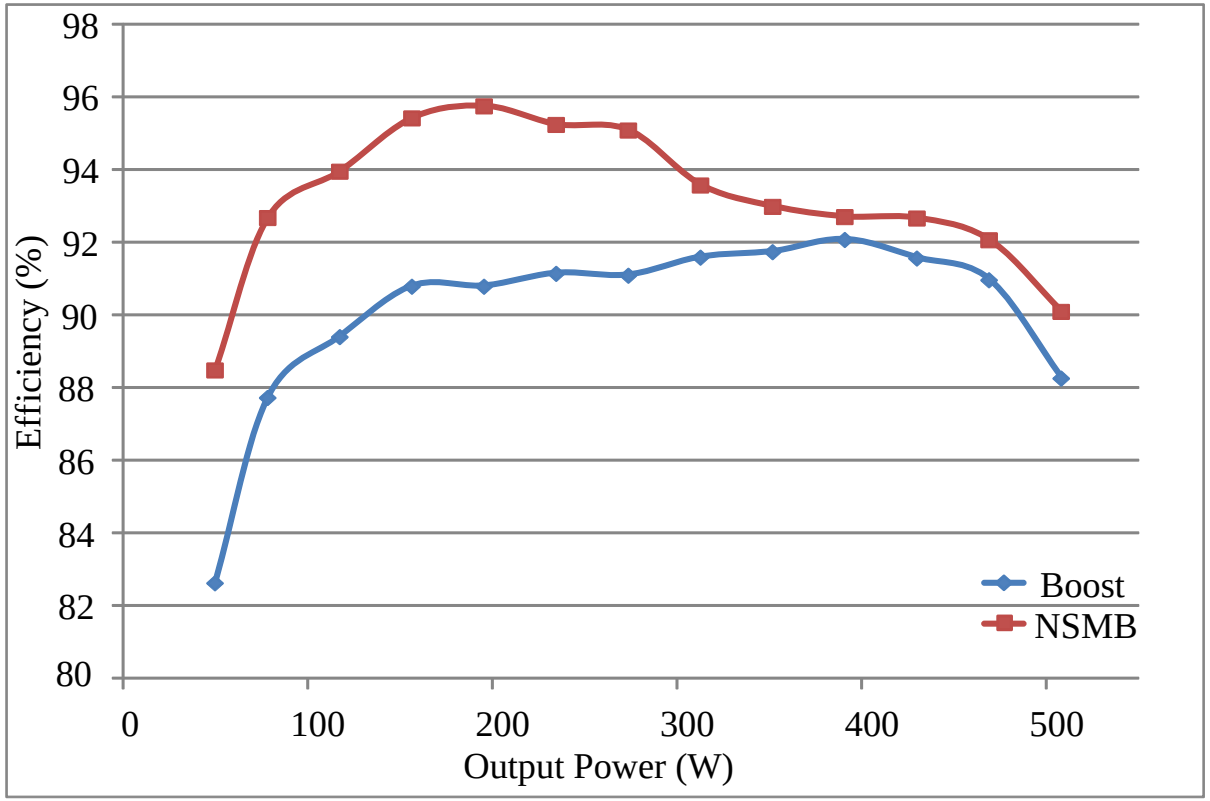

NSMB
THD=14.03%
Normalized harmonic amplitudes
Frequency (Hz)


Conventional boost
THD=15.48%
Normalized harmonic amplitudes
Frequency (Hz)

Volume Comparison



Efficiency Comparisons with Conventional PFC



Up to 6% improvement in efficiency even though the same components were used for both prototypes (Non-optimized design of the NSMB)

Conclusions

- *By utilizing flexibility much smaller, more efficient, and more reliable ac-dc (and dc-dc) converters can be designed.*
- *The improvements are results of tradeoff between complexity of control scheme and in some cases larger silicon utilization (favorable tradeoff)*
- *The mixed-signal controlled supplies can also offer some new features such as remote temperature and current estimation, on-line efficiency optimization, fault-tolerant operation, load and power supply health monitoring….*

Thank You.